The Memory and Microprocessor Data Book

for

Design Engineers

European Edition

TEXAS INSTRUMENTS

CC–420B

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INTRODUCTION

This book contains detailed specifications for semiconductor memory integrated circuits manufactured and supplied worldwide by Texas Instruments. A continuous upgrading of process and design technology has resulted in a wide spectrum of memory products with information retrieval times from a few nanoseconds to a few microseconds. They cover the basic memory functions of serial storage, random-access mass storage, permanent read-only storage and programmable read-only storage of binary information. These LSI high-technology products include:

- 42 MOS Memory products to provide system economy and large storage capacity from:
  - 11 state-of-the-art high-density single transistor cell 4096-bit RAM's designed specifically for mass storage systems
  - 12 economical industry-standard 1024-bit static RAM's for simplified application in small or medium size systems
  - 12 different shift registers featuring highly efficient organizations for implementing serial and recirculating memories in data communications and display systems
- 49 TTL high-performance memories, 44 with Schottky clamping, including:
  - 256-bit RAM's featuring modified 1^2L cell design and single-level metalization to enhance reliability
  - PROM's featuring Titanium-Tungsten fuse links for fast and reliable programming
  - New high density 20-pin 2048-bit and 4096-bit PROM's for reduced board area and system cost
- 7 ECL ultra-high performance memories including:
  - 5 RAM's with access times from 10 ns to 15 ns typically
  - 1 256-bit PROM using Titanium-Tungsten fuse links with a typical access time of 15 ns

Also included are product descriptions of 11 microprocessor products from Texas Instruments, 9 manufactured with MOS technology, one in Schottky TTL, and the other with Integrated Injection Logic (I^2L), a revolutionary new semiconductor technology. These new microprocessor products are directly compatible with most of the semiconductor memory products included in this book.

An eight-page glossary defines symbols and terms used with memory integrated circuits in accordance with current deliberations by the EIA/JEDEC (Electronic Industries Association) and IEC (International Electrotechnical Commission).

Ordering instructions and mechanical data for the package types available are given at the end of the section for each technology (MOS, TTL, and ECL).

The 38510/MACH IV Procurement Specification is included in its entirety and has been updated to include provisions for memory circuits and for the CMOS technology. A current listing of JAN MIL-M-38510 integrated circuits provides cross-reference from circuit type number to 38510 slash sheet and from 38510 slash sheet to circuit type number. Also covered are the 4096-bit RAMs processed to level III of the MACH IV specification.

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STOP PRESS

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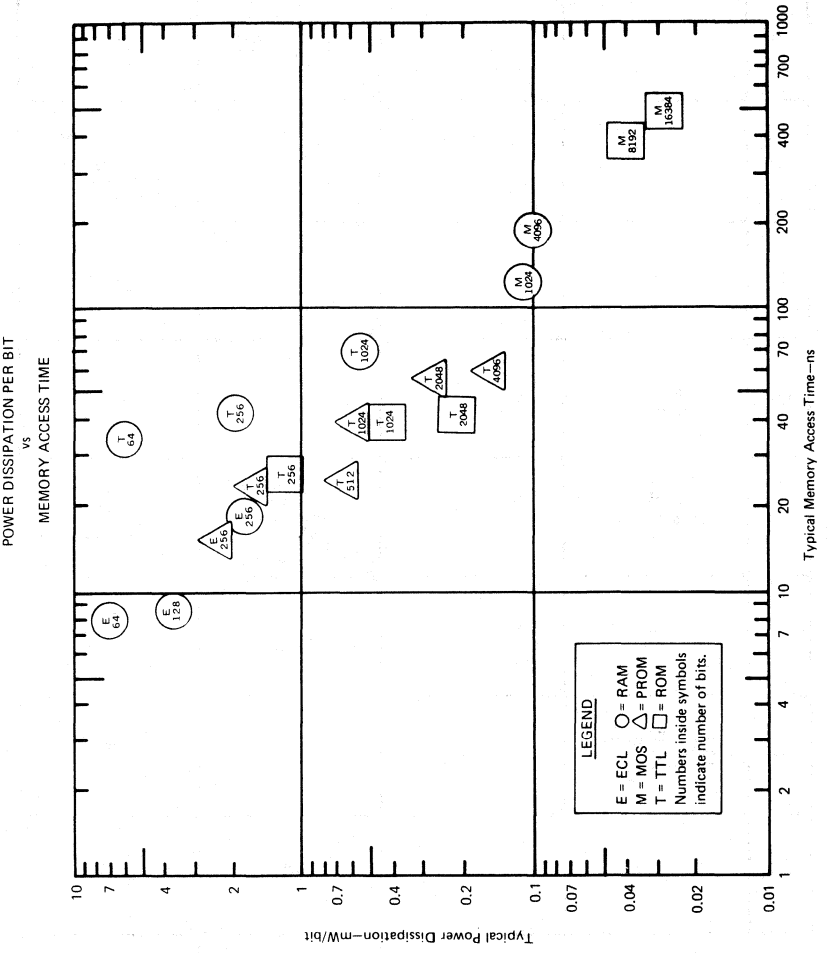
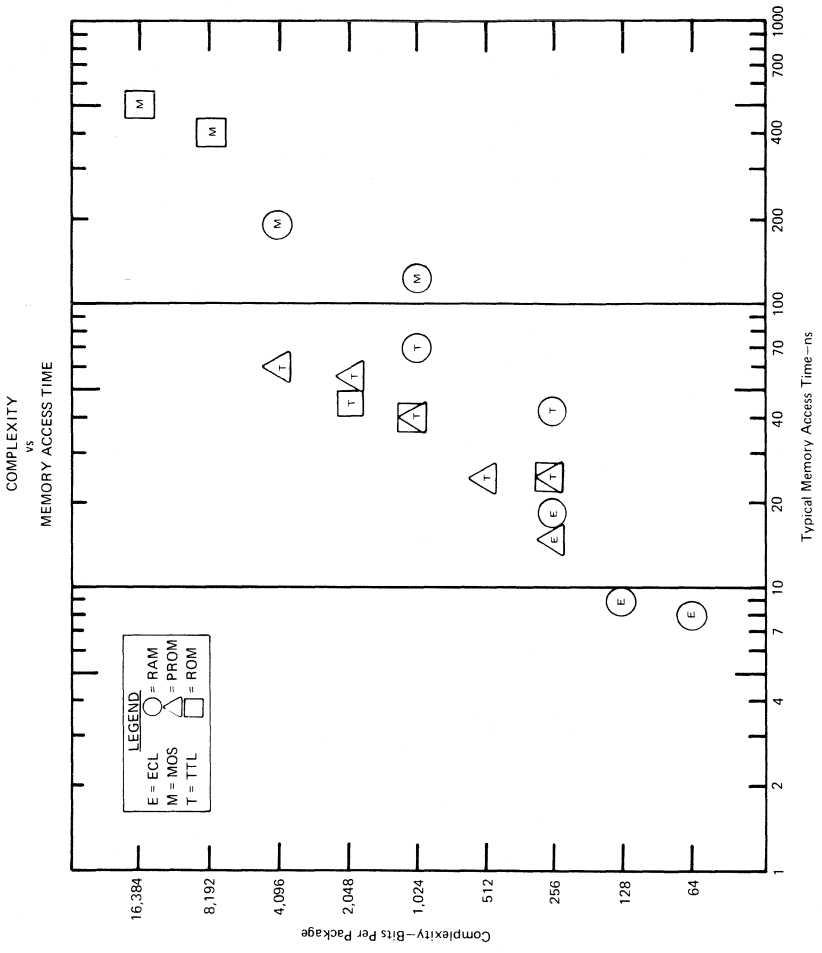
WORDS	BITS PER WORD			
	1	2	4	8
16	16	32	RAMs SN10145 SN54S189/SN74S189 SN54S289/SN74S289 SN7489	64
32	32	64	128	ROMs SN5488A/SN7488A PROMS SN54188A/SN74188A SN54S188/SN74S188 SN54S288/SN74S288
64	RAMs SN10140 SN10142 SN10148	128	256	RAMs TMS 4036 PROMs SN54186/SN74186
128	RAMs SN10147	256	512	1024
256	RAMs SN10144 SN54S201/SN74S201 SN54S301/SN74S301	512	RAMs TMS 4039, TMS 4042, TMS 4043 ROMs SN54187/SN74187 PROMs SN54S287/SN74S287 SN54S387/SN74S387	ROMs SN54S271/SN74S271 SN54S371/SN74S371 PROMs SN54S470/SN74S470 SN54S471/SN74S471
512	1024	2048	ROMs SN54S270/SN74S270 SN54S370/SN74S370	PROMs SN74S472 SN74S473
1024	RAMs TMS4033/TMS4034/TMS4035 SN54S214/SN54S314 SN54S207/SN54S208 SN54LS214/SN54LS314	2048	4096	ROMs TMS 4700
2048	4096	8192	16384	ROMs TMS 4800
4096	RAMs TMS 4030 TMS 4050 TMS 4051 TMS 4060	8192	ROMs TMS 4800	32768

Numbers on shaded lines indicate overall complexity


POWER DISSIPATION PER BIT
vs
MEMORY ACCESS TIME
Typical Power Dissipation—mW/bit
Typical Memory Access Time—ns
10
7
4
2
1
0.7
0.4
0.2
0.1
0.07
0.04
0.02
0.01
1
2
4
7
10
20
40
70
100
200
400
700
1000
E 64
E 128
E 256
E 256
T 64
T 256
T 256
T 256
T 512
T 1024
T 1024
1024
T 1024
T 2048
T 2048
T 4096
M 1024
M 4096
M 8192
M 16384
LEGEND
E = ECL
M = MOS
T = TTL
○ = RAM
△ = PROM
□ = ROM
Numbers inside symbols indicate number of bits.


COMPLEXITY
vs
MEMORY ACCESS TIME
LEGEND
E = ECL
M = MOS
T = TTL
= RAM
= PROM
= ROM
Complexity—Bits Per Package
16,384
8,192
4,096
2,048
1,024
512
256
128
64
1
2
4
7
10
20
40
70
100
200
400
700
1000
Typical Memory Access Time—ns

MEMORY INTEGRATED CIRCUIT TERMS AND DEFINITIONS

INTRODUCTION

This glossary consists of three parts: (1) general concepts and types of memories, (2) operating conditions and characteristics (including letter symbols), and (3) graphic symbols and logic conventions. The terms, symbols, abbreviations, and definitions used with memory integrated circuits have not, as yet, been standardized. All are currently under consideration by the EIA/JEDEC (Electronic Industries Association) and the IEC (International Electrotechnical Commission). The following are as consistent with the past and future works of these organizations as is possible to anticipate at this time.

PART I—GENERAL CONCEPTS AND TYPES OF MEMORIES

Chip-Enable Input

A control input to an integrated circuit that, depending on the logic level applied to it, will either permit or prevent operation of the device for input, internal transfer, manipulation, refreshing, and output of data.

NOTES: 1. Retention of data by a static memory is not affected by the logic level of the chip-enable input.
2. See "Chip-Select Input."

Chip-Select Input, Output-Enable Input

A control input to an integrated circuit that, depending on the logic level applied to it, will either permit or prevent the output of data from the device.

NOTES: 1. A chip-select input usually differs from a chip-enable input in that the chip-select input does not necessarily prevent input and internal manipulation of data when it disables the output, while the chip-enable input has that broader function.
2. When disabled by a chip-enable or chip-select signal, the outputs will assume a low level, a high level, or a floating (high-impedance) state, depending on the design of the particular circuit.

Dynamic (Read/Write) Memory

A read/write memory in which the cells require the repetitive application of control signals in order to retain the data stored.

NOTES: 1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

First-In, First-Out (FIFO) Memory; Digital Storage Buffer

A memory from which data bytes or words can be read in the same order, but not necessarily at the same rate, as that of the data entry.

Last-In, First-Out (LIFO) Memory

A memory from which data bytes or words can be read with the order reversed from that of data entry.

Mask-Programmed Read-Only Memory

A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Memory Cell

The smallest subdivision of a memory into which data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

GLOSSARY
MEMORY INTEGRATED CIRCUIT TERMS AND DEFINITIONS

Memory Integrated Circuit

An integrated circuit consisting of memory cells and usually including associated circuits such as those for address selection, amplifiers, etc.

Parallel Access

A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

1

Programmable Read-Only Memory (PROM)

A read-only memory that after being manufactured can have the data content of each memory cell altered once only.

Random-Access Memory (RAM)

A memory that provides access to any of its address locations in any desired sequence with similar nominal access time for each location.
NOTE: Although this term can be used with either read/write or read-only memories, it is often used by itself in referring to a read/write memory.

Read-Only Memory (ROM)

A memory intended to be read only.
NOTE: Unless otherwise qualified, the term "read-only memory" implies that the content is unalterable and defined by construction.

Read/Write Memory

A memory in which each cell may be selected by applying appropriate electronic input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electronic input signals.

Reprogrammable Read-Only Memory

A read-only memory that after being manufactured can have the data content of each memory cell altered more than once.

Serial Access

A feature of a memory by which all the bits of a byte or word are entered sequentially at a single input or retrieved sequentially from a single output.

Static (Read/Write) Memory

A read/write memory in which the data is retained in the absence of control signals.
NOTES: 1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. A static memory may use dynamic addressing or sensing circuits.

Volatile Memory

A memory the data content of which is lost when power is removed.

PART II—OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

The symbols for quantities involving time use upper and lower case letters according to the following historically evolved principles:

a. Time itself, is always represented by a lower case t.

b. Subscripts are lower case when one or more letters represent single words, e.g. d for delay, su for setup, rd for read, wr for write.

c. Multiple subscripts are upper case when each letter stands for a different word, e.g. CS for chip select, PLH for propagation delay from low to high, RMW for read, modify write.

Access Time

The time between the application of a specified input pulse during a read cycle and the availability of valid data signals at an output.

Example symbology:

$t_{a(ad,LH)}$	Access time from address, low-to-high-level output
$t_{a(ad,HL)}$	Access time from address, high-to-low-level output
$t_{a(CE)}$	Access time from chip enable
$t_{a(CS)}$	Access time from chip select

Current

High-level input current, I_{IH}
The current into* an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}
The current into* an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}
The current into* an output when the output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}, I_{DD}, I_{EE}, I_{GG}, I_{SS}
The current into*, respectively, the V_{CC}, V_{DD}, V_{EE}, V_{GG}, or V_{SS} supply terminal of an integrated circuit.

*Current out of a terminal is given as a negative value.

GLOSSARY
MEMORY INTEGRATED CIRCUIT TERMS AND DEFINITIONS

Cycle Time

Read cycle time, $t_{c(rd)}$ (see note)
The time interval between the start of a read cycle and the start of the next cycle.

Read, modify write cycle time, $t_{c(RMW)}$ (see note)
The time interval between the start of a cycle in which the memory is read and new data is entered and the start of the next cycle.

Write cycle time, $t_{c(wr)}$ (see note)
The time interval between the start of a write cycle and the start of the next cycle.

NOTE: The read, write, or read, modify write cycle time is the actual interval between two impulses and may be insufficient for the completion of operations within the memory. A minimum value is specified that is the shortest time in which the memory will perform its read and/or write function correctly.

Data Valid Time

Data valid time with respect to chip select, $t_{DV(CS)}$
The interval following chip deselection during which output data continues to be valid.

Data valid time with respect to address, $t_{DV(ad)}$
The interval following an initial change of address during which data stored at the initial address continues to be valid at the output.

Delay Time

The time between the specified reference points on two waveforms.

Example symbology:

$t_{d(\phi 1\text{-}\phi 2)}$	Delay time, clock 1 to clock 2
$t_{d(PH\text{-}CEH)}$	Delay time, precharge high to chip enable high

Hold Time

Hold time, t_h
The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Example symbology:

$t_{h(ad)}$	Address hold time
$t_{h(da)}$	Data hold time
$t_{h(rd)}$	Read hold time
$t_{h(wr)}$	Write hold time
$t_{h(rs)}$	Reset hold time

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

Output disable time (of a three-state output) from high or low level, t_{PXZ}
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Propagation Time

Propagation delay time, t_{PD}
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

Pulse Width

Pulse width, t_w
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

$t_{w(CEH)}$	Pulse width, chip enable high
$t_{w(CEL)}$	Pulse width, chip enable low
$t_{w(clr)}$	Clear pulse width
$t_{w(CS)}$	Chip-select pulse width
$t_{w(\phi)}$	Clock pulse width
$t_{w(rs)}$	Reset pulse width
$t_{w(wr)}$	Write pulse width

Recovery Time

Sense recovery time, t_{SR}
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

Write recovery time
The time interval between the termination of a write pulse and the initiation of a new cycle.

Refresh Time

Refresh time, $t_{refresh}$ (see note)
The time interval between successive signals that are intended to restore the level in a dynamic memory cell to its original level.

NOTE: The refresh time is the actual time between two refresh operations and may be insufficient to protect the stored data. A maximum value is specified that is the longest interval for which correct operation is guaranteed.

Setup Time

Setup time, t_{su}
The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

Example symbology:

$t_{su(ad)}$	Address setup time
$t_{su(da)}$	Data setup time
$t_{su(rd)}$	Read setup time
$t_{su(wr)}$	Write setup time

Transition Time

Transition time, low-to-high-level, t_{TLH}
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

Transition time, high-to-low-level, t_{THL}
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

Voltage

High-level input voltage, V_{IH}
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum or B-limit value (V_{IHB}, $V_{IH'B}$) is specified that is the least positive (most negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed. For ECL circuits, a least-negative-limit value (V_{IHA}) is also specified.

High-level output voltage, V_{OH}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Input clamp voltage, V_{IK}
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum or A-limit value (V_{ILA} or $V_{IL'A}$) is specified that is the most positive (least negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed. For ECL circuits, a most-negative-limit value (V_{ILB}) is also specified.

Low-level output voltage, V_{OL}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

PART III—GRAPHIC SYMBOLS AND LOGIC CONVENTIONS

All graphic symbols shown in this section are standard in the USA (ANSI and IEEE) and internationally (IEC).

Negation and Polarity Indication, Use of Bars

In this book, the logic negation symbol ○ and the polarity indicator ▷ are used interchangeably to indicate:

a. A control input (e.g. chip select) that is active when it is at its low logic level.

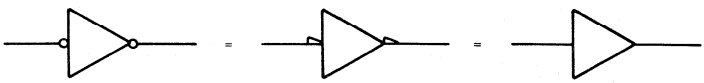
b. A dynamic input (e.g. clock) that is active on its high-to-low transition.

c. A data input that is out of phase with a data output that is not marked with a negation symbol or polarity indicator.

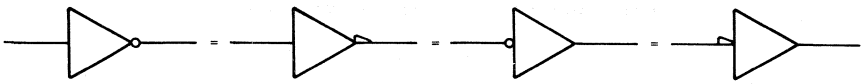
d. A data output that is out of phase with a data input that is not marked with a negation symbol or polarity indicator.

NOTE: If both data input and output are marked with a negation symbol or polarity indicator, they are in phase with each other. When used with a memory, the terms "in phase," "out of phase," and "inverted" refer to the relationship between the level at the input when a particular data bit is entered and the level at the output when that same bit is retrieved, not to the input and output levels at a given instant.

These three symbols are equivalent and represent a noninverting function:



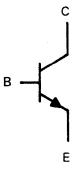
These four symbols are equivalent and represent an inverting function:



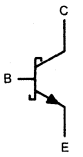
Letter abbreviations that represent inputs or outputs meeting criteria a, b, c, or d above are usually used with a bar.

Examples: $\overline{CS}$ and $\overline{E}$ represent chip-select and enable inputs that select and enable when low and do not select and enable when high. $\overline{DO}$ represents a data output the signal levels of which are inverted (out of phase) with respect to data input DI.

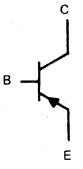
Transistor Graphic Symbols



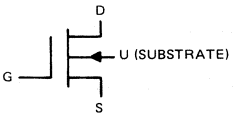
N-P-N BIPOLAR TRANSISTOR



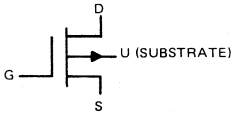
SCHOTTKY-CLAMPED N-P-N BIPOLAR TRANSISTOR



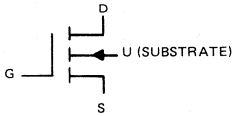
P-N-P BIPOLAR TRANSISTOR



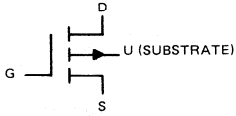
N-CHANNEL MOS DEPLETION-TYPE FIELD-EFFECT TRANSISTOR



P-CHANNEL MOS DEPLETION-TYPE FIELD-EFFECT TRANSISTOR



N-CHANNEL MOS ENHANCEMENT-TYPE FIELD-EFFECT TRANSISTOR



P-CHANNEL MOS ENHANCEMENT-TYPE FIELD-EFFECT TRANSISTOR

Interchangeability Guide

Direct replacements were based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

ECL CIRCUITS
(alphabetically by manufacturers)

ECL package cross-reference:

	TI	Fairchild	Motorola	Signetics
Ceramic dual-in-line	J	D	L	F
Ceramic and metal dual-in-line	JE		AL	

FAIRCHILD SEMICONDUCTOR

FSC TYPE	TI DIRECT REPLACEMENT
F10405	SN10147
F10410	SN10144

MOTOROLA

MOTOROLA TYPE	TI DIRECT REPLACEMENT
MMC10140	SN10140
MMC10142	SN10142
MMC10144	SN10144
MMC10145	SN10145
MMC10147	SN10147
MMC10148	SN10148

SIGNETICS

SIGNETICS TYPE	TI DIRECT REPLACEMENT
S10139	SN10139
S10140	SN10140
S10144	SN10144
S10145	SN10145
S10148	SN10148

MOS CIRCUITS
(alphabetically by manufacturers)

ADVANCED MICRO DEVICES

AMD TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
AM 1002	2 x 128 SSR		TMS 3128	2 x 128 SSR
AM 2521	2 x 128 SSR		TMS 3128	2 x 128 SSR
AM 2809	2 x 128 SSR		TMS 3128	2 x 128 SSR
AM 2810	2 x 128 SSR		TMS 3128	2 x 128 SSR
AM 2814	2 x 128 SSR	TMS 3114	TMS 3128	2 x 128 SSR
AM 3114	2 x 128 SSR	TMS 3114	TMS 3128	2 x 128 SSR
AM 9102	1 x 1024 SRAM	TMS 4034	TMS 4051	1 x 4096 DRAM
AM 9102A	1 x 1024 SRAM	TMS 4033	TMS 4051	1 x 4096 DRAM

AMERICAN MICROSYSTEMS INCORPORATED

AMI TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
S 1463	2 x 64 SSR		TMS 3121	4 x 64 SSR
S 2103	1 x 1024 DRAM		TMS 4030	1 x 4096 DRAM
S 2146	1 x 1024 DRAM		TMS 4030	1 x 4096 DRAM
S 3102	1 x 1024 SRAM	TMS 4035	TMS 4051	1 x 4096 DRAM
S 3102A	1 x 1024 SRAM	TMS 4033	TMS 4051	1 x 4096 DRAM
S 3102B	1 x 1024 SRAM	TMS 4034	TMS 4051	1 x 4096 DRAM
S 3103	1 x 1024 DRAM		TMS 4050	1 x 4096 DRAM
S 4006	1 x 1024 DRAM		TMS 4050	1 x 4096 DRAM
S 4008	1 x 1024 DRAM		TMS 4050	1 x 4096 DRAM

ELECTRONIC ARRAYS

EA TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
EA 1008	2 x 80 SSR		TMS 3120	4 x 80 SSR
EA 1009	2 x 80 SSR		TMS 3120	4 x 80 SSR
EA 1213	4 x 80 DSR		TMS 3120	4 x 80 SSR
EA 1214	4 x 80 DSR		TMS 3120	4 x 80 SSR
EA 2102	1 x 1024 SRAM	TMS 4035	TMS 4035	1 x 1024 SRAM
EA 3501	ASCII GEN		TMS 2501	ASCII GEN
EA 3701	ASCII GEN		TMS 4103	ASCII GEN
EA 4501	ASCII GEN		TMS 2501	ASCII GEN
EA 4800	8 x 2048 ROM	TMS 4800	TMS 4800	8 x 2048 ROM 4 x 4096 ROM
EA 4900	8 x 2048 ROM	TMS 4800	TMS 4800	8 x 2048 ROM 4 x 4096 ROM

FAIRCHILD SEMICONDUCTOR

FSC TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
3325	4 x 64 DSR		TMS 3121	4 x 64 DSR
3342	4 x 64 SSR	TMS 3121	TMS 3121	4 x 64 SSR
3343	2 x 128 SSR		TMS 3128	2 x 128 SSR
3344	2 x 132 SSR		TMS 3129	2 x 132 SSR
3346	2 x 144 SSR		TMS 3132	8 x 144 SSR
3347	4 x 80 SSR	TMS 3120	TMS 3120	4 x 80 SSR
3348/9	6 x 32 SSR	TMS 3112/22	TMS 3112	6 x 32 SSR
3383	1 x 256 DSR		TMS 3417	4 x 64 DSR
3524-5	1 x 1024 DRAM		TMS 4050	1 x 4096 DRAM

GENERAL INSTRUMENT

GI TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
SL-5-2100	2 x 128 SSR		TMS 3128	2 x 128 SSR
SL-6-2064	2 x 64 SSR		TMS 3121	4 x 64 SSR
SL-9-4080	4 x 80 SSR		TMS 3120	4 x 80 SSR
DL-6-2128	2 x 128 DSR		TMS 3128	2 x 128 SSR
RA -9-1103	1 x 1024 DRAM		TMS 4050	1 x 4096 DRAM
AY-5-1012	UART	TMS 6011	TMS 6011	UART

INTEL

INTEL TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
1103	1 x 1024 DRAM	TMS 1103	TMS 4050/4051 TMS4060	1 x 4096 DRAM 1 x 4096 DRAM
1311/12/13	ASCII GEN		TMS 2501	ASCII GEN
2101	4 x 256 SRAM	TMS 4039	TMS 4039	4 x 256 SRAM
2101-1	4 x 256 SRAM	TMS 4039-2	TMS 4039-2	4 x 256 SRAM
2101-2	4 x 256 SRAM	TMS 4039-1	TMS 4039-1	4 x 256 SRAM
2102-1	1 x 1024 SRAM	TMS 4033	TMS 4033	1 x 1024 SRAM
2102-2	1 x 1024 SRAM	TMS 4034	TMS 4034	1 x 1024 SRAM
2102	1 x 1024 SRAM	TMS 4035	TMS 4035	1 x 1024 SRAM
2111	4 x 256 SRAM	TMS 4042	TMS 4042	4 x 256 SRAM
2111-1	4 x 256 SRAM	TMS 4042-2	TMS 4042-2	4 x 256 SRAM
2111-2	4 x 256 SRAM	TMS 4042-1	TMS 4043-1	4 x 256 SRAM
2112	4 x 256 SRAM	TMS 4043	TMS 4043	4 x 256 SRAM
2112-2	4 x 256 SRAM	TMS 4043-1	TMS 4043-1 TMS 4043-2	4 x 256 SRAM
2107A	1 x 4096 DRAM	TMS 4030/4060	TMS 4030/4060	1 x 4096 DRAM
8308	8 x 1024 ROM	TMS 4700	TMS 4700	8 x 1024 ROM

INTERSIL

INTERSIL TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
IM 7552	1 x 1024 SRAM	TMS 4035	TMS 4035/4051	1 x 1024 SRAM
IM 7552-2	1 x 1024 SRAM	TMS 4034	TMS 4034/4051	1 x 1024 SRAM
IM 7552-1	1 x 1024 SRAM	TMS 4033	TMS 4033/4051	1 x 1024 SRAM
IM 7780	4 x 80 DSR	TMS 3409	TMS 3120	4 x 80 DSR/SSR

MOSTEK

MOSTEK TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
1002	2 x 128 SSR		TMS 3128	2 x 128 SSR
1007	4 x 80 DSR	TMS 3409	TMS 3120	4 x 80 DSR/SSR
4096	1 x 4096 DRAM		TMS 4050/4060	1 x 4096 DRAM
4102P	1 x 1024-SRAM	TMS 4035	TMS 4051	1 x 1024 SRAM
4102P-1	1 x 1024 SRAM	TMS 4033	TMS 4051	1 x 1024 SRAM

NATIONAL SEMICONDUCTOR

NATIONAL TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
MM 1103	1 x 1024 DRAM	TMS 1103	TMS 4050	1 x 1024 DRAM
MM 2102	1 x 1024 SRAM	TMS 4035	TMS 4035	1 x 1024 SRAM
MM 4020	4 x 80 DSR		TMS 3120	4 x 80 SSR
MM 4105	4 x 64 DSR		TMS 3121	4 x 64 SSR
MM 4052	2 x 80 SSR		TMS 3120	2 x 80 SSR
MM 4060	2 x 128 SSR	TMS 3128	TMS 3128	2 x 128 SSR
MM 5260	1 x 1024 DRAM		TMS 4050/4060	1 x 4096 DRAM

SIGNETICS

SIGNETICS TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
1103	1 x 1024 DRAM		TMS 4050/4060	1 x 4096 DRAM
2513	2560 ROM		TMS 2501	2560 ASCII GEN
2521	2 x 128 SSR	TMS 3128	TMS 3128	2 x 128 SSR
2522	2 x 132 SSR	TMS 3129	TMS 3129	2 x 132 SSR
2532	4 x 80 SSR	TMS 3120	TMS 3120	4 x 80 SSR
2602	1 x 1024 SRAM	TMS 4035	TMS 4051	1 x 1024 SRAM
2602-1	1 x 1024 SRAM	TMS 4033	TMS 4051	1 x 1024 SRAM

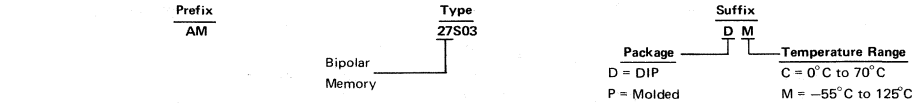
WESTERN DIGITAL

WD TYPE	DESCRIPTION	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	DESCRIPTION
TR 1602	UART	TMS 6011	TMS 6011	UART

TTL MEMORIES
(alphabetically by manufacturers)

ADVANCED MICRO DEVICES

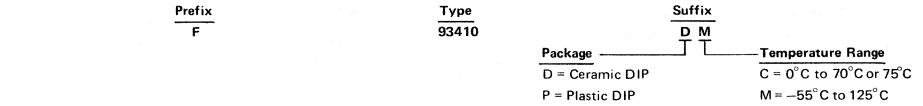
Example of AMD order code:



AMD TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS	AMD TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
2700	SN74S201	SN74S201	27S08M	SN54S188	SN54S188
2701	SN74S301	SN74S301	27S09C	SN74S288	SN74S288
27S02C	SN74S289	SN74S289	27S09M	SN54S288	SN54S288
27S02M	SN54S289	SN54S289	27S10C	SN74S387	SN74S387
27S03C	SN74S189	SN74S189	27S10M	SN54S387	SN54S387
27S03M	SN54S189	SN54S189	27S11C	SN74S287	SN74S287
27S08C	SN74S188	SN74S188	27S11M	SN54S287	SN54S287

FAIRCHILD SEMICONDUCTOR

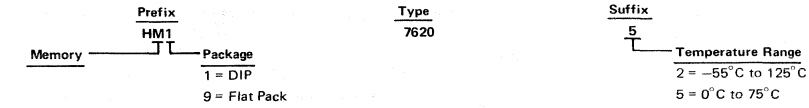
Example of Fairchild order code:



FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS	FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN
93403	SN74S289	SN74S289	93421C	SN74S201	SN74S201
93406C	SN74187	SN74S387	93421M	SN54S201	SN54S201
93410AC	SN74S301	SN74S301	93425AC	SN74S214	SN74S214
93410C	SN74S301	SN74S301	93425C	SN74S214	SN74S214
93410M	SN54S301	SN54S301	93426C	SN74S287	SN74S287
93411C	SN74S201	SN74S201	93426M	SN54S287	SN54S287
93411M	SN54S201	SN54S201	93434	SN7488A	SN74S188
93415AC	SN54S314	SN54S314	93436C	SN74S270	SN74S270
93415C	SN54S314	SN54S314	93436M	SN54S270	SN54S270
93416C	SN74S387	SN74S387	93446C	(SN74S370 ROM)	SN74S472
93417M	SN54S387	SN54S387	93446M	(SN54S370 ROM)	SN54S472

HARRIS SEMICONDUCTOR

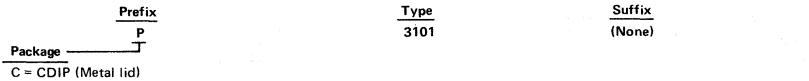
Example of Harris order code:



HARRIS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
H0512-38510	SNJ54186	SNJ54S287/SNJ54S387
HM_7602-2	SN54S188	SN54S188
HM_7602-5	SN74S188	SN74S188
HM_7603-2	SN54S288	SN54S288
HM_7603-5	SN74S288	SN74S288
HM_7610-2	SN54S387	SN54S387
HM_7610-5	SN74S387	SN74S387
HM_7611-2	SN54S287	SN54S287
HM_7611-5	SN74S287	SN74S287
HM_7620-2	(SN54S270 ROM)	SN54S387
HM_7620-5	(SN74S270 ROM)	SN74S387/SN74S473
HM_7621-2	(SN54S370 ROM)	SN54S287
HM_7621-5	(SN74S370 ROM)	SN74S287/SN74S472
HM_7640-2		SN54S287/SN54S471
HM_7640-5		SN74S287/SN74S472
HM_7641-2		SN54S387/SN54S470
HM_7641-5		SN74S387/SN74S473
HM_7642-2		SN54S287/SN54S471
HM_7642-5		SN74S472
HM_7643-2		SN54S387/SN54S470
HM_7643-5		SN74S473
HM_7644-2		SN54S287/SN54S471
HM_7644-5		SN74S472
HPROM0512-2	SN54186	SN54S470/SN54S471
HPROM0512-5	SN74186	SN74S470
HPROM1024-2	SN54S287	SN54S287
HPROM1024-5	SN74S287	SN74S287
HPROM1024A-2	SN54S387	SN54S387
HPROM1024A-5	SN74S387	SN74S387
HRPOM8256-2	SN54S188	SN54S188
HRPOM8256-2	SN54S188	SN74S188

INTEL

Example of Intel order code:

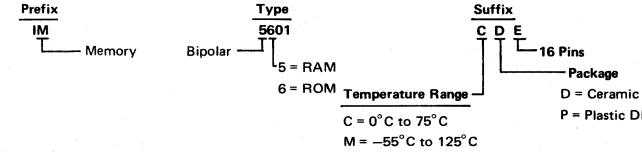


INTEL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
3101	SN54S289/SN74S289	SN54S289/SN74S289
3101A	SN54S289/SN74S289	SN54S289/SN74S289
3106	SN54S201/SN74S201	SN54S201/SN74S201
3106A	SN54S201/SN74S201	SN54S201/SN74S201
3107	SN54S301/SN74S301	SN54S301/SN74S301
3107A	SN54S301/SN74S301	SN54S301/SN74S301
3110	SN54S314	SN54S314
3301A	SN54187/SN74187	SN54S387
3304		SN54S473/SN74S473
3601	SN54S387/SN74S387	SN54S387/SN74S387
3604		SN54S473/SN74S473
3624		SN54S472/SN74S472

INTERCHANGEABILITY GUIDE

INTERSIL

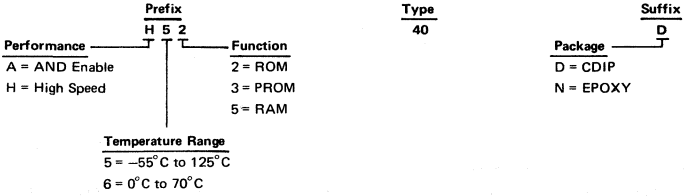
Example of Intersil order code:



INTERSIL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
IM5501C	SN74S289	SN74S289
IM5501M	SN54S289	SN54S289
IM5503AC	SN74S301	SN74S301
IM5503AM	SN54S301	SN54S301
IM5503C	SN74S301	SN74S301
IM5503M	SN54S301	SN54S301
IM5523AC	SN74S201	SN74S201
IM5523AM	SN54S201	SN54S201
IM5523C	SN74S201	SN74S201
IM5523M	SN54S201	SN54S201
IM5533AC	SN74S301	SN74S301
IM5533AM	SN54S301	SN54S301
IM5533C	SN74S301	SN74S301
IM5533M	SN54S301	SN54S301

INTERSIL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
IM5600C	SN74S188	SN74S188
IM5600CF	SN74S188	SN74S188
IM5600M	SN54S188	SN54S188
IM5603AC	SN74S387	SN74S387
IM5603AM	SN54S387	SN54S387
IM5604C	(SN74S270 ROM)	SN74S470
IM5604M	(SN54S270 ROM)	SN54S470
IM5610C	SN74S288	SN74S288
IM5610F	SN74S288	SN74S288
IM5610M	SN54S288	SN54S288
IM5623C	SN74S287	SN74S287
IM5623M	SN54S287	SN54S287
IM5624C	(SN74S370 ROM)	SN74S471
IM5624	(SN54S370 ROM)	SN54S471

MONOLITHIC MEMORIES, INC.



MMI TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
A5200		SN54S473
A5241		SN54S472
A6240		SN74S473
A6241		SN74S472
H5200	SN54187	SN54S387
H5201	(SN54S287 PROM)	SN54S370
H5240		SN54S473
H5241		SN54S472
H6201	(SN74S287 PROM)	SN74S370
H6240		SN74S473
H6241		SN74S472
5200	SN54187	SN54S387
5201	(SN54S387 PROM)	SN54S270
5205	SN54S270	SN54S270

MMI TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
5206	SN54S370	SN54S370
5210		SN54S470
5225		SN54S470
5230	SN5488A	SN54S188
5231	(SN54S188 PROM)	SN54S371
5235		SN54S470
5300	SN54S387	SN54S387
5301	SN54S287	SN54S287
5305	(SN54S270 ROM)	SN54S470
5306	(SN54S370 ROM)	SN54S471
5330	SN54S188	SN54S188
5331	SN54S288	SN54S288
5335		SN54S470
5340		SN54S473

MONOLITHIC MEMORIES, INC. (continued)

MMI TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
5530	SN54S301	SN54S301
5531	SN54S201	SN54S201
5560	SN54S289	SN54S289
5561	SN54S189	SN54S189
6200	SN74187	SN74S387
6201	(SN74S387 PROM)	SN74S270
6205	SN74S270	SN74S270
6206	SN74S370	SN74S370
6210		SN74S470
6225		SN74S473
6230	SN7488A	SN74S188
6231	(SN74S188 PROM)	SN74S371
6235		SN74S470
6300	SN74S387	SN74S387
6301	SN74S287	SN74S287
6305	(SN74S270 ROM)	SN74S470
6306	(SN74S370 ROM)	SN74S471
6330	SN74S188	SN74S188
6331	SN74S288	SN74S288
6335		SN74S470
6340		SN74S473
6530	SN74S301	SN74S301
6531	SN74S201	SN74S201
6560	SN74S289	SN74S289
6561	SN74S189	SN74S189

NATIONAL SEMICONDUCTOR

Prefix
DM
Digital Monolithic

Type
7599

Temperature Range
7 = –55°C to 125°C
8 = 0°C to 70°C

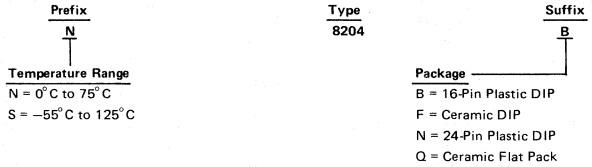
Suffix
N

Package
D = Glass/Metal DIP
F = Flat Package
N = Molded DIP

NSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
DM7573	SN54S387	SN54S387
DM7574	SN54S287	SN54S287
DM7577	SN54S188	SN54S188
DM7578	SN54S288	SN54S288
DM7595		SN54S473
DM7596		SN54S472
DM7597	SN54S370	SN54S370
DM7598		SN54S471
DM7599	SN54S189	SN54S189
DM7795		SN54S473
DM7796		SN54S472
DM8573	SN74S387	SN74S387
DM8574	SN74S287	SN74S287
DM8577	SN74S188	SN74S188
DM8578	SN74S288	SN74S288
DM8582	SN74S301	SN74S301
DM8595		SN74S473
DM8596		SN74S472
DM8597	SN74S370	SN74S370
DM8598		SN74S471
DM8599	SN74S189	SN74S189
DM85S99	SN74S189	SN74S189
DM8795		SN74S473
DM8796		SN74S472

SIGNETICS

Example of Signetics order code:



SIGNETICS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
N8204		SN74S471
N8205		SN74S472
N82S06	SN74S201	SN74S201
N82S07	SN74S301	SN74S301
N82S08	SN74S314	SN74S314
N82S10	SN74S314	SN74S314
N82S11	SN74S214	SN74S214
N82S16	SN74S201	SN74S201
N82S17	SN74S301	SN74S301
N8223	SN74S188	SN74S188
N82S23	SN74S188	SN74S188
N8225	SN74S189	SN74S189
N82S25	SN74S301	SN74S301
N82S110	SN74S314	SN74S314
N82S111	SN74S214	SN74S214
N82S114		SN74S471
N82S115		SN74S472
N82S116	SN74S201	SN74S201
N82S117	SN74S301	SN74S301
N82S123	SN74S288	SN74S288
N82S126	SN74S387	SN74S387
N82S129	SN74S287	SN74S287

SIGNETICS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
N82S130		SN74S473
N82S131		SN74S472
N82S226	SN74187	SN74S387
N82S229	(SN74S287 PROM)	SN74S370
N82S230	SN74S270	SN74S270
N82S231	SN74S370	SN74S370
S82S07	SN54S301	SN54S301
S82S16	SN54S201	SN54S201
S82S17	SN54S301	SN54S301
S82S23	SN54S188	SN54S188
S82S25	SN54S301	SN54S301
S82S114		SN54S471
S82S115		SN54S472
S82S123	SN54S288	SN54S288
S82S126	SN54S387	SN54S387
S82S129	SN54S287	SN54S287
S82S130		SN54S473
S82S131		SN54S472
S82S226	SN54187	
S82S229	(SN54S287 PROM)	SN54S370
S82S230	SN54S270	SN54S270
S72S231	SN54S370	SN54S370

MOS Memories

TMS 4030 JL, NL; TMS 4030-1 JL, NL; TMS 4030-2 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

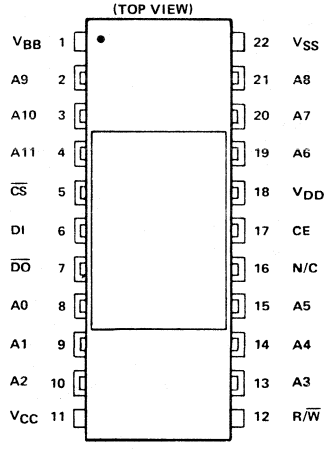
BULLETIN NO. DL-S 7512240, FEBRUARY 1975

- 4096 x 1 Organization
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4030	300 ns	470 ns	710 ns
TMS 4030-1	250 ns	430 ns	640 ns
TMS 4030-2	200 ns	400 ns	580 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed)
- Low Power Dissipation
  - 400 mW Operating (Typical)
  - 0.2 mW Standby (Typical)
- Single Low-Capacitance Clock
- N-Channel Silicon-Gate Technology
- 22-Pin 400-Mil Dual-in-Line Package

22-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 4030 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Three performance options are offered: 300 ns access for the TMS 4030, 250 ns access for the TMS 4030-1, and 200 ns for TMS 4030-2. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

All inputs except the chip enable are fully TTL-compatible and require no pull-up resistors. The low capacitance of the address and control inputs precludes the need for specialized drivers. When driven by a Series 74 device, the guaranteed dc input noise immunity is 200 mV. The TTL-compatible buffer is guaranteed to drive two Series 74 TTL gates. The TMS 4030 series uses only one clock (chip enable) to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers.

The typical power dissipation of these RAM's is 400 mW active and 0.2 mW standby. To retain data only 6 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4030 series is offered in both 22-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guarantted for operation from 0°C to 70°C. These packages are designed for insertion in mounting-hole rows on 0.400-mil centers.

operation

chip select ($\overline{CS}$)

The chip-select terminal, which can be driven from standard TTL circuits without an external pull-up resistor, affects the data-in, data-out and read/write inputs. The data input and data output terminals are enabled when chip select is low. Therefore, the read, write, and read, modify write operations are performed only when chip select is low. If the chip is to be selected for a given cycle, the chip-select input must be low on or before the rising edge of the chip enable. If the chip is not to be selected for a given cycle, chip select must be held high as long as chip enable is high. A register for the chip-select input is provided on the chip to reduce overhead and simplify system design.

chip enable (CE)

A single external clock input is required. All read, write, and read, modify write operations take place when the chip enable input is high. When the chip enable is low, the memory is in the low-power standby mode. No read/write operations can take place because the chip is automatically precharging.

operation (continued)

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected.

address (A0–A11)

All addresses must be stable on or before the rising edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data-in (DI)

Data is written during a write or read, modify write cycle while the chip enable is high. The data-in terminal can be driven from standard TTL circuits without a pull-up resistor. There is no register on the data-in terminal.

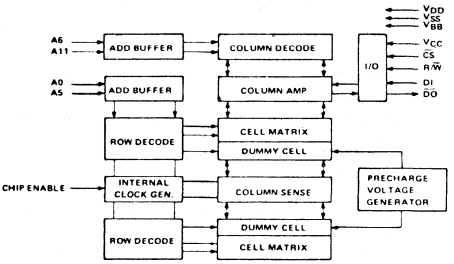
data-out ($\overline{DO}$)

The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates. The output is in the high-impedance (floating) state when the chip enable is low. It remains in the high-impedance state if the chip-select input is high when chip enable goes high and provided that chip select remains high as long as chip enable is high. If the chip select is set up low prior to the rise of chip enable and held low an interval after that rise, the output will be enabled as long as chip enable stays high regardless of subsequent changes in the level of chip select. A data-valid mode is always preceded by a low output state. Data-out is inverted from data-in.

refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs, A0 through A5 (pins 8, 9, 10, 13, 14, 15), or by addressing every row within any 2-millisecond period. Addressing any row refreshes all 64 bits in that row. The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, then chip select must be high. The column addresses (A6 through A11) can be indeterminate during refresh.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note) . . . . . −0.3 to 20 V
Supply voltage, V_{DD} (see Note) . . . . . −0.3 to 20 V
Supply voltage, V_{SS} (see Note) . . . . . −0.3 to 20 V
All input voltages (see Note) . . . . . −0.3 to 20 V
Chip-enable voltage (see Note) . . . . . −0.3 to 20 V
Output voltage (operating, with respect to V_{SS}) . . . . . −2 to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

recommended operating conditions (see Note)

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−2.7	−3	−3.3	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.25	V
High-level chip enable input voltage, $V_{IH(CE)}$	V_{DD} −0.6		V_{DD} +1.0	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note)	−0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$ (see Note)	−1		0.6	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTE: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −2 mA		2.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_O = 3.2 mA		V_{SS}		0.4	V
I_I	Input current (all inputs except chip enable)	V_I = 0 to 5.25 V				10	μA
$I_{I(CE)}$	Chip enable input current	V_I = 0 to 13.2 V				2	μA
I_{OZ}	High-impedance-state (off-state output current	V_O = 0 to 5.25 V				10	μA
I_{CC}	Supply current from V_{CC}	2 Series 74 TTL loads				1	mA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 12.6 V			30	60	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V			20	200	μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle time	TMS 4030		32		mA
			TMS 4030-1		35		
			TMS 4030-2		38		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle	Minimum cycle time	TMS 4030		32		mA
			TMS 4030-1		35		
			TMS 4030-2		38		
I_{BB}	Supply current from V_{BB}	V_{BB} = −3.3 V, V_{DD} = 12.6 V,	V_{CC} = 5.25 V, V_{SS} = 0 V		−5	−100	μA

† All typical values are at T_A = 25°C

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −3 V, V_{CC} = 5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 10.8 V		18	22	pF
		$V_{I(CE)}$ = −1,0 V		23	27	
$C_{i(\overline{CS})}$	Input capacitance chip select input			4	6	pF
$C_{i(data)}$	Input capacitance data input			4	6	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
C_o	Output capacitance			5	7	pF

† All typical values are at T_A = 25°C.

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4030		TMS 4030-1		TMS 4030-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(rd)}$	Read setup time	0↑		0↑		0↑		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

read cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4030		TMS 4030-1		TMS 4030-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable†		280		230		180	ns
$t_{a(ad)}$	Access time from address†		300		250		200	ns
t_{PHZ} or t_{PLZ}	Output disable time from high or low level‡	30		30		30		ns
t_{PZL}	Output enable time to low level‡		250		200		150	ns

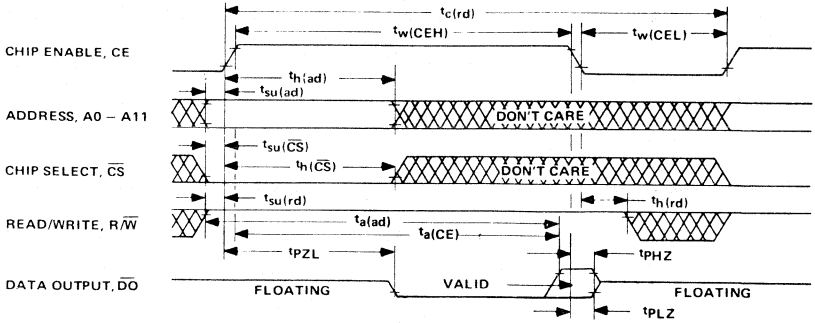
†Test conditions: C_L = 50 pF, $t_{r(CE)}$ = 20 ns, Load = 1 Series 74 TTL gate.
‡Test conditions: C_L = 50 pF, Load = 1 Series 74 TTL gate.

write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4030		TMS 4030-1		TMS 4030-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time*	0		0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

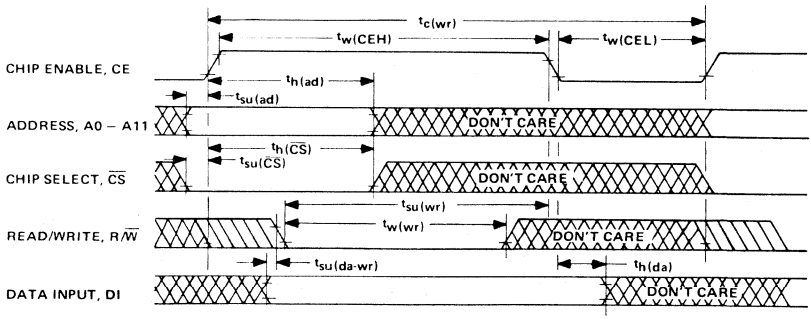
↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*If R/$\overline{W}$ is low before CE goes high then DI must be valid when CE goes high.

read cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high). During the time from the rise of CE to the fall of R/$\overline{W}$, R/$\overline{W}$ is permitted to change from high to low only.

read, modify write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4030		TMS 4030-1		TMS 4030-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(RMW)}$	Read, modify write cycle time*	710		640		580		ns
$t_{w(CEH)}$	Pulse width, chip enable high*	540	4000	470	4000	410	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write-pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time	0		0		0		ns
$t_{su(rd)}$	Read pulse setup time	0↑		0↑		0↑		ns
$t_{su(wr)}$	Write pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	280↑		230↑		180↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

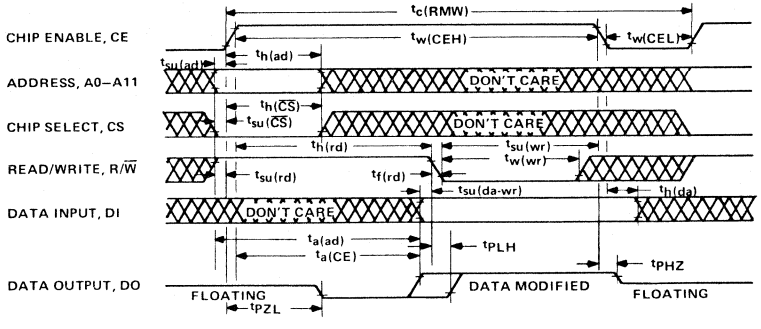
↑↓ The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*Test conditions: $t_{f(rd)}$ = 20 ns.

read, modify write cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4030		TMS 4030-1		TMS 4030-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable†		280		230		180	ns
$t_{a(ad)}$	Access time from address†		300		250		200	ns
t_{PLH}	Propagation delay time, low-to-high level output from write pulse‡	30		30		30		ns
t_{PHZ}	Output disable time from high level‡	30		30		30		ns
t_{PZL}	Output enable time to low level‡		250		200		150	ns

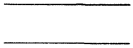
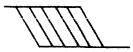
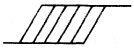
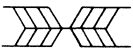
†Test conditions: C_L = 50 pF, $t_{r(CE)}$ = 20 ns, Load = 1 Series 74 TTL gate.
‡Test Conditions: C_L = 50 pF, Load = 1 Series 74 TTL gate.

read, modify write cycle timing



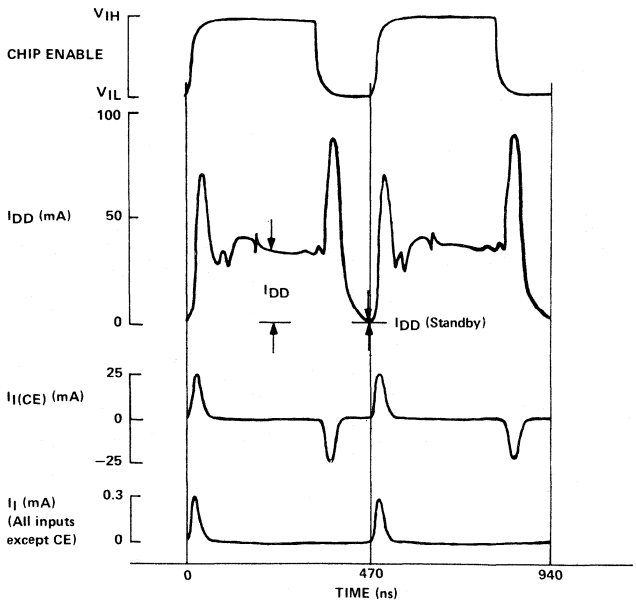
NOTE: For the chip enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

timing diagram conventions

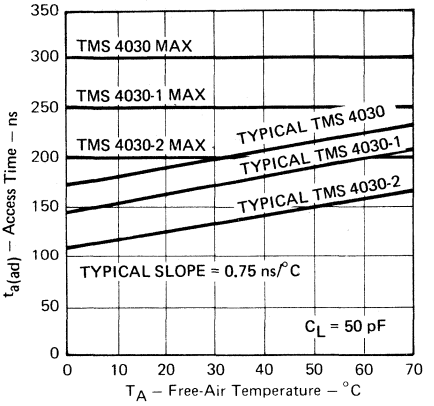
TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

3

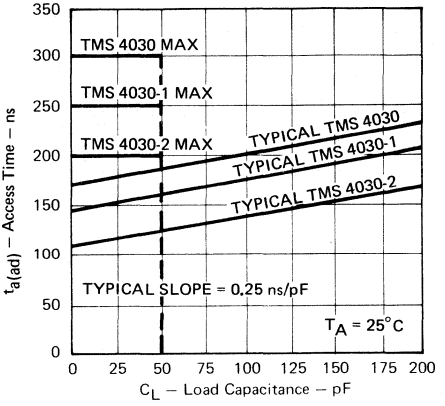
TYPICAL WAVEFORMS



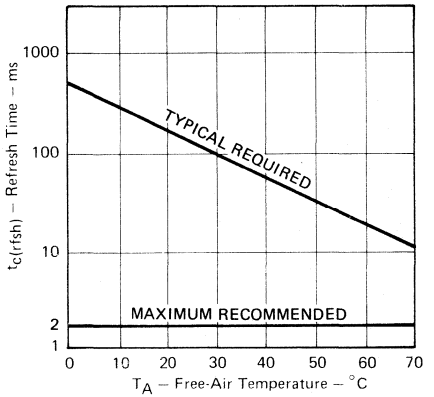
ACCESS TIMES vs TEMPERATURE



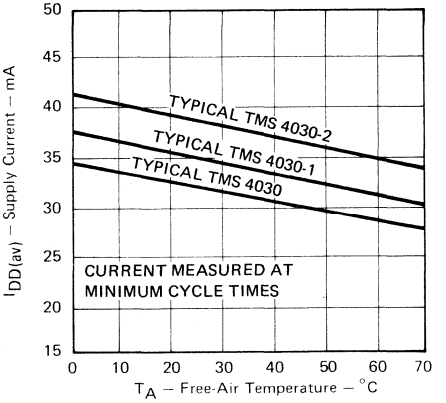
ACCESS TIMES vs LOAD CAPACITANCE



REFRESH TIME vs TEMPERATURE



AVERAGE CURRENT vs TEMPERATURE

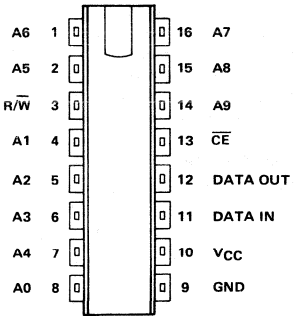


TMS 4033 JL, NL; TMS 4034 JL, NL; TMS 4035 JL, NL
1024-WORD BY 1-BIT STATIC RANDOM-ACCESS MEMORIES

BULLETIN NO. DL-S 7512189, OCTOBER 1974—REVISED MAY 1975

- 1024 x 1-Bit Organization
- Static Operation (No Clocks, No Refresh)
- Input Interface
  - Fully Decoded
  - TTL Compatible
  - Static Charge Protection
- Output Interface
  - 3-State
  - Fan-out 1 Series 74 TTL Load
  - OR-Tie Capability
- Access Time
  - TMS 4033 JL, NL . . . 450 ns Max
  - TMS 4034 JL, NL . . . 650 ns Max
  - TMS 4035 JL, NL . . . 1000 ns Max
- Interchangeable with Intel 2102-1, 2102-2, and 2102 Respectively
- N-Channel Silicon-Gate Technology

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



3

description

This series is a family of static random-access memories, each organized as 1024 one-bit words. Due to their static design, system overhead costs are minimized by elimination of refresh-clocking circuitry and by simplification of the timing requirements. In addition all inputs and outputs are fully compatible with Series 74 TTL, including the single 5-volt power supply. These memories are fabricated by means of the same technology employed with the TMS 4030 JL, NL 4K RAM – N-channel silicon-gate. This technology provides optimum chip density and performance when cost is considered. Three performance ranges allow the designer to better match the memory to the specific system requirements, thereby maximizing the cost/performance trade-off.

The TMS 4033, TMS 4034, and TMS 4035 are offered in 16-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from 0°C to 70°C.

operation

Addresses (A0-A9)

Address inputs are used to select individual storage locations within the RAM. Since the addresses are not latched, the address-valid time determines the cycle time during both the read and write cycle. Therefore, the address-valid time must be a minimum of 450 nanoseconds for the TMS 4033, 650 nanoseconds for the TMS 4034, and 1000 nanoseconds for the TMS 4035. The address inputs can be driven from standard Series 54/74 TTL with no external pull-up resistors.

operation (continued)

Chip Enable ($\overline{CE}$)

The $\overline{CE}$ input is used to enable the memory chip for a reading or writing operation. In a single-chip system, this pin can be hardwired to ground so that the chip is continuously enabled. For the read cycle, chip-enable low must extend past the address to ensure valid data for that address. Once the chip-enable goes high, the output buffer will immediately return to the high-impedance state. For the write cycle, chip-enable low must occur before the read/write input goes to the write state ensuring no ambiguity in the chip enabled for a particular write cycle. This input can be driven from Series 54/74 TTL with no external pull-up resistors.

Read/Write (R/$\overline{W}$)

In the write mode prior to an address change, R/$\overline{W}$ must be in the read state (high level) and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted location. The read/write input is TTL compatible without external pull-up resistors.

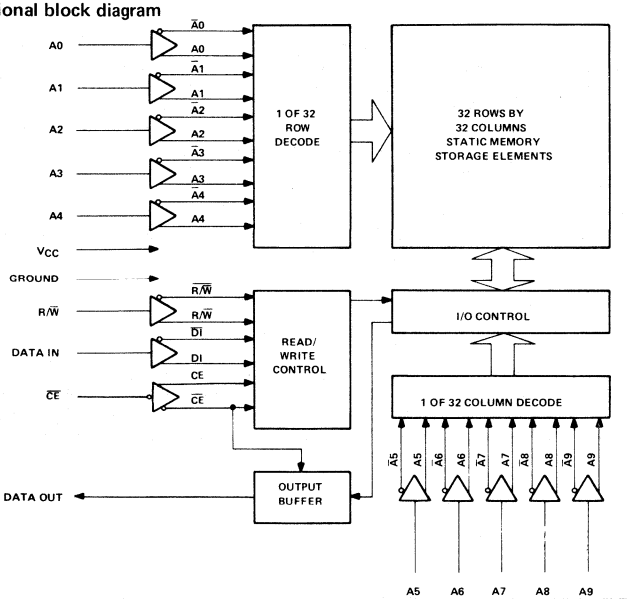
Data In (DI)

The DI input accepts the input data during the write mode. During a write cycle, data must be valid for a minimum time period before the read/write input is brought to the read state ensuring that proper data will enter the location selected. To eliminate any data ambiguity, data must be held valid past the end of the write pulse.

Data Out (DO)

Data out is a three-state terminal controlled by the chip-enable input, which supplies output data during a read cycle. A high level on chip enable places the data-out terminal in the high-impedance state.

functional block diagram



FUNCTION TABLE

$\overline{CE}$	R/$\overline{W}$	I/O
L	L	WRITE
L	H	READ
H	X	HIGH Z

H = HIGH LEVEL
L = LOW LEVEL

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . −0.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.3		0.65	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100 μA,	V_{CC} = 4.75 V	2.2			V
V_{OL}	Low-level output voltage	I_{OL} = 1.9 mA,	V_{CC} = 5.25 V			0.45	V
I_I	Input current	V_I = 0 to 5.25 V				±10	μA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 4 V			10	μA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 0.45 V		−10	−100	μA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25 V, All inputs at 5.25 V	Data out open,		45	70	mA
C_i	Input capacitance	T_A = 25°C,	f = 1 MHz		3	5	pF
C_o	Output capacitance	T_A = 25°C,	f = 1 MHz		7	10	pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

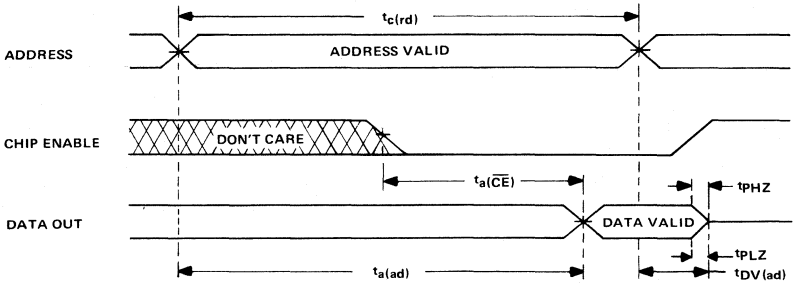
conditions for testing timing requirements

Input high levels . . . . . 2.2 V
Input low levels . . . . . 0.65 V
Input rise and fall times . . . . . 20 ns
Output load . . . . . 1 Series 74 TTL load, C_L = 100 pF
All timing requirements . . . . . 50% point of waveform

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C (unless otherwise noted)

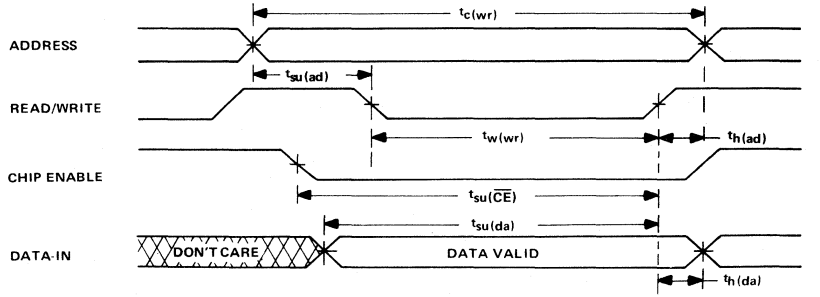
PARAMETER		TMS 4033			TMS 4034			TMS 4035			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{c(rd)}$	Read cycle time	450			650			1000			ns
$t_{a(ad)}$	Access time from address		300	450		450	650		500	1000	ns
$t_{a(\overline{CE})}$	Access time from chip enable			200			300			500	ns
$t_{DV(ad)}$	Previous output data valid from address	50			50			50			ns
t_{PHZ} or t_{PLZ}	Output disable time from chip enable	0		200	0		200	0		200	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.



write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4033		TMS 4034		TMS 4035		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	450		650		1000		ns
$t_{w(wr)}$	Write pulse width	250		400		750		ns
$t_{su(ad)}$	Address setup time	150		200		200		ns
$t_{su(\overline{CE})}$	Chip enable to write setup time	350		550		850		ns
$t_{su(da)}$	Data-in to write setup time	300		450		800		ns
$t_{h(ad)}$	Address hold time	50		50		50		ns
$t_{h(da)}$	Data hold time	50		50		50		ns



TEXAS INSTRUMENTS

TMS 4036 JL, NL; TMS 4036-1 JL, NL; TMS 4036-2 JL, NL
64-WORD BY 8-BIT STATIC RANDOM-ACCESS MEMORIES

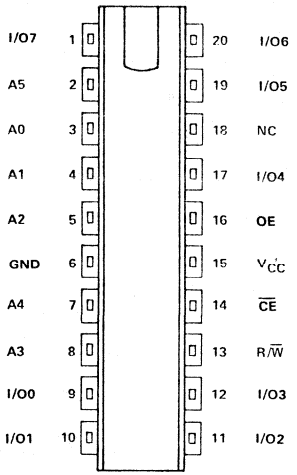
BULLETIN NO. DL-S 7512277, MAY 1975

- 64 x 8 Organization
- Static Operation (No Clocks, No Refresh)
- Compact 20-Pin 300-Mil Dual-in-Line Package
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4036	1000 ns	1000 ns
TMS 4036-1	650 ns	650 ns
TMS 4036-2	450 ns	450 ns

- Multiplexed Common Bus I/O
- Input Interface
  - Fully Decoded
  - TTL Compatible
  - Static Charge Protection
- Output Interface
  - 3-State
  - Fan-Out 1 Series 74 TTL Load
  - OR-Tie Capability
- Power Dissipation . . . 450 mW Maximum
- N-Channel Silicon-Gate Technology
- 8-Bit Word Length Ideal for Microprocessor-Based Systems

20-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

This series of static random-access memories is organized as 64 words of 8 bits. Data inputs and outputs are multiplexed on an 8-bit, bidirectional bus controlled by the combination of chip enable and output enable. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of the timing requirements. In addition, all inputs and outputs are fully compatible with Series 74 TTL, including the single 5-volt power supply. The TMS 4036 series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and the output data polarity is not inverted from data-in.

The TMS 4036 is offered in compact 20-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages designed for insertion in mounting-hole rows on 300-mil centers. The series is guaranteed for operation from 0°C to 70°C.

operation

addresses (A0-A5)

The 6-bit address selects one of 64 8-bit words. The address-valid time determines cycle time during both the read and write cycles. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors required.

operation (continued)

chip enable ($\overline{CE}$)

The $\overline{CE}$ terminal is used to enable a specific memory device. If $\overline{CE}$ is low, the device is enabled for either a read or write cycle, depending on the state of the read/write and output-enable terminals. When $\overline{CE}$ is high, the I/O buffers are in the high-impedance state. $\overline{CE}$ may be driven from Series 74 TTL. For a more complete understanding of $\overline{CE}$, see the section on output enable.

read/write (R/$\overline{W}$)

The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

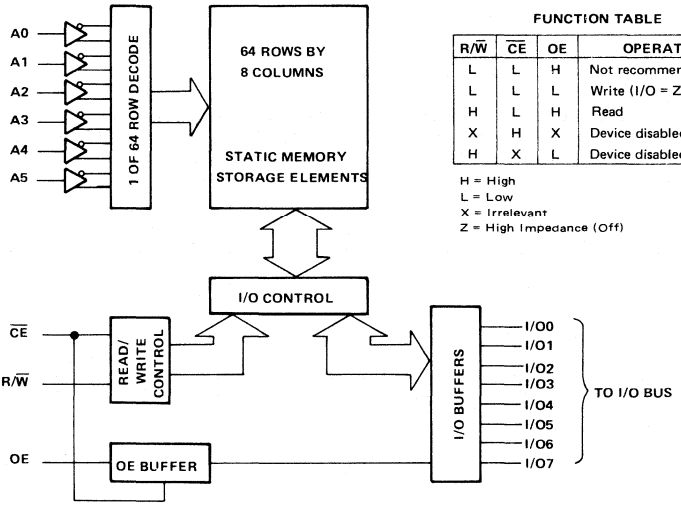
output enable (OE)

The output enable terminal controls the I/O buffer and determines whether the bus is in an input or output mode. When OE is low, the I/O terminals are in the input configuration; when OE is high, the I/O terminals are in the output configuration. The read cycle and write cycle timing diagrams show in detail the relation between $\overline{CE}$, OE, and the other signals (refer to the function table). This input is also compatible with Series 74 TTL circuits.

input/output buffer (I/O0-I/O7)

Each of these terminals interface directly with the external data bus and have the capability of being both an input and an output buffer. These buffers are controlled by a combination of $\overline{CE}$ and OE as described in the output enable section. Each buffer is three-state and fully TTL compatible, both as an input and an output.

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}$	OE	OPERATION
L	L	H	Not recommended
L	L	L	Write (I/O = Z)
H	L	H	Read
X	H	X	Device disabled (I/O = Z)
H	X	L	Device disabled (I/O = Z)

H = High
L = Low
X = Irrelevant
Z = High Impedance (Off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Notes 1 and 2) . . . . . −0.5 to 7 V
Input voltage (any input) (see Notes 1 and 2) . . . . . −0.5 to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES:
1. Voltage values are with respect to the ground terminal.
2. For all combinations of inputs, the I/O lines may be shorted to V_{SS} or V_{CC} for a period not to exceed five milliseconds.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4036			TMS 4036-1			TMS 4036-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{SS}		0			0			0		V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 3)	−0.3		0.8	−0.3		0.8	−0.3		0.8	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Write pulse width, $t_{w(wr)}$	500			300			200			ns
Address setup time, $t_{su(ad)}$	450			300			200			ns
Chip-enable setup time, $t_{su(\overline{CE})}$	700			500			400			ns
Data setup time, $t_{su(da)}$	600			400			300			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Data hold time, $t_{h(da)}$	50			50			50			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 3: The albegraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

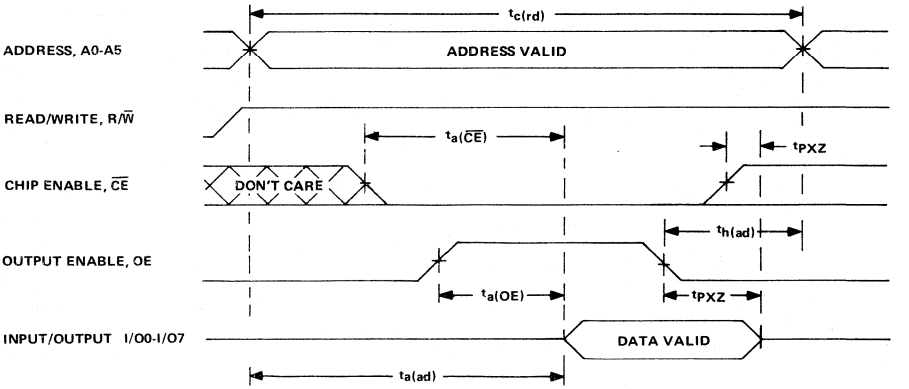
PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100 μA,	V_{CC} = 4.75 V	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 1.9 mA,	V_{CC} = 4.75 V		0.4	V
I_{IH}	High-level input current into address, R/$\overline{W}$, $\overline{CE}$, or OE	V_I = 5.25 V			10	μA
I_{OZH}	Off-state output current, high-level voltage applied at I/O terminal	V_O = 5.25 V, $\overline{CE}$ at 5.25 V	OE at 0 V,		10	μA
		V_O = 5.25 V, $\overline{CE}$ at 2.2 V	OE at 5.25 V,		10	
		V_O = 5.25 V, $\overline{CE}$ at 0 V	OE at 0.8 V,		10	
I_{OZL}	Off-state output current, low-level voltage applied at I/O terminal	V_O = 0 V, $\overline{CE}$ at 2.2 V	OE at 5.25 V,		−100	μA
		V_O = 0 V, $\overline{CE}$ at 0 V	OE at 0.8 V,		−100	
I_{CC}	Supply current from V_{CC}				85	mA
C_i	Input capacitance	f = 1 MHz,	T_A = 25°C		10	pF
$C_{i/o}$	I/O terminal capacitance	f = 1 MHz,	T_A = 25°C		20	pF

switching characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C

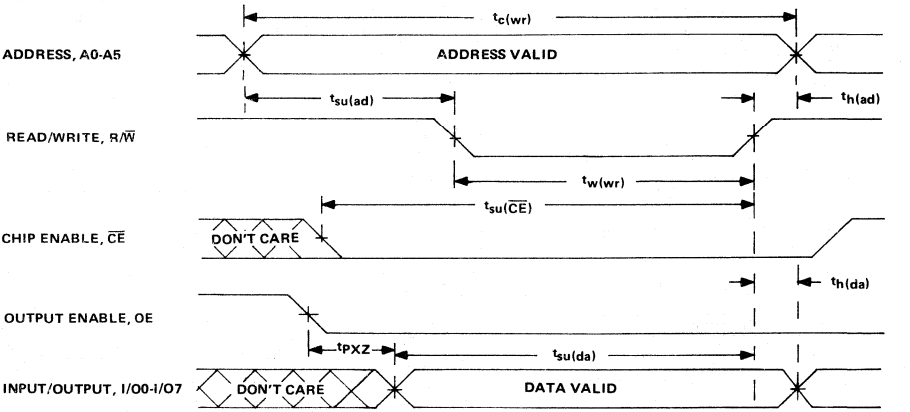
PARAMETER		TMS 4036			TMS 4036-1			TMS 4036-2			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(ad)}$	Access time from address			1000			650			450	ns
$t_{a(\overline{CE})}$	Access time from chip enable			200			190			180	ns
$t_{a(OE)}$	Access time from output enable			200			190			180	ns
t_{PXZ}	Output disable time from chip enable	0	60	200	0	60	200	0	60	200	ns
t_{PXZ}	Output disable time from output enable (see Note 4)	0	60	200	0	60	200	0	60	200	ns

NOTE 4: This parameter defines the delay for the I/O bus to enter the input mode.
†All typical values are at T_A = 25°C.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, t_r = t_f = 20 ns and all timing points are 50% points.

TMS 4039 JL, NL; TMS 4039-1 JL, NL; TMS 4039-2 JL, NL
256-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORIES

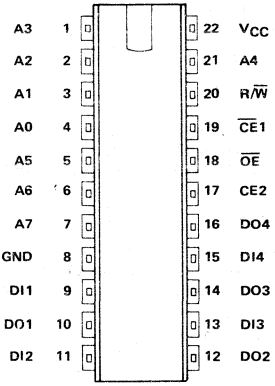
BULLETIN NO. DL-S 7512271, MAY 1975

- 256 x 4 Organization
- Static Operation (No Clocks, No Refresh)
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4039	1000 ns	1000 ns
TMS 4039-1	650 ns	650 ns
TMS 4039-2	450 ns	450 ns

- Input Interface
  - Fully Decoded
  - TTL-Compatible
  - Static Charge Protection
- Output Interface
  - Two Chip-Enable Inputs for OR-Tie Capability
  - Fan-out to 1 Series 74 TTL Load
  - 3-State Outputs and Output Enable Control for Common I/O Data Bus Systems
- Power Dissipation . . . 175 mW Typical
- Organized for Microprocessor-Based Systems
- Interchangeable with Intel 2101, 2101-2, and 2101-1, Respectively

22-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



description

This series of static random-access memories is organized as 256 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. All inputs and outputs are fully compatible with Series 74 TTL, including the single 5-volt power supply. The TMS 4039 series is manufactured using TI's reliable N-channel enhancement-type silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and output data is not inverted from data in.

The TMS 4039 series is offered in 22-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 400-mil centers. The series is characterized for operation from 0°C to 70°C.

operation

addresses (A0-A7)

The eight address inputs select one of 256 4-bit words. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable ($\overline{CE}$1 and CE2)

To enable the device, $\overline{CE}$1 must be low and CE2 must be high. The two chip-enable terminals can be driven from a common source with an inverter or either terminal can be hard wired to its enabled level. When the memory is disabled, data cannot be entered and the outputs are in the high-impedance state.

operation (continued)

read/write (R/$\overline{W}$)

The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

output enable ($\overline{OE}$)

The output enable must be low to read for when it is high the outputs are in the high-impedance state useful for OR-ties or common input/output operation. When the device is not used in the common-input/output configuration, the output enable terminal can be hard wired low.

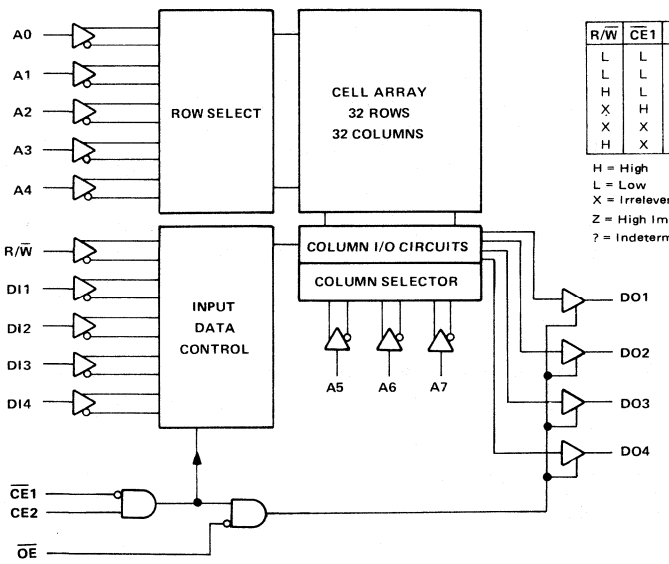
data in (DI1-DI4)

The DI inputs accept input data during a write operation. During a write cycle, data must be set up a minimum time before R/$\overline{W}$ goes to the read state (high) to ensure that correct data will enter the addressed memory cell. Also, input data must be held valid a minimum time after the rise of R/$\overline{W}$.

data out (DO1-DO4)

Data out is a three-state terminal controlled by $\overline{OE}$, $\overline{CE}$1, and CE2. To read data, $\overline{CE}$1 and $\overline{OE}$ must be low with CE2 high. When $\overline{OE}$ or $\overline{CE}$1 goes high or CE2 goes low, the output terminals are forced to the high-impedance state.

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}$1	CE2	$\overline{OE}$	OPERATION
L	L	H	L	Write (DO = ?)
L	L	H	H	Write (DO = Z)
H	L	H	L	Read
X	H	X	X	Device Disabled (DO = Z)
X	X	L	X	Device Disabled (DO = Z)
H	X	X	H	Device Disabled (DO = Z)

H = High
L = Low
X = Irrelevent
Z = High Impedance
? = Indeterminate

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . −0.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4039			TMS 4039-1			TMS 4039-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.5		0.65	−0.5		0.65	−0.5		0.65	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Write pulse width, $t_{w(wr)}$	800			450			300			ns
Address setup time, $t_{su(ad)}$	150			150			100			ns
Chip-enable setup time, $t_{su(CE)}$	900			550			400			ns
Data setup time, $t_{su(da)}$	700			400			280			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Data hold time, $t_{h(da)}$	100			100			100			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −150 μA,	V_{CC} = 4.75 V	2.2			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA,	V_{CC} = 5.25 V			0.45	V
I_I	Input current	V_I = 0 to 5.25 V				±10	μA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 4 V			15	μA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 0.45 V			−50	μA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25 V, I_O = 0 mA	T_A = 25°C			60	mA
			T_A = 0°C			70	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	T_A = 25°C,		4	8	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		8	12	pF

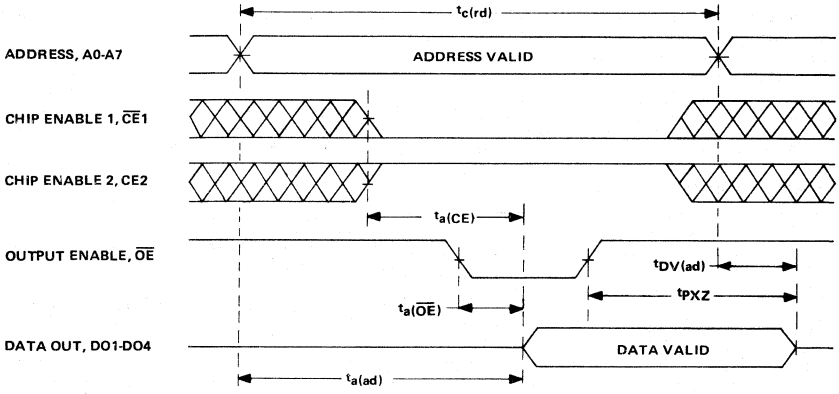
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load, C_L = 100 pF

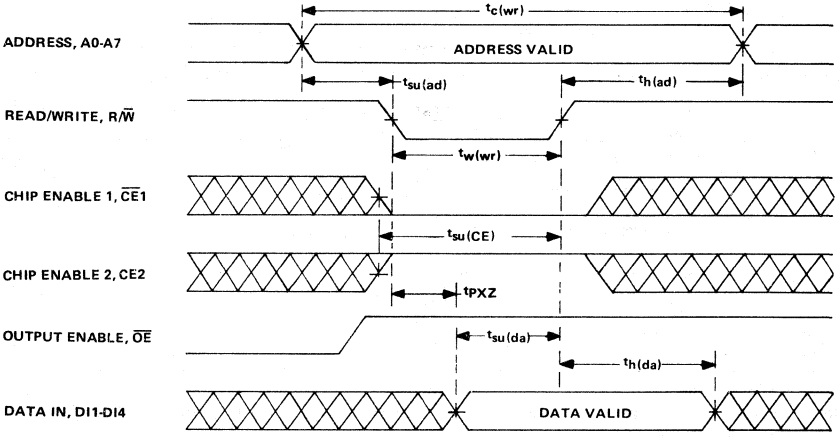
PARAMETER		TMS 4039		TMS 4039-1		TMS 4039-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(ad)}$	Access time from address		1000		650		450	ns
$t_{a(CE)}$	Access time from chip enable $\overline{CE}$1 or CE2		800		400		350	ns
$t_{a(\overline{OE})}$	Access time from output enable		700		350		300	ns
$t_{DV(ad)}$	Previous output data valid after address change	40		40		40		ns
t_{PXZ}	Output disable time from output enable (see Note 3)	0	200	0	150	0	150	ns

NOTE 3: With the outputs OR-tied to the inputs, this parameter defines the delay for the I/O bus to enter the input mode.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, $t_r = t_f$ = 20 ns and all timing points are 50% points.

TMS 4042 JL, NL; TMS 4042-1 JL, NL; TMS 4042-2 JL, NL
256-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORIES

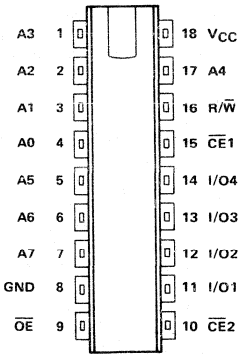
BULLETIN NO. DL-S 7512269, MAY 1975

- 256 x 4 Organization
- Common I/O
- 18-Pin Package
- Static Operation (No Clocks, No Refresh)
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4042	1000 ns	1000 ns
TMS 4042-1	650 ns	650 ns
TMS 4042-2	450 ns	450 ns

- Input Interface
  - Fully Decoded
  - TTL-Compatible
  - Static Charge Protection
- Output Interface
  - Two Chip-Enable Inputs for OR-Tie Capability
  - Fan-out to 1 Series 74 TTL Load
  - 3-State Outputs and Output Enable Control for Common I/O Data Bus Systems
- Power Dissipation . . . 175 mW Typical
- Organized for Microprocessor-Based Systems
- Interchangeable with Intel 2111, 2111-2, and 2111-1, Respectively

18-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



3

description

This series of static random-access memories is organized as 256 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. The use of common input/output terminals, controlled by the chip enable and output enable terminals, allows the use of an 18-pin package and saves board space in comparison to the TMS 4039. The common input/outputs are fully compatible with Series 74 TTL. The device requires a single 5-volt power supply. The TMS 4042 series is manufactured using TI's reliable N-channel enhancement-type silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and output data is not inverted from data in.

The TMS 4042 series is offered in 18-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. The series is characterized for operation from 0°C to 70°C.

operation

addresses (A0-A7)

The eight address inputs select one of 256 4-bit words. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable 1 and chip enable 2 ($\overline{CE}1$ and $\overline{CE}2$)

To enable the device, $\overline{CE}1$ and $\overline{CE}2$ must be low. The two chip-enable terminals can be driven from a common source or either terminal can be hard wired low. When the memory is disabled, data cannot be entered and the outputs are in the high-impedance state.

operation (continued)

read/write (R/$\overline{W}$)

The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

output enable ($\overline{OE}$)

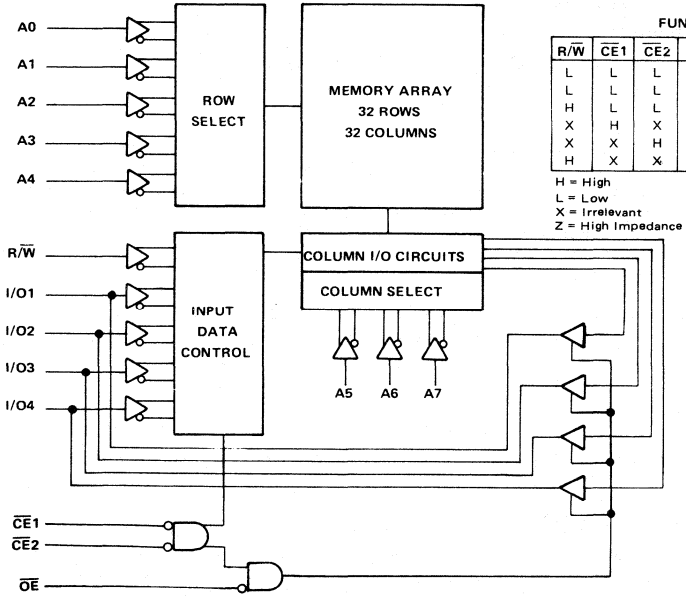
The output enable must be low to read for when it is high the outputs are in the high-impedance state.

input/output (I/O1-I/O4)

The common input/output terminals are used for both read and write operations. During a write cycle, data must be set up a minimum time before R/$\overline{W}$ goes to the read state (high) to ensure that correct data will enter the addressed memory cell. Also, input data must be held valid a minimum time after the rise of R/$\overline{W}$.

The output buffers are three-state and are controlled by $\overline{OE}$, $\overline{CE}1$, and $\overline{CE}2$. The input buffers are controlled by R/$\overline{W}$, $\overline{CE}1$, and $\overline{CE}2$. To read data, $\overline{CE}1$, $\overline{CE}2$, and $\overline{OE}$ must be low. If any one of these three inputs goes to the high level, the output terminals are forced to the high-impedance state. The common I/O terminals can be driven directly by Series 74 TTL and the buffers can drive Series 74 TTL circuits without external resistors.

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}1$	$\overline{CE}2$	$\overline{OE}$	OPERATION
L	L	L	L	Not recommended
L	L	L	H	Write (I/O = Z)
H	L	L	L	Read
X	H	X	X	Device Disabled (I/O = Z)
X	X	H	X	Device Disabled (I/O = Z)
H	X	X	H	Device Disabled (I/O = Z)

H = High
L = Low
X = Irrelevant
Z = High Impedance

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . −0.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4042			TMS 4042-1			TMS 4042-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.5		0.65	−0.5		0.65	−0.5		0.65	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Write pulse width, $t_{w(wr)}$	800			450			300			ns
Address setup time, $t_{su(ad)}$	150			150			100			ns
Chip enable setup time, $t_{su(\overline{CE})}$	900			550			400			ns
Data setup time, $t_{su(da)}$	700			400			280			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Data hold time, $t_{h(da)}$	100			100			100			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −150 μA,	V_{CC} = 4.75 V	2.2			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA,	V_{CC} = 5.25 V			0.45	V
I_I	Input current	V_I = 0 to 5.25 V				±10	μA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 4 V			15	μA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 0.45 V			−50	μA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25 V, I_O = 0 mA	T_A = 25°C			60	mA
			T_A = 0°C			70	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	T_A = 25°C,		4	8	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		10	15	pF

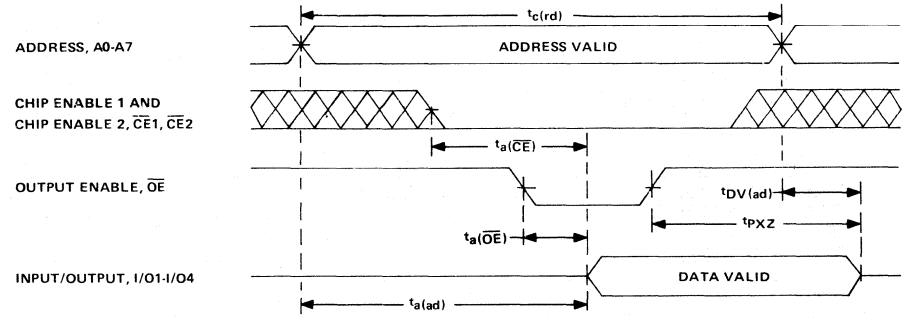
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load, C_L = 100 pF

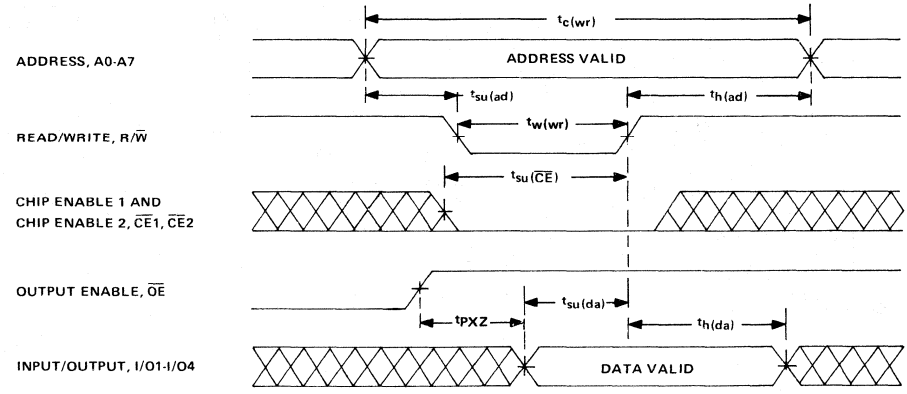
PARAMETER		TMS 4042		TMS 4042-1		TMS 4042-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(ad)}$	Access time from address		1000		650		450	ns
$t_{a(\overline{CE})}$	Access time from chip enable $\overline{CE}1$ or $\overline{CE}2$		800		400		350	ns
$t_{a(\overline{OE})}$	Access time from output enable		700		350		300	ns
$t_{DV(ad)}$	Previous output data valid after address change	40		40		40		ns
t_{PXZ}	Output disable time from output enable (see Note 3)	0	200	0	150	0	150	ns

NOTE 3: This parameter defines the delay for the I/O bus to enter the input mode.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, $t_r = t_f$ = 20 ns and all timing points are 50% points.

TEXAS INSTRUMENTS

TMS 4043 JL, NL; TMS 4043-1 JL, NL; TMS 4043-2 JL, NL
256-WORD BY 4-BIT STATIC RANDOM-ACCESS MEMORIES

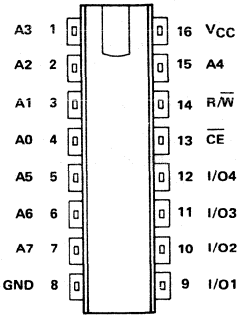
BULLETIN NO. DL-S 7512270, MAY 1975

- 256 x 4 Organization
- Common I/O
- 16-Pin Package
- Static Operation (No Clocks, No Refresh)
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4043	1000 ns	1000 ns
TMS 4043-1	650 ns	650 ns
TMS 4043-2	450 ns	450 ns

- Input Interface
  - Fully Decoded
  - TTL-Compatible
  - Static Charge Protection
- Output Interface
  - Chip-Enable Input and 3-State Outputs for OR-Tie Capability in Common I/O Data Bus Systems
  - Fan-out to 1 Series 74 TTL Load
- Power Dissipation . . . 175 mW Typical
- Organized for Microprocessor-Based Systems
- TMS 4043 and TMS 4043-1 Are Interchangeable with Intel 2112 and 2112-2, Respectively

16-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

This series of static random-access memories is organized as 256 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. The use of common input/output terminals, controlled by the chip enable and read/write terminals, allows the use of a 16-pin package and saves board space in comparison to the TMS 4039 or TMS 4042. The common input/outputs are fully compatible with Series 74 TTL. The device requires a single 5-volt power supply. The TMS 4043 series is manufactured using TI's reliable N-channel enhancement-type silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and output data is not inverted from data in.

The TMS 4043 series is offered in 16-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. The series is characterized for operation from 0°C to 70°C.

operation

addresses (A0-A7)

The eight address inputs select one of 256 4-bit words. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable ($\overline{CE}$)

To enable the device, $\overline{CE}$ must be low. When the memory is disabled, data cannot be entered and the outputs are in the high-impedance state.

operation (continued)

read/write (R/$\overline{W}$)

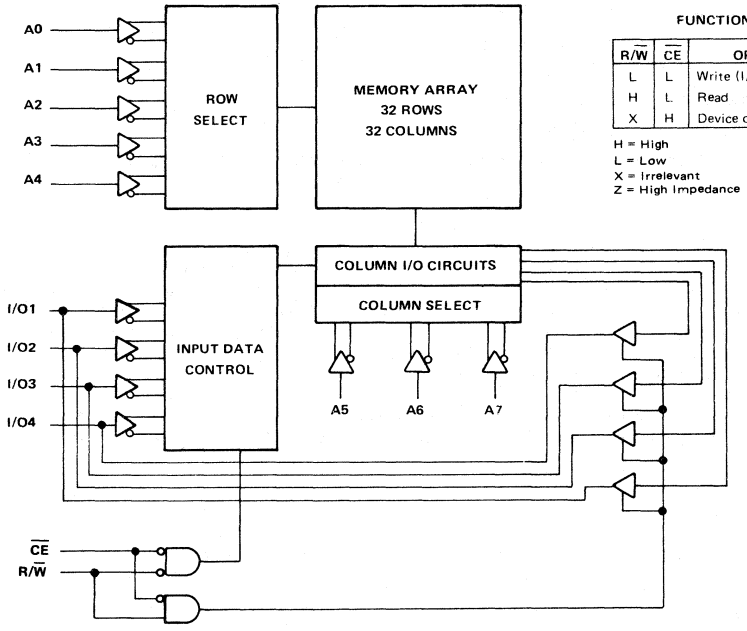
The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

input/output (I/O1-I/O4)

The common input/output terminals are used for both read and write operations. During a write cycle, data must be set up a minimum time before R/$\overline{W}$ goes to the read state (high) to ensure that correct data will enter the addressed memory cell. Also, input data must be held valid a minimum time after the rise of R/$\overline{W}$.

The output buffers are three-state and they are controlled by $\overline{CE}$ and R/$\overline{W}$. If $\overline{CE}$ goes high or R/$\overline{W}$ goes low, the output terminals are forced to the high-impedance state. The input buffers are also controlled by $\overline{CE}$ and R/$\overline{W}$. To read data, $\overline{CE}$ must be low and R/$\overline{W}$ high. The common I/O terminals can be driven directly by Series 74 TTL and the buffers can drive Series 74 TTL circuits without external resistors.

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}$	OPERATION
L	L	Write (I/O = Z)
H	L	Read
X	H	Device disabled (I/O = Z)

H = High
L = Low
X = Irrelevant
Z = High Impedance

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . −0.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4043			TMS 4043-1			TMS 4043-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.5		0.65	−0.5		0.65	−0.5		0.65	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Address setup time, $t_{su(ad)}$	150			100			50			ns
Chip-enable setup time, $t_{su(\overline{CE})}$	0			0			0			ns
Data setup time, $t_{su(da)}$	600			300			150			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Chip-enable hold time, $t_{h(\overline{CE})}$	0			0			0			ns
Data hold time, $t_{h(da)}$	100			50			50			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −150 μA,	V_{CC} = 4.75 V	2.2			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA,	V_{CC} = 5.25 V			0.45	V
I_I	Input current	V_I = 0 to 5.25 V				±10	μA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 4 V			15	μA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 0.45 V			−50	μA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25 V, I_O = 0 mA	T_A = 25°C			60	mA
			T_A = 0°C			70	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	T_A = 25°C,		4	8	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		10	15	pF

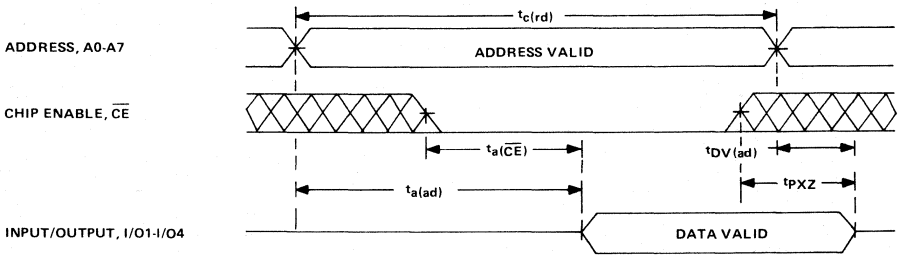
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load, C_L = 100 pF

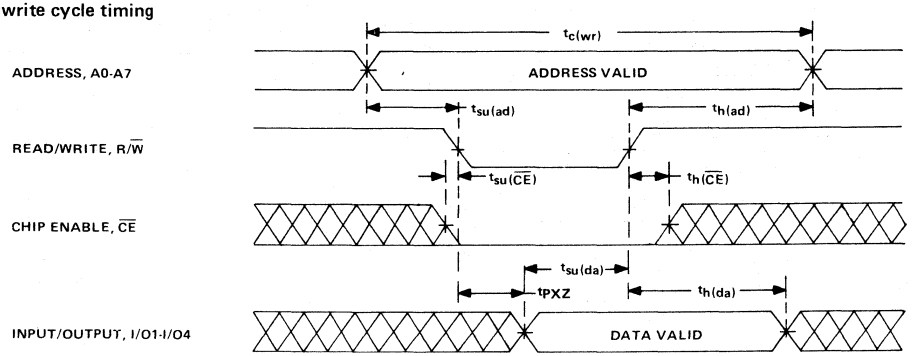
PARAMETER		TMS 4043		TMS 4043-1		TMS 4043-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(ad)}$	Access time from address		1000		650		450	ns
$t_{a(\overline{CE})}$	Access time from chip enable		800		500		350	ns
$t_{DV(ad)}$	Previous output data valid after address change	40		40		40		ns
t_{PXZ}	Output disable time from chip enable (see Note 3)	0	200	0	150	0	150	ns
t_{PXZ}	Output disable time from read/write (see Note 3)		200		200		200	ns

NOTE 3: This parameter defines the delay for the I/O bus to enter the input mode.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, $t_r = t_f$ = 20 ns and all timing points are 50% points.

TMS 4050 JL, NL; TMS 4050-1 JL, NL; TMS 4050-2 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

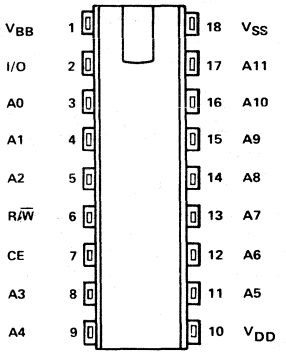
BULLETIN NO. DL-S 7512242, FEBRUARY 1975—REVISED MAY 1975

- 4096 x 1 Organization
- 18-Pin 300-Mil Package Configuration
- Multiplexed Data Input/Output
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4050	300 ns	470 ns	730 ns
TMS 4050-1	250 ns	430 ns	660 ns
TMS 4050-2	200 ns	400 ns	600 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed)
- Registers for Addresses Provided on Chip
- Open-Drain Output Buffer
- Single Low-Capacitance Clock
- Low-Power Dissipation
  - 420 mW Operating (Typical)
  - 0.1 mW Standby (Typical)
- N-Channel Silicon-Gate Technology

18-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



description

The TMS 4050 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Three performance options are offered: 300 ns access for the TMS 4050, 250 ns access for the TMS 4050-1, and 200 ns for TMS 4050-2. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

All inputs except the chip enable are fully TTL-compatible and require no pull-up resistors. The input buffers allow a minimum 200 mV noise margin when driven by a series 74 TTL device. The TTL-compatible open-drain buffer is guaranteed to drive 1 series 74 TTL gate. The low capacitance of the address and control inputs precludes the need for specialized drivers. The TMS 4050 series uses only one clock (chip enable) to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers. The data input and output are multiplexed to facilitate compatibility with a common bus system. A 12 line address is available, which minimizes external control logic and optimizes system performance.

The typical power dissipation of these RAM's is 420 mW active and 0.1 mW standby. To retain data only 6 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4050 series is offered in both 18-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting hole rows on 300-mil centers.

operation

chip enable (CE)

A single external clock input is required. All read, write, and read, modify write operations take place when the chip enable input is high. When the chip enable is low, the memory is in the low-power standby mode and is not selected. No read/write operations can take place during the standby mode because the chip is deselected and is automatically precharging.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

operation (continued)

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected and the data output is disabled when the write mode is selected.

address (A0–A11)

All addresses must be stable on or before the rising edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data input/output (I/O)

Data input and output are multiplexed on a common input/output terminal, which is controlled by the R/$\overline{W}$ input. Data is written during a write or read, modify write cycle while the chip enable is high. The I/O terminal requires connection to an external pull-up resistor since the output buffer has an open-drain configuration. The open-drain output buffer provides direct TTL sink compatibility with a fan-out of one Series 74 TTL gate. A low logic level results from conduction in the open-drain output buffer while a high level occurs with the buffer in its high-impedance state. Data written into the memory is read out in its true form.

refresh

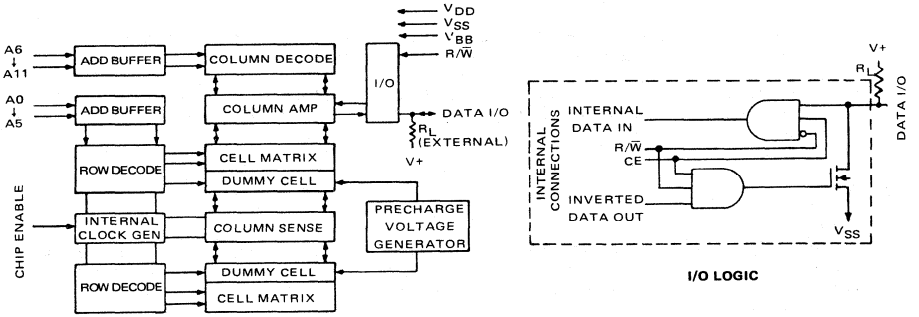
Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses (A0 through A5) every 2 milliseconds or less. Addressing any row refreshes all 64 bits in that row. The column addresses (A6 through A11) can be indeterminate during refresh.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 20 V
All input voltages (see Note 1)	−0.3 to 20 V
Chip-enable voltage (see Note 1)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

functional block diagram



I/O LOGIC

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.5	V
High-level chip enable input voltage, $V_{IH(CE)}$	V_{DD} −0.6		V_{DD}+1	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note 2)	−0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$ (see Note 2)	−1		0.6	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	t_a = guaranteed maximum access time, R_L = 2.2 kΩ to 5.5 V, C_L = 50 pF, Load = 1 Series 74 TTL gate		2.4			V
V_{OL}	Low-level output voltage			V_{SS}		0.4	V
I_{OL}	Low-level output current	t_a = guaranteed maximum access time, C_L = 50 pF, V_{OL} = 0.4 V		5			mA
I_I	Input current (all inputs including I/O except chip enable)	V_I = −0.6 to 5.5 V				10	μA
$I_{I(CE)}$	Chip enable input current	V_I = −1 to 13.2 V				10	μA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 13.2 V	TMS4050		35	60	mA
			TMS4050-1				
			TMS4050-2		35	70	
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V			10	200	μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle timing	TMS 4050		32		mA
			TMS 4050-1		35		
			TMS 4050-2		38		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle		TMS 4050		32		mA
			TMS 4050-1		35		
			TMS 4050-2		38		
I_{BB}	Supply current from V_{BB}	V_{BB} = −5.5 V, V_{SS} = 0 V, V_{DD} = ↑2.6 V,			5	100	μA

† All typical values are at T_A = 25°C.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 12 V		24	28	pF
		$V_{I(CE)}$ = 0 V		29	33	
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
$C_{(I/O)}$	I/O terminal capacitance			7	9	pF

† All typical values are at T_A = 25°C.

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4050		TMS 4050-1		TMS 4050-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(rd)}$	Read setup time	0↑		0↑		0↑		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

read cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4050		TMS 4050-1		TMS 4050-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable*		280		230		180	ns
$t_{a(ad)}$	Access time from addresses†		300		250		200	ns
t_{PLH}	Propagation delay time, low-to-high level output from chip enable*	40		40		40		ns

*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate.
†Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate, $t_{r(CE)}$ = 20 ns.

write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

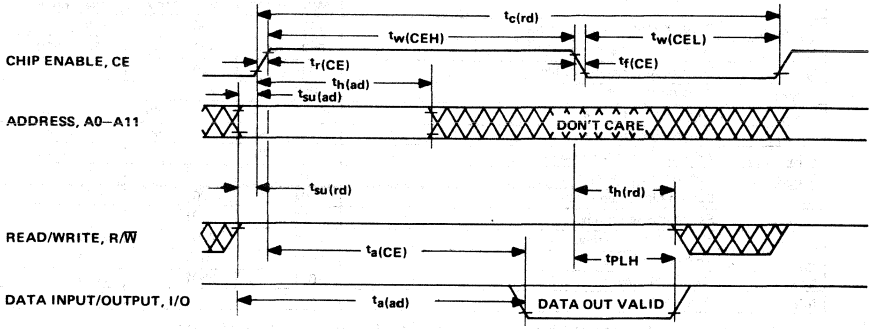
PARAMETER		TMS 4050		TMS 4050-1		TMS 4050-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time*	0		0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{d(CEH\text{-}wr)}$	Chip-enable-high-to-write delay time†		40↑		40↑		40↑	ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

*If $R/\overline{W}$ is low before CE goes high, then I/O (data in) must be valid when CE goes high.

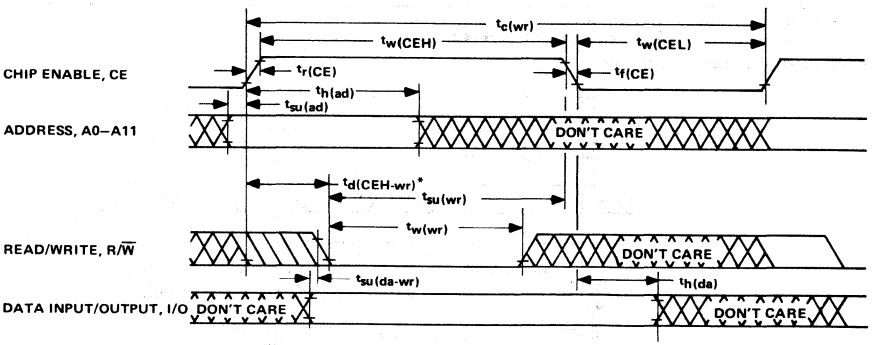
†The write pulse must go low at least $t_{su(wr)}$ minimum before CE goes low. If $R/\overline{W}$ remains high more than $t_{d(CEH\text{-}wr)}$ maximum (40 ns) after CE goes high, the data-in driver must be disabled until $R/\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices (see comments on Region 1 under read, modify write timing diagram).

read or refresh cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(\overline{CE})}$ and $t_{f(\overline{CE})}$ are equal to 20 ns.

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

*The write pulse must go low at least $t_{su(wr)}$ minimum before $\overline{CE}$ goes high. If R/$\overline{W}$ remains high more than $t_{d(\overline{CE}L\text{-}wr)}$ maximum (60 ns) after $\overline{CE}$ goes low, the data-in driver must be disabled until R/$\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices. During $t_{d(CEH\text{-}wr)}$, R/$\overline{W}$ is permitted to change from high to low only.

read, modify write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4050		TMS 4050-1		TMS 4050-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(RMW)}$	Read, modify write cycle time†	730		660		600		ns
$t_{w(CEH)}$	Pulse width, chip enable high†	560	4000	490	4000	430	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{d(wr\text{-}daL)}$	Write to data-in-low delay time		20		20		20	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(daH)}$	Data-in-high setup time	240↓		220↓		210↓		ns
$t_{su(rd)}$	Read-pulse setup time	0↑		0↑		0↑		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	300↑		250↑		200↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

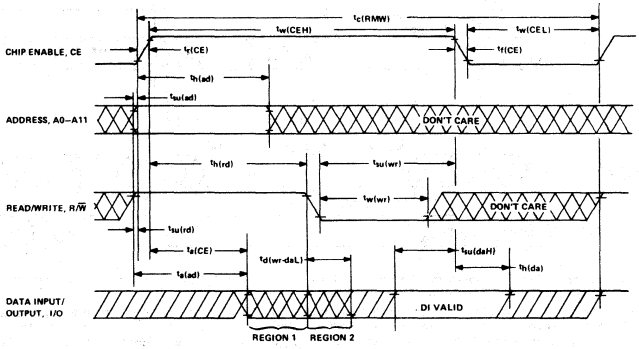
↑↓ The arrow indicates the edge of the chip-enable pulse for reference: ↑ for the rising edge; ↓ for the falling edge.
†Test conditions: $t_{f(rd)}$ = 20 ns.

read, modify write cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4050		TMS 4050-1		TMS 4050-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable*		280		230		180	ns
$t_{a(ad)}$	Access Time from addresses†		300		250		200	ns

*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ, Load = 1 Series 74 TTL gate.
†Test conditions: C_L = 50 pF, R_L = 2.2 kΩ, Load = 1 Series 74 TTL gate. $t_{r(CE)}$ = 20 ns.

read, modify write cycle timing



REGION 1 – In region 1, data-out is valid until the I/O terminal is forced high or low by the data-in driver. A transition from low to high is permissible but additional power to overcome the output buffer will be required. A transition from high to low is permitted without power penalty.

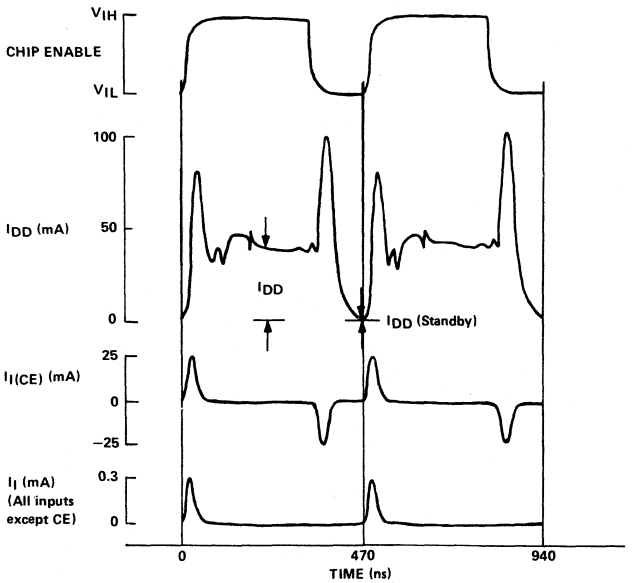
REGION 2 – In region 2 a single transition is permitted. It is NOT a true "Don't Care" region. If a low is to be written it must be valid by the end of region 2.

NOTE: For the chip enable input high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(CE)}$ and $t_{f(CE)}$ are equal to 20 ns.

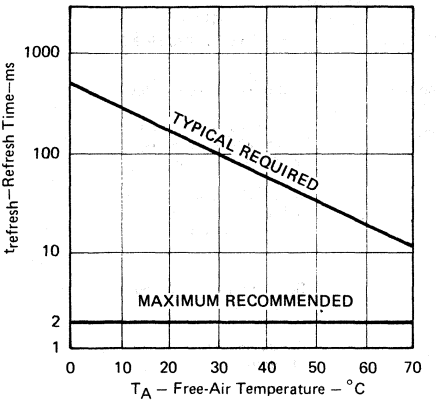
timing diagram conventions

TIMING DIAGRAM SYMBOL	MEANING	
	INPUT FORCING FUNCTIONS	OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

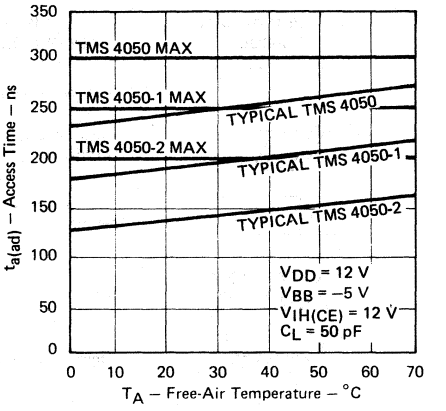
TYPICAL WAVEFORMS



REFRESH TIME vs TEMPERATURE



ACCESS TIMES vs TEMPERATURE



TEXAS INSTRUMENTS

TMS 4051 JL, NL; TMS 4051-1 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

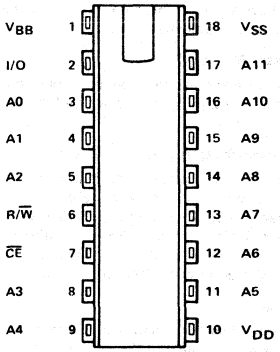
BULLETIN NO. DL-S 7512256, MAY 1975

- 4096 x 1 Organization
- 18-Pin 300-Mil Package Configuration
- Single Low-Capacitance TTL-Compatible Clock
- Multiplexed Data Input/Output
- 2 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4051	300 ns	470 ns	730 ns
TMS 4051-1	250 ns	430 ns	660 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed Except with $\overline{CE}$)
- Registers for Addresses Provided on Chip
- Open-Drain Output Buffer
- Low-Power Dissipation
  - 460 mW Operating (Typical)
  - 60 mW Standby (Typical)
- N-Channel Silicon-Gate Technology

18-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



description

The TMS 4051 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Two performance options are offered: 300 ns access for the TMS 4051 and 250 ns access for the TMS 4051-1. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

The address, data input/output, and read/write inputs can be driven directly from Series 74 TTL circuits. A 200-mV noise margin is guaranteed in this configuration, which eliminates the need for specialized drivers. The chip-enable input is TTL-compatible and can interface with a Series 74 TTL circuit as long as a pull-up resistor to V_{CC} is employed in order to provide a high-level input voltage of 3 V minimum. The data input and output are multiplexed to facilitate compatibility with a common bus system. A 12-line address is available, which minimizes external control logic and optimizes system performance.

The typical power dissipation of these RAM's is 460 mW active and 60 mW standby. To retain data only 70 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4051 series is offered in both 18-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil centers.

operation

chip enable ($\overline{CE}$)

A single external clock input is required. All read, write, and read, modify write operations take place when the chip enable input is low. When the chip enable is high, the memory is in the low-power standby mode and is not selected. No read/write operations can take place during the standby mode because the chip is deselected and is automatically precharging. The $\overline{CE}$ input can be driven by a standard TTL circuit with a pull-up resistor.

operation (continued)

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected and the data output is disabled when the write mode is selected.

address (A0–A11)

All addresses must be stable on or before the falling edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data input/output (I/O)

Data input and output are multiplexed on a common input/output terminal, which is controlled by the R/$\overline{W}$ input. Data is written during a write or read, modify write cycle while the chip enable is low. The I/O terminal requires connection to an external pull-up resistor since the output buffer has an open-drain configuration. The open-drain output buffer provides direct TTL sink compatibility with a fan-out of one Series 74 TTL gate. A low logic level results from conduction in the open-drain output buffer while a high level occurs with the buffer in its high-impedance state. Data written into the memory is read out in its true form.

refresh

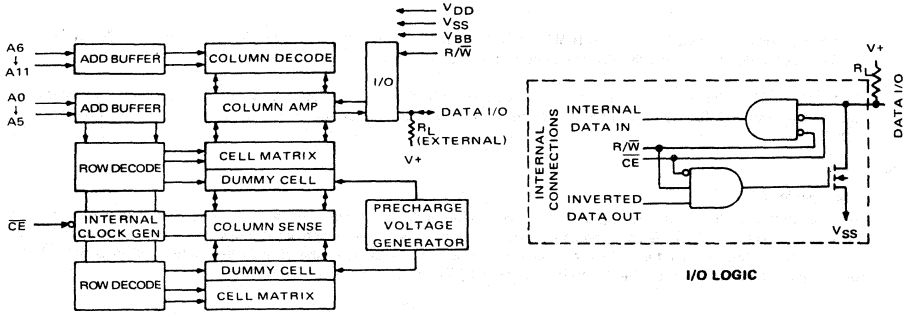
Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses (A0 through A5) every 2 milliseconds or less. Addressing any row refreshes all 64 bits in that row. The column addresses (A6 through A11) can be indeterminate during refresh.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 20 V
All input voltages (see Note 1)	−0.3 to 20 V
Chip-enable voltage (see Note 1)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

functional block diagram



I/O LOGIC

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.5	V
High-level chip enable input voltage, $V_{IH(\overline{CE})}$	3		5.5	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note 2)	−0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(\overline{CE})}$ (see Note 2)	−0.6		0.6	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	t_a = guaranteed maximum access time, R_L = 2.2 kΩ to 5.5 V, C_L = 50 pF, Load = 1 Series 74 TTL gate		2.4			V
V_{OL}	Low-level output voltage			V_{SS}		0.4	V
I_{OL}	Low-level output current	t_a = guaranteed maximum access time, C_L = 50 pF, V_{OL} = 0.4 V		5			mA
I_I	Input current (all inputs including I/O except chip enable)	V_I = −0.6 to 5.5 V				10	μA
$I_{I(\overline{CE})}$	Chip enable input current	V_I = −0.6 to 5.5 V				10	μA
I_{DD}	Supply current from V_{DD}	$V_{IL(\overline{CE})}$ = 0.6 V			37	70	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IH(\overline{CE})}$ = 3.5 V			5	8	mA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle timing	TMS 4051		45		mA
			TMS 4051-1		47		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle		TMS 4051		50		mA
			TMS 4051-1		54		
I_{BB}	Supply current from V_{BB}	V_{BB} = −5.5 V, V_{SS} = 0 V	V_{DD} = 12.6 V,		5	100	μA

†All typical values are at T_A = 25°C.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −5 V, $V_{I(\overline{CE})}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs		5	7	pF
$C_{i(\overline{CE})}$	Input capacitance clock input		5	7	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input		5	7	pF
$C_{(I/O)}$	I/O terminal capacitance		7	9	pF

†All typical values are at T_A = 25°C.

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	470		430		ns
$t_{w(\overline{CE}H)}$	Pulse width, chip enable high	130		130		ns
$t_{w(\overline{CE}L)}$	Pulse width, chip enable low	300	4000	260	4000	ns
$t_{r(\overline{CE})}$	Chip-enable rise time		40		40	ns
$t_{f(\overline{CE})}$	Chip-enable fall time		40		40	ns
$t_{su(ad)}$	Address setup time	0↓		0↓		ns
$t_{su(rd)}$	Read setup time	0↓		0↓		ns
$t_{h(ad)}$	Address hold time	180↓		165↓		ns
$t_{h(rd)}$	Read hold time	80↑		80↑		

↑↓The arrow indicates the edge of the chip-enable pulse used for reference: ↑for the rising edge, ↓for the falling edge.

read cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		TYP†	MAX	TYP†	MAX	
$t_{a(\overline{CE})}$	Access time from chip enable‡		280		230	ns
$t_{a(ad)}$	Access time from addresses*		300		250	ns
t_{PLH}	Propagation delay time, low-to-high level output from chip enable‡	60		60		ns

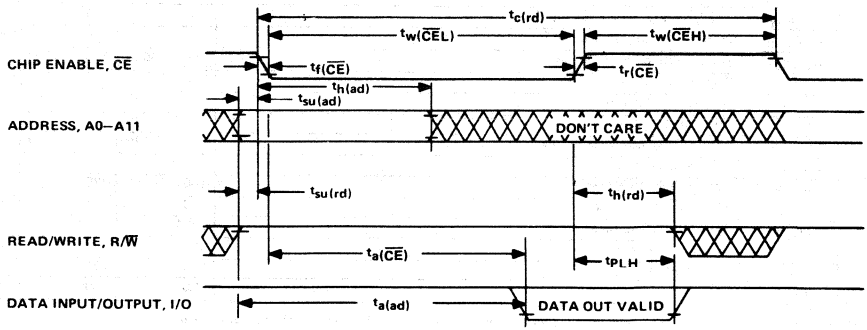
†All typical values are at T_A = 25°C.
‡Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate.
*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate, $t_{f(\overline{CE})}$ = 20 ns.

write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	470		430		ns
$t_{w(\overline{CE}H)}$	Pulse width, chip enable high	130		130		ns
$t_{w(\overline{CE}L)}$	Pulse width, chip enable low	300	4000	260	4000	ns
$t_{w(wr)}$	Write pulse width	200		190		ns
$t_{r(\overline{CE})}$	Chip-enable rise time		40		40	ns
$t_{f(\overline{CE})}$	Chip-enable fall time		40		40	ns
$t_{su(ad)}$	Address setup time	0↓		0↓		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time*	0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↑		220↑		ns
$t_{d(\overline{CE}L\text{-}wr)}$	Chip-enable-low-to-write delay time†		60↓		60↓	ns
$t_{h(ad)}$	Address hold time	180↓		165↓		ns
$t_{h(da)}$	Data hold time	80↑		80↑		ns

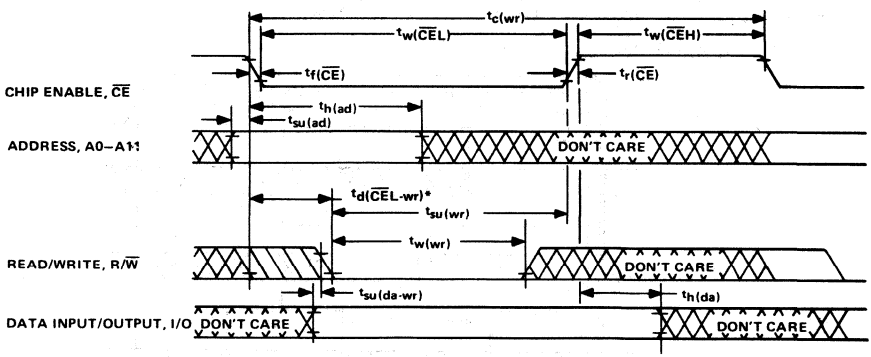
↑↓The arrow indicates the edge of the chip-enable pulse used for reference: ↑for the rising edge, ↓for the falling edge.
*If R/$\overline{W}$ is low before $\overline{CE}$ goes low, then I/O (data in) must be valid when $\overline{CE}$ goes low.
†The write pulse must go low at least $t_{su(wr)}$ minimum before $\overline{CE}$ goes high. If R/$\overline{W}$ remains high more than $t_{d(\overline{CE}L\text{-}wr)}$ maximum (60 ns) after $\overline{CE}$ goes low, the data-in driver must be disabled until R/$\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices (see comments on Region 1 under read, modify write timing diagram).

read or refresh cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(\overline{CE})}$ and $t_{f(\overline{CE})}$ are equal to 20 ns.

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 3.0 V (high) and 1.0 V (low). Other timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
*The write pulse must go low at least $t_{su(wr)}$ minimum before $\overline{CE}$ goes high. If R/$\overline{W}$ remains high more than $t_{d(\overline{CE}L\text{-}wr)}$ maximum (60 ns) after $\overline{CE}$ goes low, the data-in driver must be disabled until R/$\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices. During $t_{d(\overline{CE}L\text{-}wr)}$, R/$\overline{W}$ is permitted to change from high to low only.

read, modify write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(RMW)}$	Read, modify write cycle time†	730		660		ns
$t_{w(\overline{CE}H)}$	Pulse width, chip enable high†	130		130		ns
$t_{w(\overline{CE}L)}$	Pulse width, chip enable low	560	4000	490	4000	ns
$t_{w(wr)}$	Write pulse width	200		190		ns
$t_{r(\overline{CE})}$	Chip-enable rise time		40		40	ns
$t_{f(\overline{CE})}$	Chip-enable fall time		40		40	ns
$t_{d(wr\text{-}daL)}$	Write to data-in-low delay time		20		20	ns
$t_{su(ad)}$	Address setup time	0↓		0↓		ns
$t_{su(daH)}$	Data-in-high setup time	240↑		220↑		ns
$t_{su(rd)}$	Read-pulse setup time	0↓		0↓		ns
$t_{su(wr)}$	Write-pulse setup time	240↑		220↑		ns
$t_{h(ad)}$	Address hold time	180↓		165↓		ns
$t_{h(rd)}$	Read hold time	320↓		270↓		ns
$t_{h(da)}$	Data hold time	80↑		80↑		ns

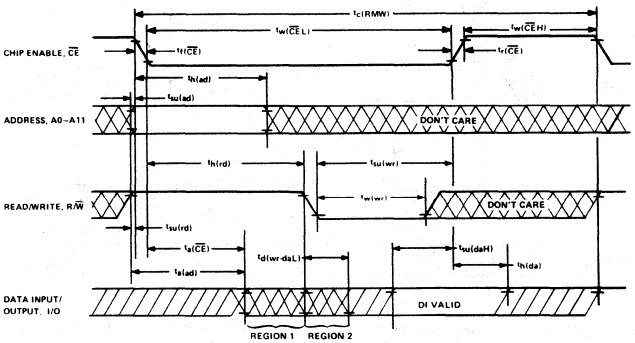
↑↓The arrow indicates the edge of the chip-enable pulse for reference: ↑for the rising edge; ↓for the falling edge.
†Test conditions: $t_{f(rd)}$ = 20 ns.

read, modify write cycle swithcing characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4051		TMS 4051-1		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(\overline{CE})}$	Access time from chip enable*		280		230	ns
$t_{a(ad)}$	Access time from addresses†		300		250	ns

*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ, Load = 1 Series 74 TTL gate.
†Test conditions: C_L = 50 pF, R_L = 2 2 kΩ, Load = 1 Series 74 TTL gate. $t_{f(\overline{CE})}$ = 20 ns.

read, modify write cycle timing



REGION 1 — In region 1, data-out is valid until the I/O terminal is forced high or low by the data-in driver. A transition from low to high is permissible but additional power to overcome the output buffer will be required. A transition from high to low is permitted without power penalty.

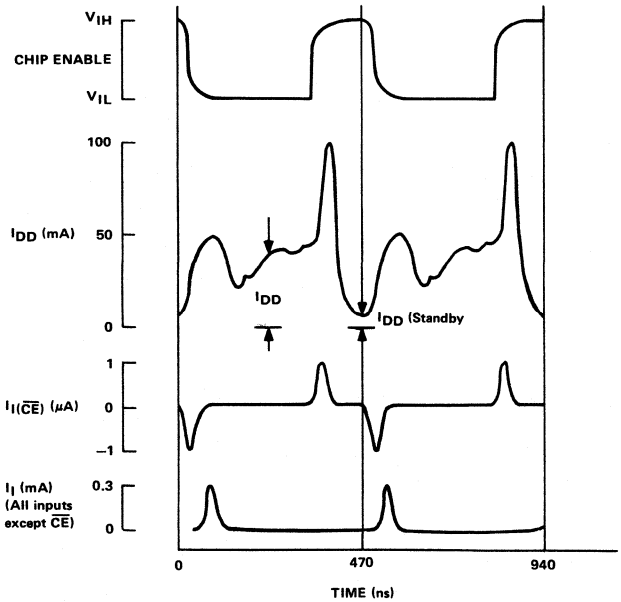
REGION 2 — In region 2 a single transition is permitted. It is NOT a true "Don't Care" region. If a low is to be written it must be valid by the end of region 2.

NOTE: For the chip enable input high and low timing points are 3.0 V (high) and 1.0 V (low). Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).
For minimum cycle, $t_{r(\overline{CE})}$ and $t_{f(\overline{CE})}$ are equal to 20 ns.

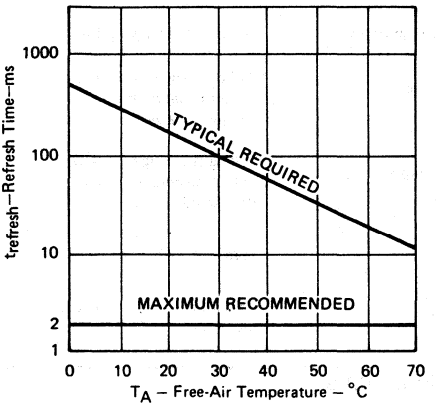
timing diagram conventions

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

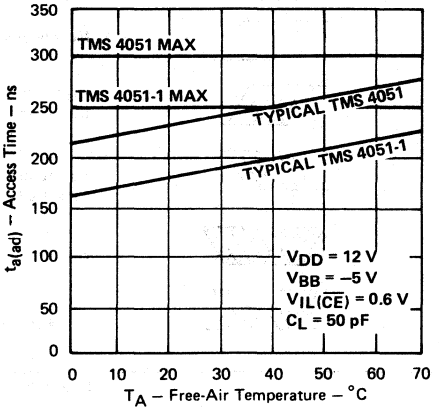
TYPICAL WAVEFORMS



REFRESH TIME vs TEMPERATURE



ACCESS TIMES vs TEMPERATURE



TMS 4060 JL, NL; TMS 4060-1 JL, NL; TMS 4060-2 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

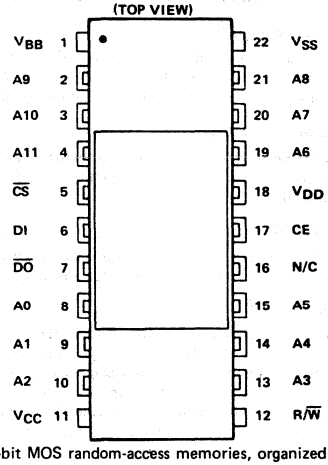
BULLETIN NO. DL-S 7512241, FEBRUARY 1975

- 4096 x 1 Organization
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4060	300 ns	470 ns	710 ns
TMS 4060-1	250 ns	430 ns	640 ns
TMS 4060-2	200 ns	400 ns	580 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed)
- Low Power Dissipation
  - 400 mW Operating (Typical)
  - 0.2 mW Standby (Typical)
- Single Low-Capacitance Clock
- N-Channel Silicon-Gate Technology
- 22-Pin 400-Mil Dual-in-Line Package

22-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 4060 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Three performance options are offered: 300 ns access for the TMS 4060, 250 ns access for the TMS 4060-1, and 200 ns for TMS 4060-2. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

All inputs except the chip enable are fully TTL-compatible and require no pull-up resistors. The low capacitance of the address and control inputs precludes the need for specialized drivers. When driven by a Series 74 device, the guaranteed dc input noise immunity is 200 mV. The TTL-compatible buffer is guaranteed to drive two Series 74 TTL gates. The TMS 4060 series uses only one clock (chip enable) to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers.

The typical power dissipation of these RAM's is 400 mW active and 0.3 mW standby. To retain data only 6 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4060 series is offered in both 22-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guaranteed for operation from 0°C to 70°C. These packages are designed for insertion in mounting-hole rows on 0.400-mil centers.

operation

chip select ($\overline{CS}$)

The chip-select terminal, which can be driven from standard TTL circuits without an external pull-up resistor, affects the data-in, data-out and read/write inputs. The data input and data output terminals are enabled when chip select is low. Therefore, the read, write, and read, modify write operations are performed only when chip select is low. If the chip is to be selected for a given cycle, the chip-select input must be low on or before the rising edge of the chip enable. If the chip is not to be selected for a given cycle, chip select must be held high as long as chip enable is high. A register for the chip-select input is provided on the chip to reduce overhead and simplify system design.

chip enable (CE)

A single external clock input is required. All read, write, and read, modify write operations take place when the chip enable input is high. When the chip enable is low, the memory is in the low-power standby mode. No read/write operations can take place because the chip is automatically precharging.

operation (continued)

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected.

address (A0–A11)

All addresses must be stable on or before the rising edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data-in (DI)

Data is written during a write or read, modify write cycle while the chip enable is high. The data-in terminal can be driven from standard TTL circuits without a pull-up resistor. There is no register on the data-in terminal.

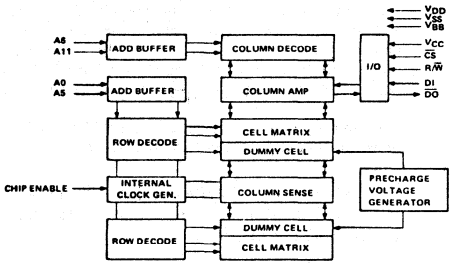
data-out ($\overline{DO}$)

The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates. The output is in the high-impedance (floating) state when the chip enable is low. It remains in the high-impedance state if the chip-select input is high when chip enable goes high and provided that chip select remains high as long as chip enable is high. If the chip select is set up low prior to the rise of chip enable and held low an interval after that rise, the output will be enabled as long as chip enable stays high regardless of subsequent changes in the level of chip select. A data-valid mode is always preceded by a low output state. Data-out is inverted from data-in.

refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs, A0 through A5 (pins 8, 9, 10, 13, 14, 15), or by addressing every row within any 2-millisecond period. Addressing any row refreshes all 64 bits in that row. The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, then chip select must be high. The column addresses (A6 through A11) can be indeterminate during refresh.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note)	−0.3 to 20 V
Supply voltage, V_{DD} (see Note)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note)	−0.3 to 20 V
All input voltages (see Note)	−0.3 to 20 V
Chip-enable voltage (see Note)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

recommended operating conditions (see Note)

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.25	V
High-level chip enable input voltage, $V_{IH(CE)}$	V_{DD} −0.6		V_{DD} +1.0	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note)	−0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$ (see Note)	−1		0.6	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTE: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −2 mA		2.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_O = 3.2 mA		V_{SS}		0.4	V
I_I	Input current (all inputs except chip enable)	V_I = 0 to 5.25 V				10	μA
$I_{I(CE)}$	Chip enable input current	V_I = 0 to 13.2 V				2	μA
I_{OZ}	High-impedance-state (off-state) output current	V_O = 0 to 5.25 V				10	μA
I_{CC}	Supply current from V_{CC}	2 Series 74 TTL loads				1	mA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 12.6 V			30	60	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V			20	200	μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle time	TMS 4060		32		mA
			TMS 4060-1		35		
			TMS 4060-2		38		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle		TMS 4060		32		mA
			TMS 4060-1		35		
			TMS 4060-2		38		
I_{BB}	Supply current from V_{BB}	V_{BB} = −5.5 V, V_{DD} = 12.6 V,	V_{CC} = 5.25 V, V_{SS} = 0 V		−5	−100	μA

†All typical values are at T_A = 25°C.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −5 V, V_{CC} = 5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 10.8 V		18	22	pF
		$V_{I(CE)}$ = −1.0 V		23	27	
$C_{i(\overline{CS})}$	Input capacitance chip select input			4	6	pF
$C_{i(data)}$	Input capacitance data input			4	6	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
C_o	Output capacitance			5	7	pF

†All typical values are at T_A = 25°C.

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(rd)}$	Read setup time	0↑		0↑		0↑		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

read cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable†		280		230		180	ns
$t_{a(ad)}$	Access time from address†		300		250		200	ns
t_{PHZ} or t_{PLZ}	Output disable time from high or low level‡	30		30		30		ns
t_{PZL}	Output enable time to low level‡		250		200		150	ns

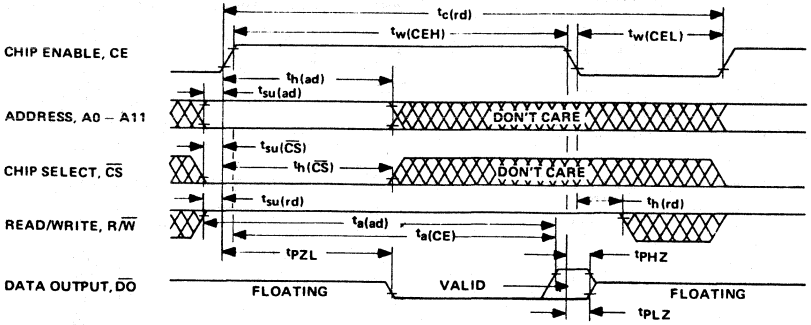
†Test conditions: C_L = 50 pF, $t_{r(CE)}$ = 20 ns, Load = 1 Series 74 TTL gate.
‡Test conditions: C_L = 50 pF, Load = 1 Series 74 TTL gate.

write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time*	0		0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

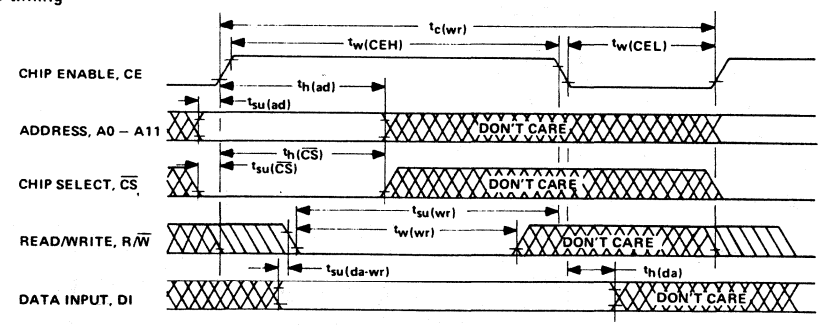
↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*If R/$\overline{W}$ is low before CE goes high then DI must be valid when CE goes high.

read cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high). During the time from the rise of CE to the fall of R/$\overline{W}$, R/$\overline{W}$ is permitted to change from high to low only.

read, modify write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(RMW)}$	Read, modify write cycle time*	710		640		580		ns
$t_{w(CEH)}$	Pulse width, chip enable high*	540	4000	470	4000	410	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write-pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time	0		0		0		ns
$t_{su(rd)}$	Read pulse setup time	0↑		0↑		0↑		ns
$t_{su(wr)}$	Write pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	280↑		230↑		180↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

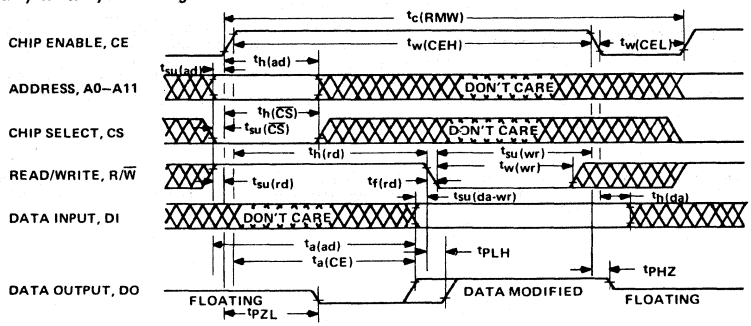
↑↓ The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*Test conditions: $t_{f(rd)}$ = 20 ns.

read, modify write cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable†		280		230		180	ns
$t_{a(ad)}$	Access time from address†		300		250		200	ns
t_{PLH}	Propagation delay time, low-to-high level output from write pulse‡	30		30		30		ns
t_{PHZ}	Output disable time from high level‡	30		30		30		ns
t_{PZL}	Output enable time to low level‡		250		200		150	ns

†Test conditions: C_L = 50 pF, $t_{r(CE)}$ = 20 ns, Load = 1 Series 74 TTL gate.
‡Test conditions: C_L = 50 pF, Load = 1 Series 74 TTL gate.

read, modify write cycle timing



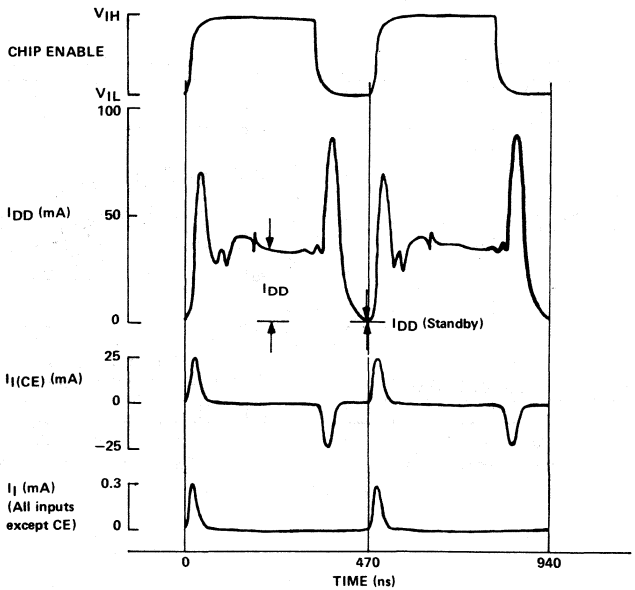
NOTE: For the chip enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

timing diagram conventions

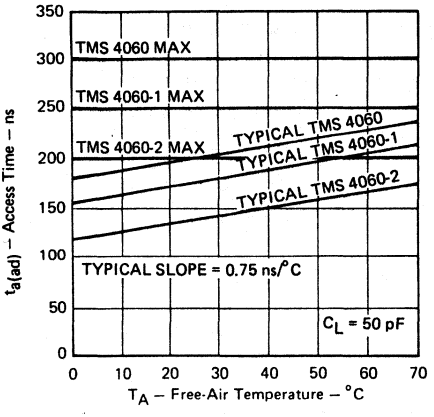
TIMING DIAGRAM SYMBOL	MEANING	
	INPUT FORCING FUNCTIONS	OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

3

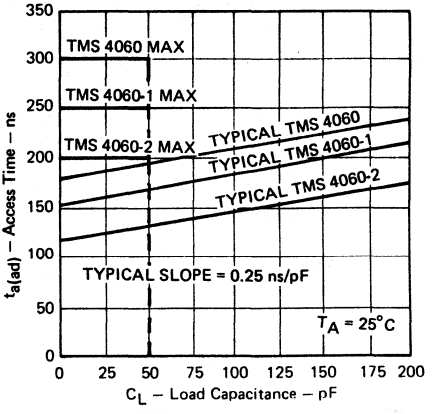
TYPICAL WAVEFORMS



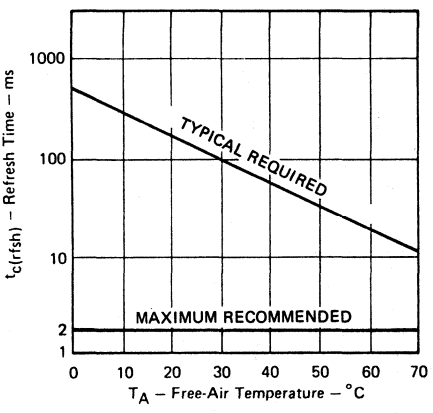
ACCESS TIMES vs TEMPERATURE



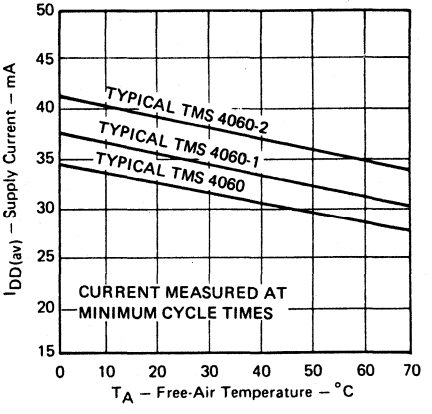
ACCESS TIMES vs LOAD CAPACITANCE



REFRESH TIME vs TEMPERATURE



AVERAGE CURRENT vs TEMPERATURE



TMS 4070 JL
16,384-BIT DYNAMIC RANDOM-ACCESS MEMORY

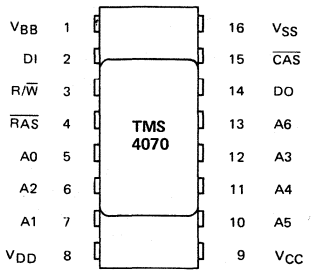
JULY 1976

The TMS 4070 is the first of the new generation of dynamic RAMs which have been designed for mainframe and microprocessor applications. It combines high performance, low power and high packing density in one N-Channel Silicon-Gate LSI device. All inputs/outputs are fully TTL compatible to simplify system interface. The device has been designed with 7 multiplexed address lines and an unlatched data output and separate data input. This offers the best package size/performance trade-off in a high density RAM.

Features

- 16,384 X 1 Organization
- 16-Pin 300-Mil Package Configuration
- All Inputs Including Clocks TTL Compatible
- Three-State Fully TTL-Compatible Output
- On-Chip Latches for Addresses and Data Input
- Access Times:
  - Row Address . . . 350 ns (Maximum)
  - Column Address . . . 230 ns (Maximum)
- Cycle Times:
  - Read or Write . . . 550 ns (Minimum)
  - Read-Write† . . . 730 ns (Minimum)
- Low-Power Dissipation
  - 600 mW Operating (Typical)
  - 25 mW Standby (Typical)
- 1-T Cell Design, N-Channel Silicon-Gate Technology

16-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



3

TENTATIVE DATA

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

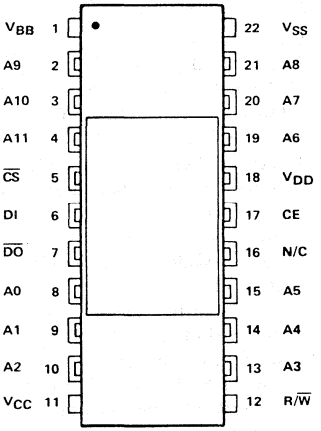
TMS 4030 JR, TMS 4050 JR, TMS 4060 JR
SMC 4030 JR, SMC 4050 JR, SMC 4060 JR
4096-BIT RANDOM-ACCESS MEMORIES

BULLETIN NO. DL-S 7512276, MAY 1975

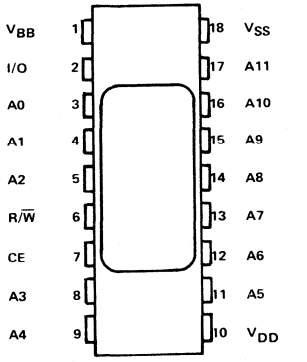
EXTENDED TEMPERATURE RANGE AND HI-REL DEVICES

- 4096 x 1 Organization
- Extended Temperature Range (−55°C to 85°C)
- SMC Type Processed to Class B of MIL-STD-883 per Level III of TI 38510/MACH-IV Program
- Maximum Access Time . . . 300 ns
- Minimum Read or Write Cycle . . . 470 ns
- Minimum Read, Modify Write Cycle: 710 ns (730 ns for TMS 4050)
- Full TTL Compatibility on All Inputs (No Pull-Up Resistors Needed)
- Single Low-Capacitance Clock

TMS 4030 JR, TMS 4060 JR
SMC 4030 JR, SMC 4060 JR
22-PIN CERAMIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



TMS 4050 JR, SMC 4050 JR
18-PIN CERAMIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS 4030 JR, TMS 4050 JR, and TMS 4060 JR are extended temperature range (−55°C to 85°C) versions of the TMS 4030 JL, TMS 4050 JL, and TMS 4060 JL. These devices are ideal for critical equipment applications in aerospace, industrial, and military environments.

The SMC 4030 JR, SMC 4050 JR, and SMC 4060 JR are also rated to operate from −55°C to 85°C. These SMC devices are specifically processed and 100% screened to the requirements of Class B of MIL-STD-883 per level III of the Texas Instruments 38510/MACH-IV program.

The SMC series of 4096-bit RAMs receive the following special screening tests:

Precap visual	method 2010.2
Stabilization bake	method 1006.1
Temperature cycling	method 1010.1
Centrifuge	method 2001.1
Fine and gross leak	method 1014.1
Burn-in for 168 hours at 125°C	method 1015.1
Final electrical testing at 25°C and high temperatures	

These two series of devices are offered only in ceramic (JR suffix) dual-in-line packages. The 22-pin package (TMS 4030, TMS 4060, SMC 4030, and SMC 4060) inserts in mounting-hole rows on 400-mil centers. The 18-pin package (TMS 4050, SMC 4050) is designed for insertion in mounting-hole rows on 300-mil centers and is ideal for high-density applications.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

operation

For a complete description of the device operation see the appropriate data sheets on the commercial temperature range (0°C to 70°C, JL, NL suffix) 4K RAM products. All timing parameters on these extended-temperature range and high-reliability devices are identical with the associated 300-ns-access-time commercial device types.

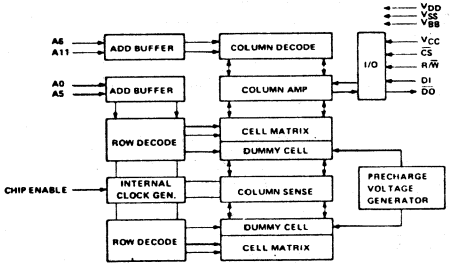
For detailed information on processing, refer to TI's MACH IV program and High-Reliability Microelectronics Procurement Specifications, MIL-STD-883.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

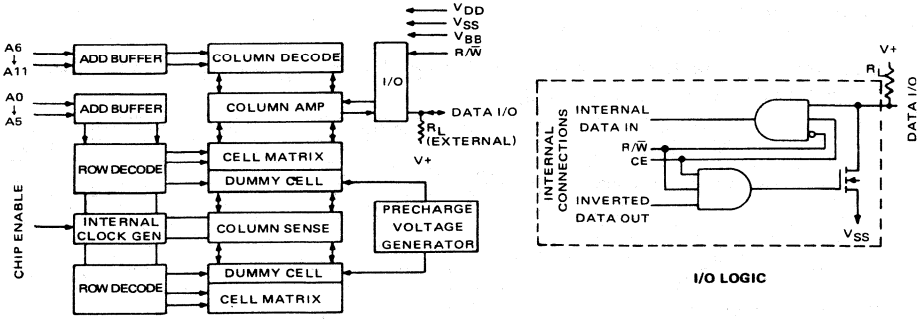
Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 20 V
All input voltages (see Note 1)	−0.3 to 20 V
Chip-enable voltage (see Note 1)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet voltage values are with respect to V_{SS}.

functional block diagram



TMS 4030/SMC 4030, TMS 4060/SMC 4060



I/O LOGIC

TMS 4050/SMC 4050

recommended operating conditions

PARAMETER	TMS 4030 JR SMC 4030 JR			TMS 4060 JR SMC 4060 JR			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	11.4	12	12.6	V
Supply voltage, V_{SS}		0			0		V
Supply voltage, V_{BB}	−2.7	−3	−3.3	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.25	2.2		5.25	V
High-level chip enable input voltage, $V_{IH(CE)}$	V_{DD} −0.6		V_{DD} +1	V_{DD} −0.6		V_{DD} +1	V
Low-level input voltage, V_{IL} (all inputs except chip enable)	−0.6†		0.6	−0.6†		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$	−1†		0.6	−1†		0.6	V
Refresh time, $t_{refresh}$			1			1	ms
Operating free-air temperature, T_A	−55		85	−55		85	°C

†The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = −55°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −2 mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_O = 3.2 mA	V_{SS}		0.4	V
I_I	Input current (all inputs except chip enable)	V_I = 0 to 5.25 V			10	μA
$I_{I(CE)}$	Chip-enable input current	V_I = 0 to 13.2 V			2	μA
I_{OZ}	High-impedance-state (off-state) output current	V_O = 0 to 5.25 V			10	μA
I_{CC}	Supply current from V_{CC}	2 Series 74 TTL loads			1	mA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 12.6 V		30	80	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V		20	200	μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle time		32		mA
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle	Minimum cycle time		32		mA
I_{BB}	Supply current from V_{BB}	V_{BB} = MAX‡, V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_{SS} = 0 V		−5	−100	μA

†All typical values are at T_A = 25°C.
‡MAX = −3.3 V for TMS 4030; −5.5 V for TMS 4060.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = NOM, V_{CC} = 5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = −55°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 10.8 V		18	22	pF
		$V_{I(CE)}$ = −1 V		23	27	
$C_{i(\overline{CS})}$	Input capacitance chip-select input			4	6	pF
$C_{i(data)}$	Input capacitance data input			4	6	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
C_o	Output capacitance			5	7	pF

†All typical values are at T_A = 25°C.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.5	V
High-level chip-enable input voltage, $V_{IH(CE)}$	V_{DD} −0.6		V_{DD} +1	V
Low-level input voltage, V_{IL} (all inputs except chip enable)	−0.6†		0.6	V
Low-level chip-enable input voltage, $V_{IL(CE)}$	−1†		0.6	V
Refresh time, $t_{refresh}$			1	ms
Operating free-air temperature, T_A	−55		85	°C

†The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = −55°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	t_a = guaranteed maximum access time, R_L = 2.2 kΩ to 5.5 V, C_L = 50 pF, Load = 1 Series 74 TTL gate	2.4			V
V_{OL}	Low-level output voltage		V_{SS}		0.4	V
I_{OL}	Low-level output current	t_a = guaranteed maximum access time, C_L = 50 pF, V_{OL} = 0.4 V	5			mA
I_I	Input current (all inputs including I/O except chip enable)	V_I = −0.6 to 5.5 V			10	μA
$I_{I(CE)}$	Chip-enable input current	V_I = −1 to 13.2 V			10	μA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 13.2 V		35	80	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V		10	200	μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle timing		32		mA
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle	Minimum cycle timing		32		mA
I_{BB}	Supply current from V_{BB}	V_{BB} = −5.5 V, V_{DD} = 12.6 V, V_{SS} = 0 V		5	100	μA

†All typical values are at T_A = 25°C.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = −55°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 12 V		24	28	pF
		$V_{I(CE)}$ = 0 V		29	33	
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
$C_{(I/O)}$	I/O terminal capacitance			7	9	pF

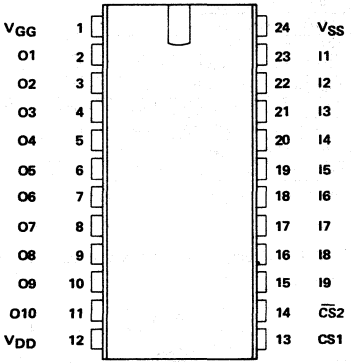
†All typical values are at T_A = 25°C.

TMS 2501 JC, NC
64 x 5 x 7 STATIC USASCII CHARACTER GENERATOR

MAY 1975

- Organization . . . 64 Characters of 35 Bits in a 5 x 7 Matrix
- Access Time . . . 250 ns Typical
- Inputs and Outputs Fully TTL-Compatible
- Two Chip-Select Inputs
- 3-State Output Buffers for OR-Ties
- Row Output (Seven 5-Bit Rows in Sequence)

24-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)

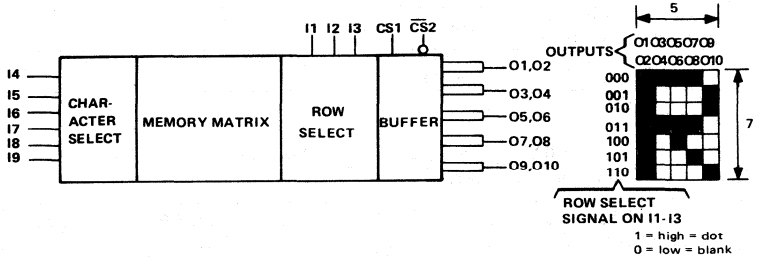


description

The TMS 2501 generates 64 USASCII characters for driving a 5 x 7 matrix display. All inputs can be driven directly from Series 74 TTL circuits and the 3-state push-pull output buffers can drive Series 74 TTL circuits without external resistors. The 5-bit row words appear on the odd-numbered outputs with I9 low and on the even-numbered outputs with I9 high. Outputs O1 and O2, O3 and O4, . . . O9 and O10 must be externally OR-tied in pairs. CS1 must be high and $\overline{CS2}$ low to enable the device.

The TMS 2501 is offered in 24-pin ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The devices are characterized for operation from −25°C to 85°C.

functional block diagram

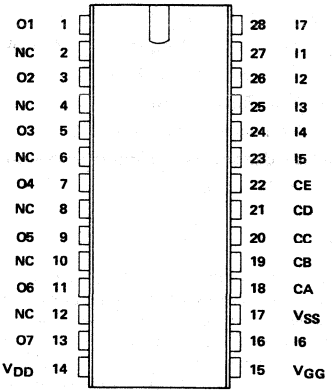


TMS 4103 JC, NC
64 x 5 x 7 STATIC USASCII CHARACTER GENERATOR

MAY 1975

- Organization . . . 64 Characters of 35 Bits in a 5 x 7 Matrix
- Access Time . . . 500 ns Typical
- Inputs and Outputs Fully TTL-Compatible
- 7-Bit Input Address
- Open-Drain Output Buffers
- Column Output (Five 7-Bit Columns in Sequence)

28-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



NC – No Connection

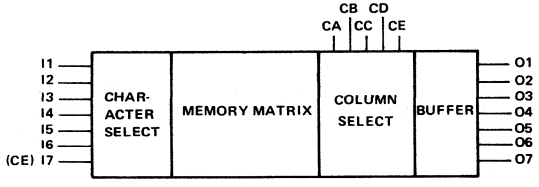
description

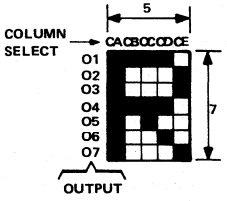
The TMS 4103 generates 64 USASCII characters for driving a 5 x 7 matrix display. Output buffers are open-drain and are capable of driving Series 74 TTL circuits without external resistors. All inputs can be driven directly from Series 74 TTL circuits.

The five 7-bit column words appear on O1 through O7 as column select inputs CA through CE are strobed in sequence with a high level pulse. The device is enabled with a high level on I7.

The TMS 4103 is offered in 28-pin ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The devices are characterized for operation from −25°C to 85°C.

functional block diagram



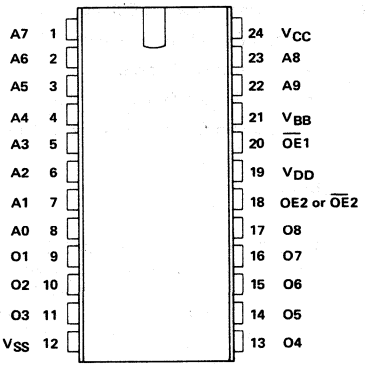


TMS 4700 JL, NL
1024-WORD BY 8-BIT READ-ONLY MEMORY

BULLETIN NO. DL-S 7512273, MAY 1975

- 1024 x 8 Organization
- All Inputs and Outputs TTL-Compatible
- Maximum Access Time . . . 450 ns
- Minimum Cycle Time . . . 450 ns
- Typical Power Dissipation . . . 310 mW
- 3-State Outputs for OR-Ties
- Output Enable Control
- Silicon-Gate Technology
- 8-Bit Output for use in Microprocessor Based Systems

24-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 4700 JL, NL is an 8,192-bit read-only memory organized as 1024 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits. All inputs can be driven by Series 74 TTL circuits with the use of external pull-up resistors and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus. Two output-enable controls, one customer programmable, allow data to be read. The option on output enable 2 is explained in the section "Software Package".

The TMS 4700 is designed for high-density fixed-memory applications such as logic-function generation and microprogramming. This ROM is supplied in 24-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The device is characterized for operation from 0°C to 70°C.

operation

address (A0-A9)

The address-valid interval determines the device cycle time. The 10-bit positive-logic address is decoded on-chip to select one of 1024 words of 8-bit length in the memory array. A0 is the least-significant bit and A9 the most-significant bit of the word address.

output enable ($\overline{OE}1$ and OE2†)

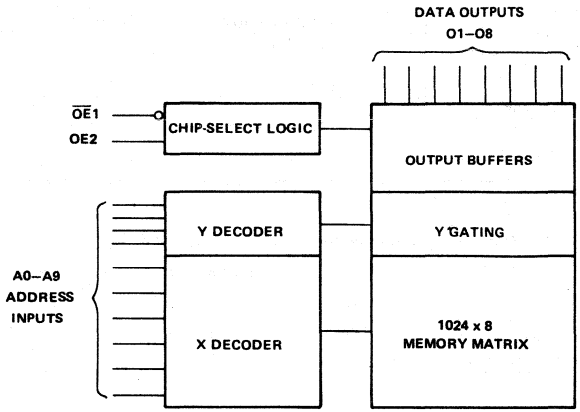
$\overline{OE}1$ is active when it is low. OE2 can be programmed, during mask fabrication, to be active with a high or a low level input. When both output enables are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either output enable is not active, all eight outputs are in a high-impedance state.

data out (O1-O8)

The eight outputs must be enabled by both output enable controls before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled. When disabled, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

†Symbol OE2 assumes output enable 2 is programmed active high. If active low, the symbol would be $\overline{OE}2$.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . –0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1) . . . . . –0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1) . . . . . –0.3 V to 20 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most positive supply, V_{BB} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	–4.75	–5	–5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	3.3		V_{CC}	V
Low-level input voltage, V_{IL}	V_{SS}		0.8	V
Read cycle time, $t_{c(rd)}$	430			ns
Output-enable rise time, $t_{r(\overline{OE1})}$ and $t_{r(OE2)}$		10	20	ns
Output-enable fall time, $t_{f(\overline{OE1})}$ and $t_{f(OE2)}$		10	20	ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C (unless otherwise noted)

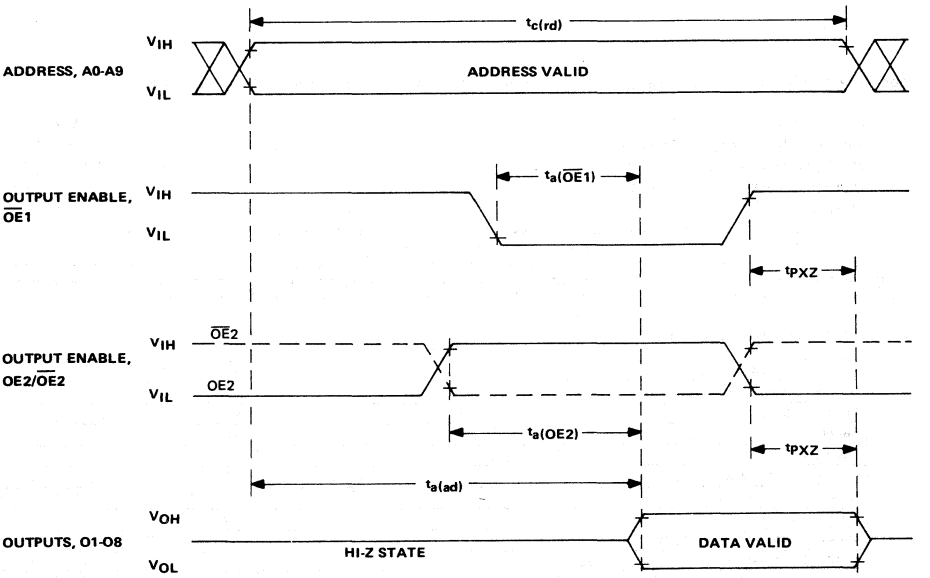
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA	3.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.45	V
I_I	Input current	V_I = 0 to 6.5 V			±10	μA
I_{BB}	Supply current from V_{BB}	Both output enables active		−0.1		mA
I_{CC}	Supply current from V_{CC}			2		mA
I_{DD}	Supply current from V_{DD}			25		mA
P_D	Power dissipation			310		mW

† All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{a(ad)}$	Access time from address	C_L = 50 pF, 1 Series 74 TTL load		430	ns
$t_{a(\overline{OE}1)}$	Access time from output enable 1			90	ns
$t_{a(OE2)}$	Access time from output enable 2			130	ns
t_{PXZ}	Output disable time from either chip enable			90	ns

voltage waveforms



NOTE: Timing points are 90% (high) and 10% (low).

SOFTWARE PACKAGE

The TMS 4700 JL, NL is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer inputs supplied in the format shown. The device is organized as 1024 8-bit words with address locations numbered 0 to 1023. Any 8-bit word can be coded as a 2-digit hexadecimal number between 00 and FF. All stored words and addresses in the following format are coded in hexadecimal numbers. In coding, all binary words must be in positive logic before conversion to hexadecimal. O1 is considered the least-significant bit and O8 the most-significant bit. For addresses A0 is least significant and A9 is most significant.

Every card should include the TI Custom Device Number in the form ZAXXXX (4-digit number to be assigned by TI) in columns 75 through 80.

Output enable 2 is customer programmable. Every card should include in column 74 a 1 if the output is to be enabled with a high-level input at $\overline{OE}2$ or a 0 for enabling with a low-level input.

The 1024 coded words must be supplied on 64 cards with 16 2-digit hex numbers per card.

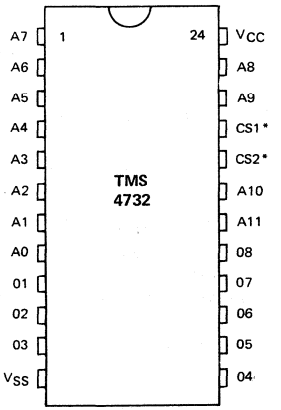
CARD	COLUMN	HEXADECIMAL INFORMATION
1	1–9	BLANK
	10	: (ASCII character colon)
	11–12	10 (specifies 16 words per card)
	13	BLANK
	14–16	Hex address of 1st word on 1st card (0th word, address normally 000)
	17–18	BLANK
	19–20	0th word in Hex
	•	
	•	
	•	
	49–50	15th word in Hex
	51–73	BLANK
64	1–9	BLANK
	10	: (ASCII character colon)
	11–12	10
	13	BLANK
	14–16	Hex address of 1st word on 64th card (1008th word, address normally 3F0)
	17–18	BLANK
	19–20	1008th word in Hex
	•	
	•	
	•	
	49–50	1023rd word in Hex
	51–73	BLANK

PRELIMINARY INFORMATION

TMS 4732
4k x 8 BIT STATIC READ ONLY MEMORY

The TMS 4732 is a 32k Read Only Memory specifically designed for microprocessor systems to meet the growing need for large program memories. The device has been designed using N-channel Silicon Gate technology and has all the inherent advantages of this technology.

The device is mask programmable by Texas Instruments from an 80 column card deck supplied by the user. The card deck specifies the logic level of all 32k memory cells and the function of the two programmable chip-select inputs.



*or inverse (programmable)

Features

- 4k x 8 bit Static ROM
- Fully TTL Compatible
- Single 5 volt power supply operation
- High performance
  - 450 ns Address access time
  - 300 mW power dissipation
- 3-state outputs for simple system expansion

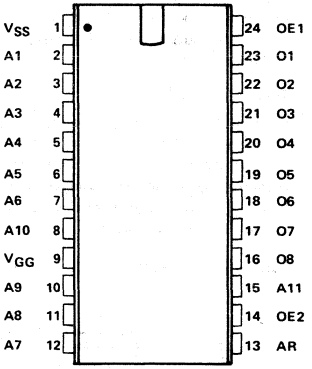
TEXAS INSTRUMENTS

TMS 4800 JL, NL
16384-BIT READ-ONLY MEMORY

BULLETIN NO. DL-S 7512260, MAY 1975

- 2048 x 8 or 4096 x 4 Organization
- Total TTL-Compatibility
- Maximum Access Time . . . 700 ns
- Minimum Cycle Time . . . 1000 ns
- Typical Power Dissipation . . . 450 mW
- Open-Drain Output for Wire-OR Configurations
- 24-Pin 600-Mil Dual-in-Line Packages
- Two Chip-Enable Controls

24-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 4800 JL, NL is a 16384-bit read-only memory, organized as either 2048 words of 8-bits or 4096 words of 4-bits. All inputs are TTL-compatible. The eight open-drain outputs must be connected by pull-down resistors to an external negative supply to drive standard TTL circuits. Two output-enable terminals allow each 2048 x 4-bit array to be read independently as 4-bit words or simultaneously as 8-bit words.

Two devices can be OR-tied, with proper choice of programming on the output-enable terminals to be specified by the customer. Addresses may change up to 50 ns after the clock cycle begins. This allows TTL address-decoding circuits to synchronize on the rise of the clock and stabilize during this interval effectively shortening the device read-access time. The TMS 4800 is designed with P-channel enhancement-type technology for high-density, fixed-memory applications such as logic function generation and microprogramming. This ROM is supplied in a ceramic (JL suffix) or plastic (NL suffix) 24-pin package designed for insertion in mounting-hole rows on 600-mil centers.

operation

address read (AR)

Address read constitutes the master timing signal of the device. After AR goes high, address and output enable inputs latch. The address-read clock is high during the address-valid and output-enable-valid intervals. Data out is valid both before and after AR goes low, since enabled outputs latch during the cycle.

address (A1-A11)

Any of the 2048-word addresses are selected by an 11-bit positive-logic binary word, A1 being the least-significant bit progressing through to A11, which is the most-significant bit. Address inputs can change up to 50 ns after the AR clock goes high and must remain valid 250 ns after AR goes high. This input latching feature allows the user to change address while data is being read. These system advantages result from latching of the internal address register during a short address-valid interval.

output enable (OE1 and OE2)

The ROM consists of two side-by-side 2048-word-by-4-bit arrays. OE1 enables output terminals O1 through O4 and OE2 outputs O5 through O8 with the two arrays being enabled independently. The user may choose any of four combinations by enabling with either a low or high level on OE1 or OE2. To read 8-bit words with a single address, both OE1 and OE2 must be enabled. For 8-bit readout, two devices may be OR-tied to increase the effective size of the ROM system by programming complementary enable levels on corresponding device terminals.

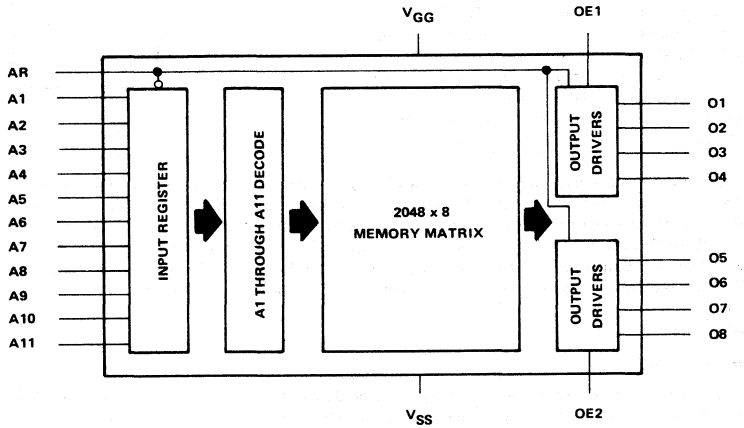
operation (continued)

Output terminals on a single device are OR-tied for a 4096-word x 4-bit organization as follows: O1 to O5; O2 to O6; O3 to O7; and O4 to O8. Since the OE1 and OE2 inputs latch internally, the enable signals may change before or during the output data-valid interval. For additional information on OR-ties, see the section on Expanded Memory Configurations.

data out (O1-O8)

Outputs O1 through O4 are enabled by OE1 with outputs O5 through O8 enabled by OE2. Output transistors are open-drain and compatible with TTL circuits when connected to an external negative supply through a pull-down resistor. All outputs go low immediately after the rise of AR. A disabled output rises to a high level after a propagation delay following the fall of the AR clock if a high logic level was stored. If devices are OR-tied, an enabled output should be read before AR goes low in order to distinguish a stored high from a high coming from the OR-tied disabled output. Because the outputs latch, data on an enabled output remains valid until the next rise of the AR clock.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{GG} (see Note 1)	−20 to 0.3 V
All input voltages (see Note 1)	−20 to 0.3 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to a floating ground.

*COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{SS}	4.75	5	5.25	V
Supply voltage, V_{GG}	−11	−12	−13	V
High-level input voltage, V_{IH} (all inputs)	V_{SS} −1.5		V_{SS}	V
Low-level input voltage, V_{IL} (all inputs) (see Note 2)	−4		0.6	V
Read cycle time, $t_{c(rd)}$	1000			ns
Pulse width, address read high, $t_{w(ARH)}$	500		100000	ns
Pulse width, address read low, $t_{w(ARL)}$	450			ns
Address-read rise time, $t_{r(AR)}$			40	ns
Address-read fall time, $t_{f(AR)}$			40	ns
Address-read-high-to-address delay time, $t_{d(ARH-ad)}$			50	ns
Address-read-high-to-output-enable delay time, $t_{d(ARH-OE)}$			50	ns
Address hold time, $t_{h(ad)}$	250			ns
Output-enable hold time, $t_{h(OE)}$	250			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 2. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only.

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2.4 mA	2.5			V
I_{OL}	Low-level output current	V_{OL} = 0.4 V			50	μA
I_I	Input current (all inputs)	$V_I = V_{SS}$			1	μA
I_{SS}	Supply current from V_{SS}			29	40	mA
I_{GG}	Supply current from V_{GG}			−29	−40	mA

‡All typical values are at T_A = 25°C.

switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C (unless otherwise noted)

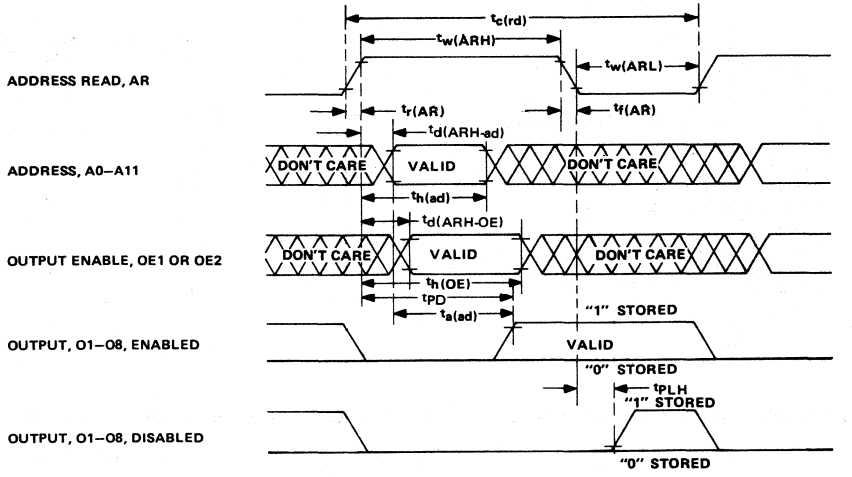
PARAMETER		MIN	TYP‡	MAX	UNIT
$t_{a(ad)}$	Access time from address		550	700	ns
t_{PLH}	Propagation delay time, low-to-high level output from address read (output disabled)	200			ns
t_{PD}	Propagation delay time from address read to data valid		600	750	ns

‡Typical values are measured at V_{SS} = 5 V, V_{GG} = −12 V, and T_A = 25°C.

NOTES: 3. Enabled outputs remain valid until next AR pulse. Disabled outputs may be considered valid until 200 ns after the high-to-low transition of AR.

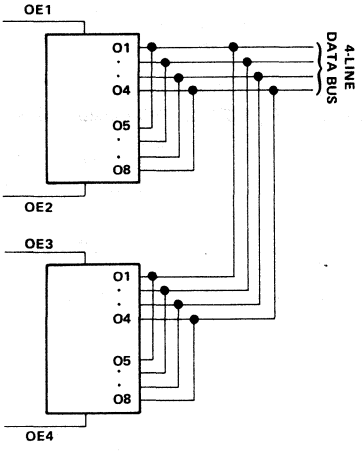
4. All rise and fall times are ≤20 ns.

voltage waveforms



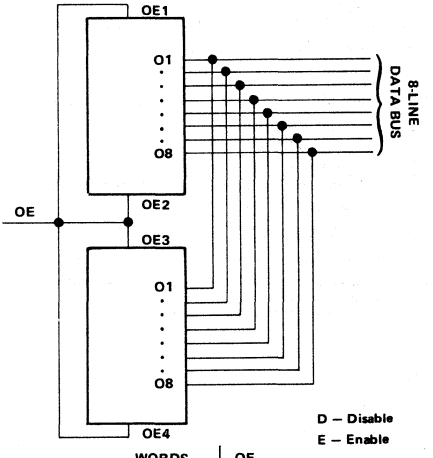
EXPANDED READ-ONLY MEMORY CONFIGURATIONS

8K x 4



WORDS	OE1	OE2	OE3	OE4
0–2048	E	D	D	D
2049–4096	D	E	D	D
4097–6144	D	D	E	D
6145–8192	D	D	D	E

4K x 8



WORDS	OE
0–2048	E
2049–4096	D

NOTE: One device programmed to enable with OE1 = OE2 = 1
Other device programmed to enable with OE1 = OE2 = 0

SOFTWARE PACKAGE

The TMS 4800 JL, NL is a fixed program memory in which the programming is performed by TI, at the factory during the manufacturing cycle, to the specific customer inputs supplied in the format shown. The device is organized so that it can be used for storing either 2048 words of 8 bits or 4096 words of 4 bits. Words of 8- or 4-bit lengths are read by proper enable levels on OE1 and OE2. Output O1 is the least-significant bit in an 8-bit word, O5 and O1 in 4-bit words. All addresses and stored words in either organization are coded in octal. Any address up to 2048 can be written as a 4-digit octal number. Any 8-bit binary word can be converted to a 3-bit octal number. In coding, all binary words must be in positive logic and right justified before conversion to octal.

Every card must include the following coded information.

Column 73—OE1 enable code
Column 74—OE2 enable code
Columns 75–80 — TI CUSTOM DEVICE NUMBER ZAXXXX (4-DIGIT NUMBER ASSIGNED BY TI)

The output enable (OE) option is programmed on the chip with the customer pattern. A high voltage level enable is specified by a "1" in columns 73 or 74, a low voltage level enable by a "0".

2048-word by 8-bits

Code deck format –

Card	Column	Octal Information
1	1–4	Octal address (N) of 1st output word on 1st card
	5–7	1st stored 8-bit word (in octal)
	8–10	2nd stored 8-bit word (in octal)
	•	
	•	
	50–52	16th stored 8-bit word (in octal)
2	1–4	Octal address (N + 16) of 1st output word on 2nd card
	5–7	17th stored 8-bit word
	•	
	•	
	50–52	32nd stored 8-bit word
128	1–4	Octal address (N + 2032) of 1st output word on 128th card
	5–7	2033rd stored 8-bit word
	•	
	•	
	50–52	2048th stored 8-bit word

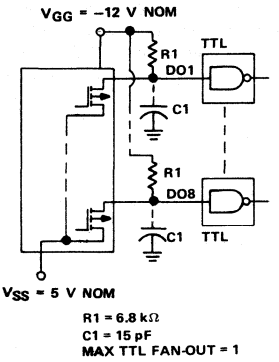
4096-word by 4-bits

Terminals OE1 and OE2 independently enable outputs O1-O4 and O5-O8. Each enable terminal can be programmed to enable with a high or low level input.

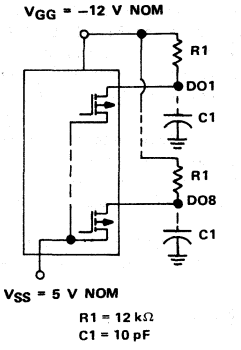
To read only 4 bits simultaneously from either set of output terminals, the stored information *must* be coded as an 8-bit positive logic binary word converted to octal. Each 4-bit binary word is right justified before forming the 8-bit word. In coding, words 1 and 2049, 2 and 2050, . . . and 2048 and 4096 are combined (O8-O5 on the left of O4-O1) as 8-bit words and converted to octal as in the case of the 2048 by 8 coding instructions. This coding format also requires 128 cards with 16 octal words (32 4-bit binary words) per card.

OUTPUT INTERFACE

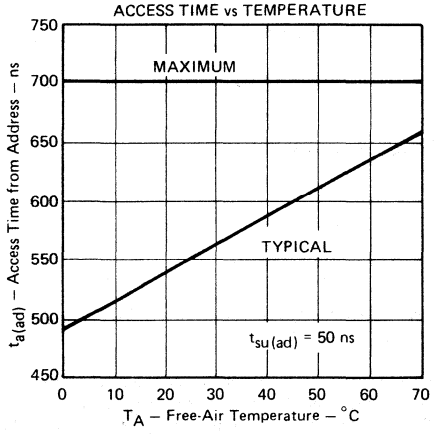
single resistor TTL interface

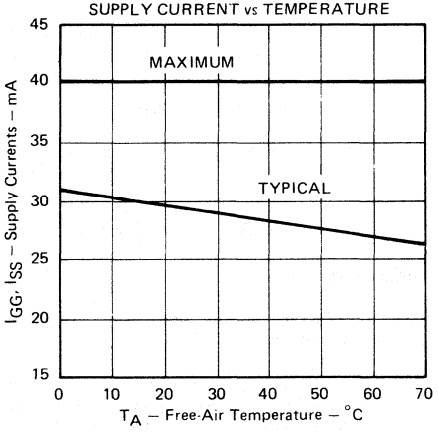


MOS interface



TYPICAL CHARACTERISTICS





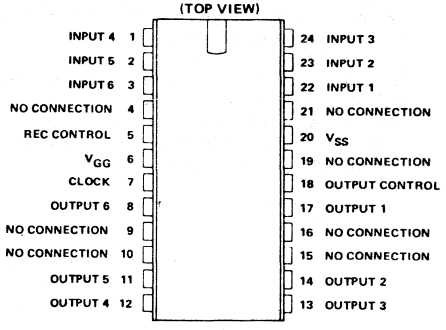
TEXAS INSTRUMENTS

TMS 3112 JC, NC;
HEX 32-BIT STATIC SHIFT REGISTER

- DC to 2-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs are Fully TTL-Compatible
- Single-Ended (Open-Drain) Buffers
- On-Chip Recirculate Logic
- Gated-Output Control
- Power Supplies . . . 5 V, −12 V
- MOS Low-Threshold P-Channel Technology

CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES

TMS 3112
(TOP VIEW)



description

The TMS 3112, is a 6-channel by 32-bit shift register on a single monolithic chip with separate inputs and outputs and a common recirculate control. The TMS 3112 features a common output gating control. The clock and all inputs can be driven directly from Series 74 TTL circuits and all outputs are capable of driving one Series 74 TTL circuit.

Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows input data rates from dc to 2 MHz and long-term data storage.

P-channel enhancement-type low-threshold processing has been employed to reduce power dissipation and provide simple interfaces with bipolar circuits.

The TMS 3112 is offered in 24-pin dual-in-line ceramic (JC suffix) or plastic (NC suffix) packages This device is characterized for operation from −25°C to 85°C

applications

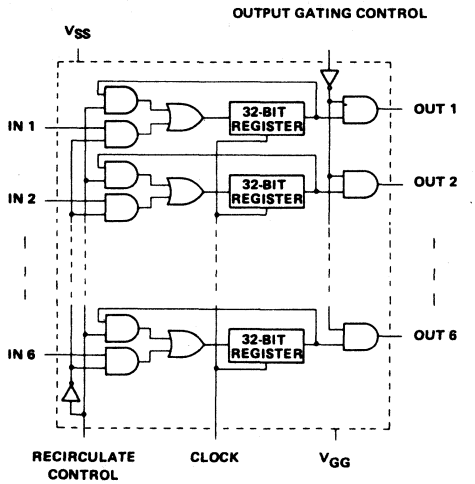
The TMS 3112, can be used in printers, terminals, and peripheral (IBM System 3) applications where 32, bits of serial storage are needed.

operation

Transfer of data into and out of the shift register occurs on the low-to-high transition of the clock. Input data must be set up a minimum time before the low-to-high transition and must be held for a minimum time after that transition. For long-term data storage, the clock must be maintained high, and in this mode the recirculate and data input levels may change without affecting the data output levels.

Recirculate occurs on the low-to-high clock transition with the recirculate control high. The recirculate control level must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control low. During recirculation, data is continuously available at the outputs when the output gate control is low. A high level on the output gate control forces all outputs low. Data inputs are inhibited during recirculation.

functional block diagram



FUNCTION TABLE

RECIRCULATE	INPUT	FUNCTION
H	L	Recirculate
H	H	Recirculate
L	L	L is written
L	H	H is written

H = high level
L = low level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−20 V to 0.3 V
Data input voltage (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to a floating ground.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH}	V_{SS} −1.3		V_{SS}	V
High-level clock voltage, $V_{IH(\phi)}$	V_{SS} −1.3		V_{SS}	V
Low-level input voltage, V_{IL}			V_{SS} −4	V
Low-level clock voltage, $V_{IL(\phi)}$			V_{SS} −4	V
Clock pulse transition time, low-to-high-level, $t_{TLH(\phi)}$			5000	ns
Clock pulse transition time, high-to-low-level, $t_{THL(\phi)}$			5000	ns
Pulse width, clock high, $t_{w(\phi H)}$	300		∞	ns
Pulse width, clock low, $t_{w(\phi L)}$	150		50000	ns
Recirculate pulse width, $t_{w(rec)}$	250			ns
Data setup time, $t_{su(da)}$	60			ns
Recirculate setup time, $t_{su(rec)}$	120			ns
Data hold time, $t_{h(da)}$	60			ns
Recirculate hold time, $t_{h(rec)}$	100			ns
Clock frequency, f_{ϕ}	0		2	MHz
Operating free-air temperature, T_A	−25		85	°C

electrical characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R_L = 7.5 kΩ to V_{GG}	V_{SS} −1			V
V_{OL}	Low-level output voltage	R_L = 7.5 kΩ to V_{GG}, $I_{OL} \approx$ −1.6 mA			0.6	V
I_I	Input current (all inputs)	V_I = 0 V			−500	nA
I_{GG}	Supply current from V_{GG}	Load = 1 TTL gate (see Note 2), f = 1 MHz, T_A = 25°C		−15	−25	mA
I_{SS}	Supply current from V_{SS}	Load = 1 TTL gate (see Note 2), f = 1 MHz, T_A = 25°C		25	30	mA
P_D	Power dissipation	Load = 1 TTL gate (see Note 2), f = 1 MHz, T_A = 25°C		425	500	mW
C_i	Input capacitance, all inputs except clock	V_I = V_{SS}, f = 1 MHz		5	7	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = V_{SS}, f = 1 MHz		6	7	pF

†All typical values are at T_A = 25°C.

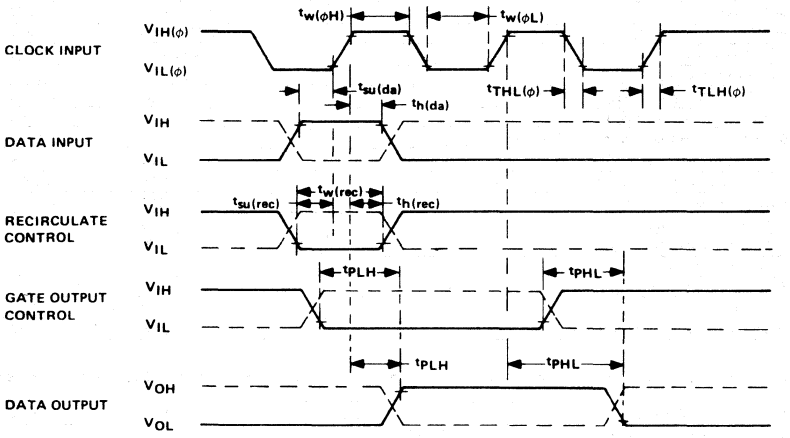
NOTE 2: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF.

switching characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	R_L = 7.5 kΩ to V_{GG}, C_L = 70 pF		350	440	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			350	440	ns
t_{PLH}	Propagation delay time, low-to-high-level output from output control	R_L = 7.5 kΩ to V_{GG}, C_L = 70 pF		180	250	ns
t_{PHL}	Propagation delay time, high-to-low-level output from output control			180	250	ns

†All typical values are at T_A = 25°C.

voltage waveforms



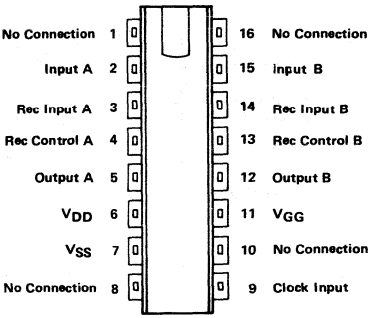
NOTE: Measurements are made at 90% (high) and 10% (low) timing points.

TMS 3113 JC, NC; TMS 3114 JC, NC
DUAL 133-, 128-BIT STATIC SHIFT REGISTERS

BULLETIN NO. DL-S 7512262, MAY 1975

- DC to 2-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- On-Chip Recirculate Logic
- Power Supplies . . . 5 V, −12 V
- Low-Threshold Technology

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 3113 JC, NC and TMS 3114 JC, NC are dual static shift registers with independent input, output, and recirculate controls for each register. A single-phase clock is common to both registers. The clock and all inputs can be driven from Series 74 TTL circuits and each output can drive one Series 74 TTL circuit.

Three clocks are generated internally. Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows data rates from dc to 2 MHz and long-term data storage.

P-channel enhancement-type low-threshold processing has been employed to reduce power dissipation and provide simple interfaces with bipolar circuits.

The TMS 3113 and TMS 3114 are offered in 16-pin dual-in-line ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

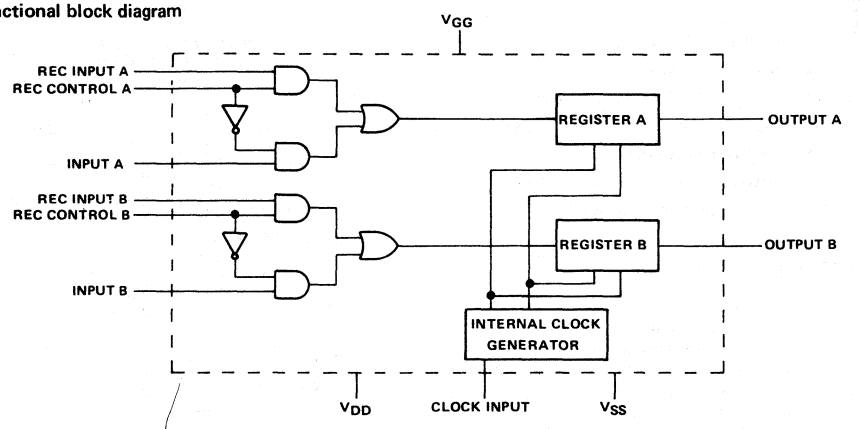
The TMS 3113 and TMS 3114 can be used in printers, peripherals, and display equipment.

operation

Transfer of data into and out of the shift register occurs on the low-to-high transition of the clock. Input data must be set up a minimum time before the low-to-high transition and must be held for a minimum time after that transition. For long-term data storage, the clock must be maintained high, and in this mode the recirculate and data input levels may change without affecting the data output levels.

Data recirculation is accomplished by externally connecting each output to the corresponding input. Recirculate occurs on the low-to-high clock transition with the recirculate control high. The recirculate control level must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control low. During recirculation, data is continuously available at the outputs and data inputs are inhibited.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage V_{DD} (see Note 1)	−6 V to 0.3 V
Supply voltage V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−15 V to 0.3 V
Data input voltage (see Note 1)	−15 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		0		V
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH}	3.5			V
High-level clock input voltage, $V_{IH(\phi)}$	3.5			V
Low-level input voltage, V_{IL}			0.6	V
Low-level clock input voltage, $V_{IL(\phi)}$			0.6	V
Clock pulse transition time, low-to-high-level, $t_{TLH(\phi)}$		0.02	5	μs
Clock pulse transition time, high-to-low-level, $t_{THL(\phi)}$		0.02	5	μs
Pulse width, clock high, $t_{w(\phi H)}$	330		∞	ns
Pulse width, clock low, $t_{w(\phi L)}$	130		50000	ns
Data setup time, $t_{su(da)}$	100			ns
Recirculate setup time, $t_{su(rec)}$	100			ns
Data hold time, $t_{h(da)}$	100			ns
Recirculate hold time, $t_{h(rec)}$	150			ns
Clock frequency, f_{ϕ}	0		2	MHz
Operating free-air temperature, T_A	−25		85	°C

electrical characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 0.2 mA	4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.5	V
I_I	Input current (all inputs)	V_I = 0.6 V			–500	nA
I_{GG}	Supply current from V_{GG}	Load = 1 TTL gate (see Note 2)		–17		mA
I_{SS}	Supply current from V_{SS}	Load = 1 TTL gate (see Note 2)		32		mA
P_D	Power dissipation	Load = 1 TTL gate (see Note 2)		360		mW
C_i	Input capacitance, all inputs except clock	V_I = 5 V, f = 1 MHz		8	12	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = 5 V, f = 1 MHz		9	13	pF

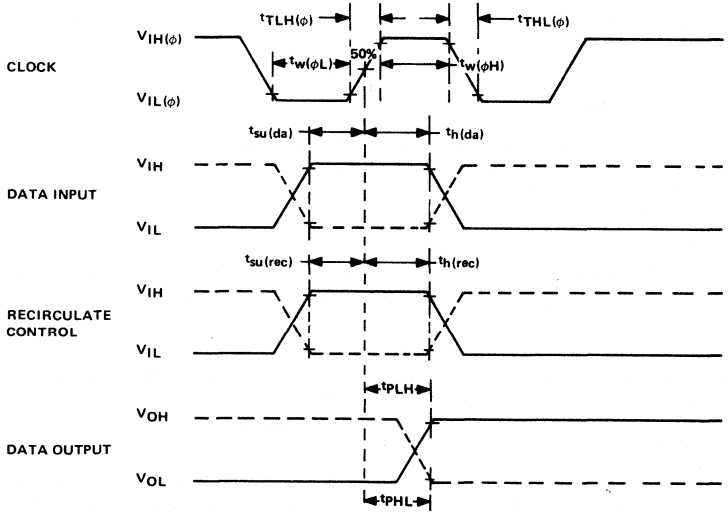
†All typical values are at T_A = 25°C.
NOTE 2: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF.

switching characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	1 Series 74 TTL Load + 10 pF OR 10 MΩ + 10 pF (MOS Load) (see Note 3)		300	350	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			300	350	ns

†All typical values are at T_A = 25°C.
NOTE 3: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 10 MΩ and 10 pF. All loads are connected between output and V_{SS}.

voltage waveforms



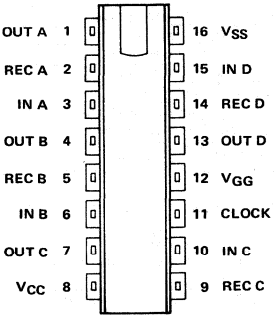
NOTE: Timing points are at 90% (high) and 10% (low) unless otherwise noted.

TMS 3120 JC, NC; TMS 3121 JC, NC
QUADRUPLE 80-, 64-BIT STATIC SHIFT REGISTERS

BULLETIN NO. DL-S 7512267, MAY 1975

- DC to 2.5-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- Push-Pull Output Buffers
- On-Chip Recirculate Logic
- Power Supplies . . . 5 V, −12 V
- Low-Threshold MOS Technology

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 3120 and TMS 3121 are quad 80-bit and quad 64-bit shift registers with independent inputs, outputs, and recirculate controls for each register. A single-phase clock is common to all registers. The clock and data inputs can be driven from Series 74 TTL circuits and the push-pull output buffers can drive one TTL load or low-level MOS loads without external pull-up resistors.

Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows input data rates from dc to 2.5 MHz and long-term data storage.

P-channel enhancement-type low-threshold processing has been employed to reduce power dissipation and provide simple interface with bipolar circuits.

The TMS 3120 and TMS 3121 are offered in 16-pin dual-in-line ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

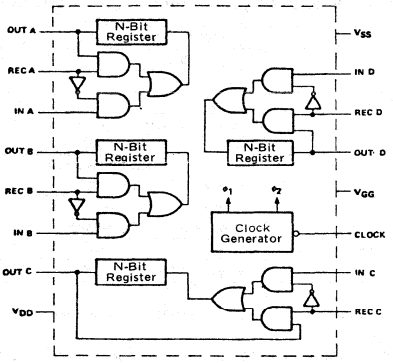
The TMS 3120 can be used in card punch, key-to-tape, key-to-disk, printer, and CRT display equipment for both 40- and 80-column applications. The TMS 3121 is used in general purpose buffer memories.

operation

Transfer of data into and out of the shift register occurs on the high-to-low transition of the clock. Input data must be set up a minimum time before the high-to-low clock transition and must be held for a minimum time after that transition. For long term data storage, the clock must be maintained low, and in this mode the recirculate and data input levels may change without affecting the data output levels.

Recirculate occurs on the high-to-low clock transition with the recirculate control high. The recirculate control must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control low. During recirculation, data is continuously available at the output and the data input is inhibited.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−20 V to 0.3 V
Data input voltage (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		0		V
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH}	V_{SS} −1.6			V
High-level clock input voltage, $V_{IH(\phi)}$	V_{SS} −1.6			V
Low-level input voltage, V_{IL}			0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$			0.8	V
Clock pulse transition time, low-to-high-level, $t_{TLH(\phi)}$			10	μs
Clock pulse transition time, high-to-low-level, $t_{THL(\phi)}$			10	μs
Pulse width, clock high, $t_{w(\phi H)}$	200		100000	ns
Pulse width, clock low, $t_{w(\phi L)}$	200		∞	ns
Data setup time, $t_{su(da)}$	190			ns
Recirculate setup time, $t_{su(rec)}$	190			ns
Data hold time, $t_{h(da)}$	90			ns
Recirculate hold time, $t_{h(rec)}$	90			ns
Clock frequency, f_{ϕ} (see Note 2)	0		2.5	MHz
Operating free-air temperature, T_A	−25		85	°C

NOTE 2: For cascading, data input frequency = 2 MHz maximum.

electrical characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 100 μA	V_{SS} –1	V_{SS} –0.5		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		0.2	0.4	V
I_I	Input current (all inputs)	V_I = 0			–0.1	μA
I_{GG}	Supply current from V_{GG}	Load = 1 TTL gate (see Note 3) f = 1 MHz, T_A = 25°C		–10	–15	mA
I_{SS}	Supply current from V_{SS}	Load = 1 TTL gate (see Note 3) f = 1 MHz, T_A = 25°C		30	35	mA
P_D	Power dissipation	Load = 1 TTL gate (see Note 3) f = 1 MHz, T_A = 25°C			355	mW
C_i	Input capacitance, all inputs except clock	V_I = V_{SS}, f = 1 MHz		3.5	5	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = V_{SS}, f = 1 MHz		3.5	5	pF

†All typical values are at T_A = 25°C.
NOTE 3: For test purposes, a TTL load is simulated by a load of 2.7 kΩ and 20 pF between the output and V_{SS}.

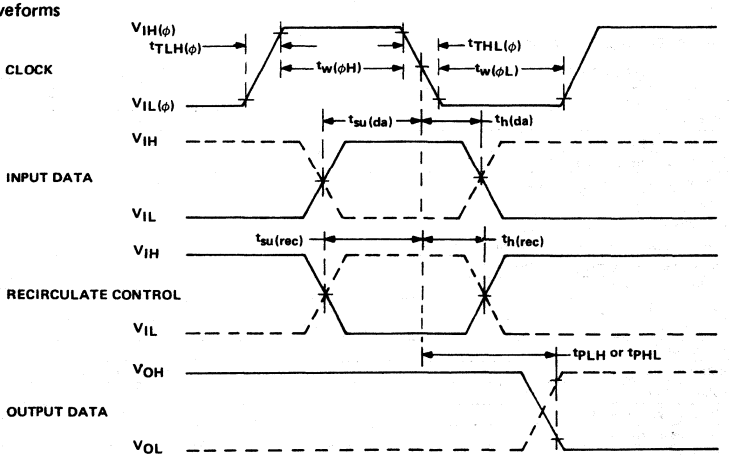
3

switching characteristics under nominal operating conditions, T_A = –25°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	1 Series 74 TTL Load + 10 pF (see Note 4)	100	400	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		100	400	ns
t_{PLH}	Propagation delay time, high-to-low-level output from clock	R_L = 10 MΩ, C_L = 10 pF (MOS Load), (see Note 4)	100	300	ns
t_{PHL}	Propagation delay time, low-to-high-level output from clock		100	300	ns

NOTE 4: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 10 MΩ and 10 pF. All loads are connected between output and V_{SS}.

voltage waveforms



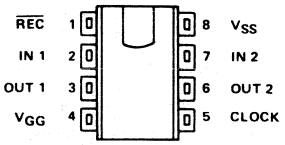
NOTE: For the clock input and output data, timing points are 90% (high) and 10% (low). All other timing points are at 50%.

TMS 3127, 3128, 3129, 3130, 3132 LC, NC
DUAL 100-, 128-, 132-, 133-, 144-BIT
STATIC SHIFT REGISTERS

MAY 1975

- DC to 2.5-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- Push-Pull Output Buffers
- On-Chip Recirculate Logic
- Power Supplies . . . 5 V, −12 V
- Seven Standard Bit Lengths

8-PIN PLASTIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

This series is a family of MOS dual static shift registers. These circuits are monolithically constructed by use of thick-oxide techniques and P-channel enhancement-type transistors, which allow TTL-compatibility for ease of system design.

An on-chip clock generator provides three internal phases from a single external TTL-level clock. All inputs including the low-capacitance clock can be driven directly from Series 74 TTL circuits without the need for pull-up resistors. The push-pull outputs are compatible with Series 74 TTL and have a fan-out capability of one TTL load. A current limiter has been incorporated in the output buffers to reduce power dissipation when driving bipolar logic. No external components are needed for TTL interface.

Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows input data rates from dc to 2.5 MHz and long-term data storage. Recirculate logic has been incorporated on the chip to simplify system design.

These devices are offered in the 8-pin dual-in-line plastic package (suffix NC). The 8-pin dual-in-line package is designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

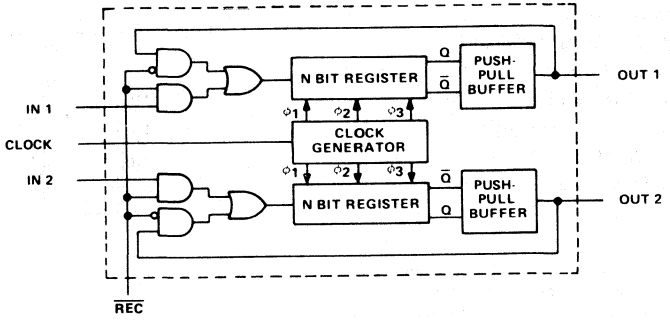
Various bit lengths are offered to cover most computer peripheral applications such as printers, buffer memories, and CRT refresh memories.

operation

Transfer of data into and out of the shift registers occurs on the low-to-high transition of the clock. Input data must be set up a minimum time before the low-to-high clock transition and must be held for a minimum time after that transition. For long-term data storage, the clock must be maintained high, and in this mode the recirculate and data input levels may change without affecting the data output levels.

Recirculate occurs on the low-to-high clock transition with the recirculate control low. The recirculate control must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control high. During recirculation, data is continuously available at the output and the data input is inhibited.

functional block diagram



3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{GG} (see Note 1) . . . . . −20 V to 0.3 V
Clock input voltage (see Note 1) . . . . . −20 V to 0.3 V
Data input voltage (see Note 1) . . . . . −20 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to a floating ground.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.5	5	5.5	V
High-level input voltage, V_{IH}	V_{SS} −1.8			V
Low-level input voltage, V_{IL}			V_{SS} −3.9	V
Clock pulse transition time; low-to-high level, $t_{TLH(\phi)}$		0.02	5	μs
Clock pulse transition time, high-to-low level, $t_{THL(\phi)}$		0.02	5	μs
Pulse width, clock high, $t_{w(\phi H)}$	300		∞	ns
Pulse width, clock low, $t_{w(\phi L)}$	100		1000000	ns
Recirculate pulse width, $t_{w(rec)}$	125			ns
Data setup time, $t_{su(da)}$	80			ns
Recirculate setup time, $t_{su(rec)}$	100			ns
Data hold time, $t_{h(da)}$	80			ns
Recirculate hold time, $t_{h(rec)}$	25			ns
Clock frequency, f_{ϕ}	0		2.5	MHz
Operating free-air temperature, T_A	−25		85	°C

electrical characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 0.2 mA		4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA				0.4	V
I_I	Input current (all inputs)	V_I = 0.8 V				–500	nA
I_{OS}	Short-circuit output current	V_O = 0 V,	V_{GG} = –11 V			–10	mA
I_{GG}	Supply current from V_{GG}	f = 2.5 MHz,	1 TTL load (see Note 2)		–22	–30	mA
P_D	Power dissipation	f = 2.5 MHz,	1 TTL load (see Note 2)		374	510	mW
C_i	Input capacitance, all inputs except clock	V_I = 5 V,	f = 1 MHz		3.5	5	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = 5 V,	f = 1 MHz		3.5	5	pF

† All typical values are at T_A = 25°C.

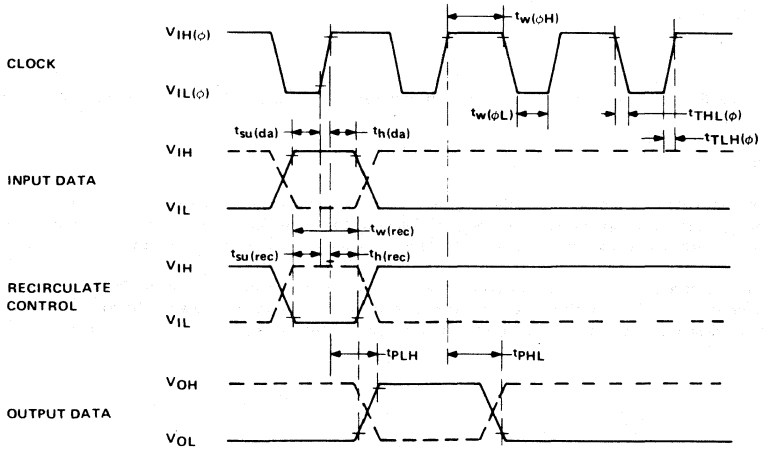
NOTE 2: For test purposes, a TTL load is simulated by a load of 2.7 kΩ and 20 pF between the output and V_{SS}.

switching characteristics under nominal operating conditions, T_A = –25°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	Load = 1 TTL gate (see Note 3)		250	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			250	ns

NOTE 3: For test purposes, a TTL load is simulated by a load of 2.7 kΩ and 20 pF between the output and V_{SS}.

voltage waveforms



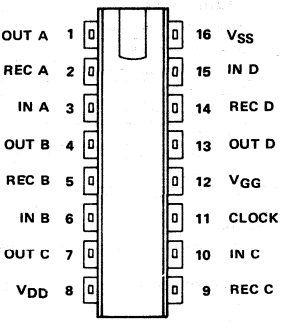
NOTE: All timing measurements are made at 10% or 90% points.

TMS 3409 JC, NC; TMS 3417 JC, NC
QUADRUPLE 80-, 64-BIT DYNAMIC SHIFT REGISTERS

BULLETIN NO. DL-S 7512266, MAY 1975

- 10-kHz to 5-MHz Operation
- Dynamic Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- On-Chip Recirculate Logic
- Power Supplies . . . 5 V, −12 V
- MOS Low-Threshold Self-Aligned-Gate Technology

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 3409 and TMS 3417 are quad 80-bit and quad 64-bit shift registers, respectively, with independent inputs, outputs, and recirculate controls for each register. A single external clock signal generates two internal clock phases to each register. The clock and all inputs can be driven from Series 74 TTL circuits and all outputs can drive TTL circuits without the use of external resistors.

P-channel enhancement-type low-threshold processing with self-aligned gates has been employed to reduce power dissipation and provide simple interfaces with bipolar circuits.

The TMS 3409 and TMS 3417 are offered in 16-pin dual-in-line ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

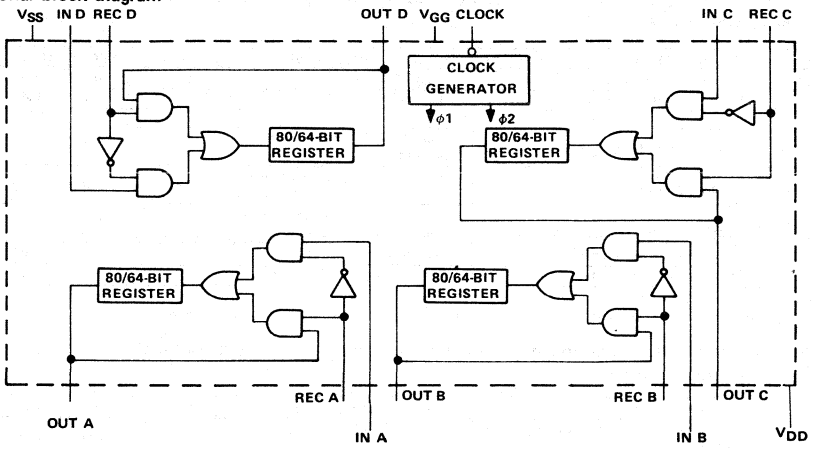
The TMS 3409 and TMS 3417 can be used in terminals, CRT displays, key-to-tape, key-to-disk, and card-punch applications.

operation

Transfer of data into and out of the shift register occurs on the high-to-low transition of the clock with output data becoming valid after a specified propagation delay following that transition. Input data must be set up a minimum time before the high-to-low transition and must be held for a minimum time after that transition.

Recirculate occurs on the high-to-low clock transition with the recirculate control high. The recirculate control level must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control low. During recirculation, data is continuously available at the outputs and data inputs are inhibited.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−20 V to 0.3 V
Data input voltage (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		0		V
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH}	V_{SS} −2		V_{SS}	V
High-level clock input voltage, $V_{IH(\phi)}$	V_{SS} −2		V_{SS}	V
Low-level input voltage, V_{IL}	0		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$	0		0.4	V
Pulse width, clock high, $t_{w(\phi H)}$	75		50000	ns
Pulse width, clock low, $t_{w(\phi L)}$	125		50000	ns
Data setup time, $t_{su(da)}$	50			ns
Recirculate setup time, $t_{su(rec)}$	200			ns
Data hold time, $t_{h(da)}$	50			ns
Recirculate hold time, $t_{h(rec)}$	100			ns
Clock frequency, f_{ϕ}	0.01		5	MHz
Operating free-air temperature, T_A	−25		85	°C

electrical characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 0.5 mA	V_{SS} –1	V_{SS} –0.5	V_{SS}	V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		0.3	0.4	V
I_I	Input current (all inputs)	V_I = 0			–100	nA
I_{GG}	Supply current from V_{GG}	Load = 1 TTL gate (see Note 2), f = 1 MHz		–10	–12	mA
I_{SS}	Supply current from V_{SS}	Load = 1 TTL gate (see Note 2), f = 1 MHz		33	47	mA
P_D	Power dissipation	Load = 1 TTL gate (see Note 2), f = 1 MHz		285	400	mW
C_i	Input capacitance, all inputs except clock	V_I = V_{SS}, f = 1 MHz			10	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = V_{SS}, f = 1 MHz			25	pF

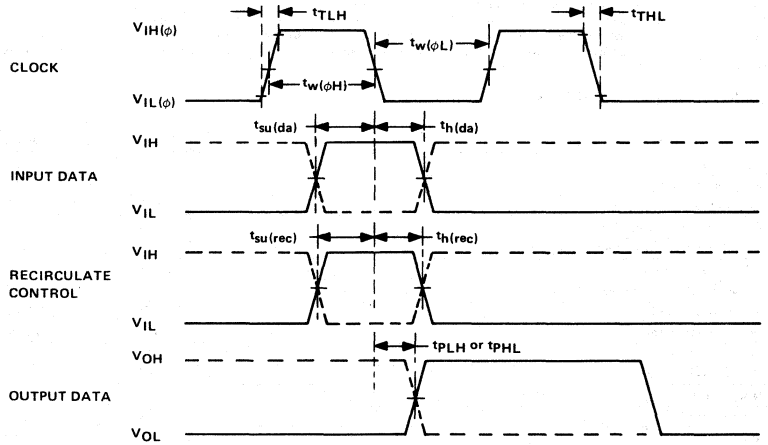
†All typical values are at T_A = 25°C.
NOTE 2: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF.

switching characteristics under nominal operating conditions, T_A = –25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	1 Series 74 TTL Load + 10 pF OR 10 MΩ + 10 pF (MOS Load) (see Note 3)		100	160	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			100	160	ns
t_{TLH}	Transition time, low-to-high-level output	1 Series 74 TTL Load + 10 pF (see Note 3)			60	ns
t_{THL}	Transition time, high-to-low-level output				50	ns

†All typical values are at T_A = 25°C.
NOTE 3: For final test purposes a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 10 MΩ and 10 pF. All loads are connected between output and V_{SS}.

voltage waveforms



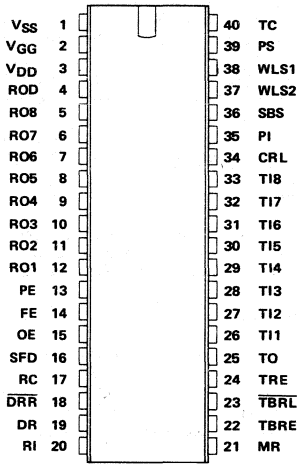
NOTE 3. All timings are with respect to 50% points of transitions with the exception of clock transition times, which are measured at 90% (high) and 10% (low).

TMS 6011 JC, NC
ASYNCHRONOUS DATA INTERFACE (UART)

BULLETIN NO. DL-S 7512275, MAY 1975

- Transmits, Receives, and Formats Data
- Full-Duplex or Half-Duplex Operation
- Operation from DC to 200 kHz
- Static Logic
- Buffered Parallel Inputs and Outputs
- Programmable Word Lengths . . . 5, 6, 7, 8 Bits
- Programmable Information Rate
- Programmable Parity Generation/Verification
- Programmable Parity Inhibit
- Automatic Data Formatting
- Automatic Status Generation
- 3-State Push-Pull Buffers
- Low-Threshold Technology
- Standard Power Supplies . . . 5 V, −12 V
- Full TTL Compatibility . . . No External Components

40-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 6011 JC, NC is an MOS/LSI subsystem designed to provide the data interface between a serial communications link and data processing equipment such as a peripheral or a computer. The device is often referred to as an asynchronous data interface or as a universal asynchronous receiver/transmitter (UART).

The receiver section of the TMS 6011 will accept serial data from the transmission line and convert it to parallel data. The serial word will have start, data, and stop bits. Parity may be generated and verified. The receiver section will validate the received data transmission by checking proper start, parity, and stop bits, and will convert the data to parallel.

The transmitter section will accept parallel data, convert it to serial form, and generate the start, parity, and stop bits.

The TMS 6011 is a fully programmable circuit allowing maximum flexibility of operation, defined as follows:

- The receiver and transmitter sections are separate and can operate either in full-duplex (simultaneous transmission and reception) or in half-duplex mode (alternate transmission and reception).
- The data word may be externally selected to be 5, 6, 7, or 8 bits long.
- Baud rate is externally selected by the clock frequency. Clock frequency can vary between 0 and 200 kHz.
- Parity, which is generated in the transmit mode and verified in the receive mode, can be selected as either odd or even. It is also possible to disable the parity bit by inhibiting the parity generation and verification.
- The stop bit can be selected as either a single- or a double-bit stop.
- Static logic is used to maximize flexibility of operation and to simplify the task of the user. The data holding registers are static and will hold a data word until it is replaced by another word.
- Asynchronous operation allows the use of a single transmission line. The clock period has to be within ±4% of 1/16 of the time for one bit for the transmitter and/or receiver but no phase relationship is required.

To allow for a wide range of possible configurations, three-state push-pull buffers have been used on all outputs except **Transmitter Output (TO)** and **Transmitter Register Empty (TRE)**. They allow the wire-OR configuration.

description (continued)

The TMS 6011 can be used in a wide range of data handling equipment such as modems, peripherals, printers, data displays, and minicomputers. By taking full advantage of the latest MOS/LSI design and processing techniques, it has been possible to implement the entire transmit, receive, and format function necessary for digital data communication in a single package, avoiding the cumbersome circuitry previously necessary.

P-channel enhancement-type low-threshold technology permits the use of standard power supplies (5 V, −12 V) as well as direct TTL interface. No external components are needed.

The TMS 6011 is offered in both 40-pin dual-in-line ceramic (JC suffix) and plastic (NC suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The device is characterized for operation from −25°C to 85°C.

operation

The operation can be best understood by visualizing the TMS 6011 as three separate sections: 1) common control, 2) transmitter, and 3) receiver. The transmitter and receiver sections are independent while the control section directs both receive and transmit.

common control section

The common control section will direct both the receiver and the transmitter sections.

The initialization of the TMS 6011 is performed through the **Master Reset (MR)** terminal. The **MR** terminal is strobed to a high level after power turn-on to reset all status and transmitter registers and to reset **Transmitter Output (TO)** to a high level. The **Receiver Outputs (RO1-RO8)** are not controlled by the **MR** terminal.

Status flags **Parity Error, Framing Error, Overrun Error, Data Ready,** and **Transmitter Buffer Register Empty** are disabled when the **Status Flags Disable (SFD)** is at a high level. When disabled, the status flags float (three-state buffers are in the high-impedance state). The **Transmitter Register Empty (TRE)** status flag is not a three-state output.

The number of bits per word is controlled by the **Word Length Select 1 (WLS1)** and **Word Length Select 2 (WLS2)** inputs. The word length may be 5, 6, 7, or 8 bits. Selection is as follows:

WORD LENGTH	WLS1	WLS2
5	Low	Low
6	High	Low
7	Low	High
8	High	High

The parity to be checked by the receiver and generated by the transmitter is determined by the **Parity Select (PS)** input. A high level on the **PS** input selects even parity and a low level selects odd parity.

The parity will not be checked or generated if a high level is applied to **Parity Inhibit (PI)**; in this case the stop bit or bits will immediately follow the data bit.

When a high level is applied to **PI**, the **Parity Error (PE)** status flag is brought to a low level indicating a no-parity error because parity is disregarded in this mode.

To select either one or two stop bits, the **Stop Bit(s) Select (SBS)** terminal is used. A high level at this terminal will result in two stop bits while a low level will produce only one.

To load the control bits (**WLS1, WLS2, PS, PI,** and **SBS**) a high level is applied to the **Control Register Load (CRL)** terminal. This terminal may be strobed or hard wired to a high level.

operation (continued)

transmitter section

The transmitter section will accept data in parallel form, then serialize, format, and transmit the data in serial form.

Parallel input data is received through the **Transmitter Inputs (TI1-TI8)**.

Serial output data is transmitted from the **Transmitter Output (TO)** terminal.

Input data is stored in the transmitter-buffer register. A low level at the **Transmitter Buffer Register Load ($\overline{\text{TBRL}}$)** command terminal will load a word in the transmitter-buffer register. The length of this word is determined by **Word Length Select 1 (WLS1)** and **Word Length Select 2 (WLS2)**. If a word of length greater than this appears at **TI8** through **TI1**, only the least significant bits are accepted. The word is justified into the least significant bit, **TI1**.

The data is transferred to the transmitter register when the $\overline{\text{TBRL}}$ terminal goes from low to high. The loading of the transmitter register is delayed if the transmitter section is presently transmitting data. In this case the loading of the transmitter register is delayed until the transmission has been performed.

Output serial data (transmitted from the **TO terminal**) is clocked out by **Transmitter Clock (TC)**. The clock rate is 16 times faster than the data rate.

The data is formatted as follows: start bit, data, parity bit, stop bits (1 or 2). Start bits, parity bits, and stop bits are generated by the TMS 6011. When no data is transmitted the output **TO** remains at a high level.

The start of transmission is defined as the transition of **TO** from a high to a low logic level.

Two flags are provided. A high level at the **Transmitter Buffer Register Empty (TBRE)** flag indicates that a word has been transferred to the transmitter/receiver and that the transmitter buffer register is now ready to accept a new word. A high level at the **Transmitter Register Empty (TRE)** flag indicates that the transmitter section has completed the transmission of a complete word including stop bits. The **TRE** flag will remain at a high level until the start of transmission of a new word.

Both the transmitter buffer register and the transmitter register are static and will perform long-term storage of data.

receiver section

The data is received in serial form at the **Receiver Input (RI)**. The data from **RI** enters the receiver register at a point determined by the character length, the parity, and the number of stop bits. **RI** must be maintained high when no data is being received. The data is clocked by the **Receiver Clock (RC)**. The clock rate is 16 times faster than the data rate.

Data is transferred from the receiver register to the receiver buffer register. The output data is then presented in parallel form at the eight **Receiver Outputs (RO1** through **RO8)**. The MOS output buffers used for the eight **RO** terminals are three-state push-pull output buffers that permit the wire-OR configuration through use of the **Receiver Output Disable (ROD)** terminal. When a high level is applied to **ROD** the **RO** outputs are floating. If the word length is less than 8 bits, the most significant bits will be at a low level. The output word is right justified. **RO1** is the least significant bit and **RO8** is the most significant bit.

A low level applied to the **Data Ready Reset ($\overline{\text{DRR}}$)** terminal resets the **Data Ready (DR)** output to a low level.

Several flags are provided in the receiver section. There are three error flags (**Parity Error, Framing Error,** and **Overrun Error**) and a **DR** flag. These status flags may be disabled by a high level at the **Status Flags Disable (SFD)** terminal.

A high level at the **Parity Error (PE)** terminal indicates an error in parity.

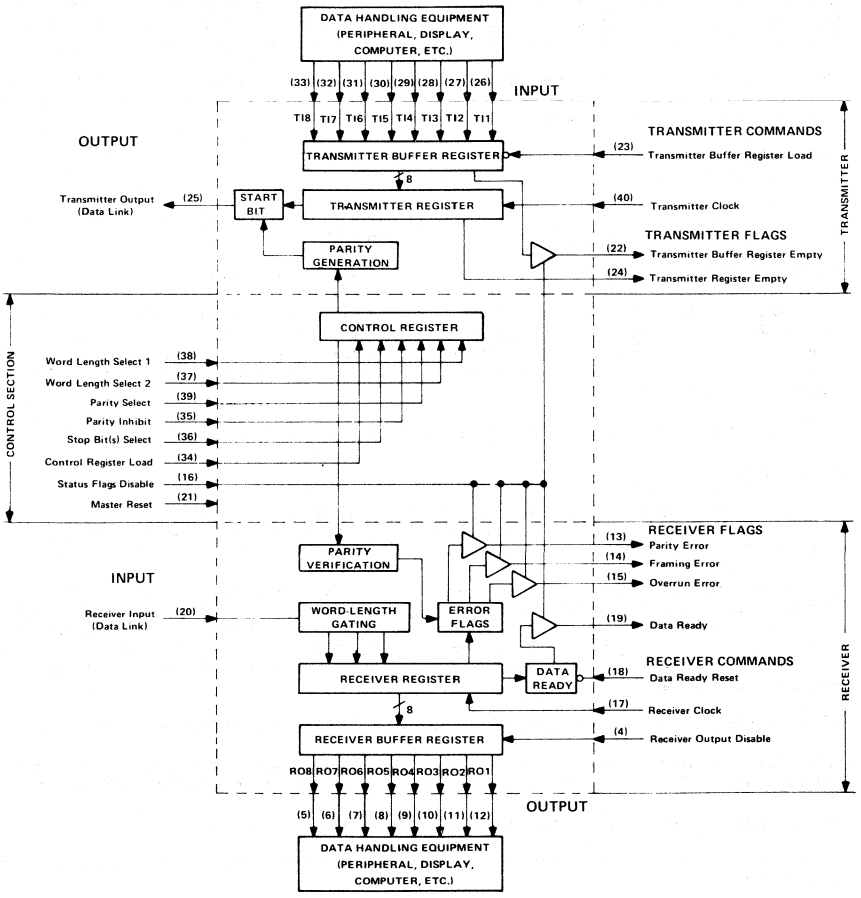
A high level at the **Framing Error (FE)** terminal indicates a framing error that is an invalid or nonexistent stop bit in the received word.

operation (continued)

A high level at the **Overrun Error (OE)** terminal indicates an overrun. An overrun occurs when the previous word has not been read, i.e., when the **DR** output has not been reset before the present data was transferred to the receiver buffer register.

A high level at the **DR** terminal indicates that a word has been received, stored in the receiver-buffer register and that the data is available at outputs **RO1** through **RO8**. The **DR** terminal can be reset through the $\overline{\text{DRR}}$ terminal.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Input voltage (any input) (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}			0		V
Supply voltage, V_{GG}		−11.5	−12	−12.5	V
Supply voltage, V_{SS}		4.75	5	5.25	V
High-level input voltage, all inputs, V_{IH} (see Notes 2 and 3)		V_{SS} −1.5		V_{SS} +0.3	V
Low-level input voltage, all inputs, V_{IL} (see Notes 2 and 3)		−12		0.8	V
Pulse width, t_w	Clock	2.5			μs
	Transmitter buffer register load	400			ns
	Control register load	250			ns
	Parity inhibit (see Notes 4 and 5)	400			ns
	Parity select (see Notes 4 and 5)	300			ns
	Word length select and stop bit select (see Notes 4 and 5)	300			ns
	Master reset	1.5			μs
	Data ready reset	250			ns
Data setup time, $t_{su(da)}$		10↓			ns
Data hold time, $t_{h(da)}$		20↑			ns
Clock frequency, f_ϕ (see Note 6)		0		200	kHz
Operating free-air temperature, T_A		−25		85	°C

NOTES: 2. All data, clock, and command inputs have internal pull-up resistors to allow direct clocking by any TTL circuit.
3. The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.
4. Inputs to PI, PS, WLS1, WLS2, and SBS are normally static signals. A minimum pulse width has been indicated for possible pulsed operation.
5. All control signal pulses should be centered with respect to CRL to ensure maximum setup and hold time.
6. Clock frequency is 16 times the baud rate.

↑↓The arrow indicates the edge of the $\overline{TBRL}$ pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −200 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.6	V
I_{IH}	High-level input current, all inputs	V_I = 5 V			10	μA
I_{IL}	Low-level input current, all inputs	V_I = 0 V			−1.6	mA
I_{GG}	Supply current from V_{GG}	All inputs at a high level		−7	−12	mA
I_{SS}	Supply current from V_{SS}	All inputs at a high level		20	30	mA
P_D	Power dissipation	All inputs at a high level		190	300	mW
C_i	Input capacitance, all inputs	V_I = V_{SS}, f = 1 MHz		10	20	pF

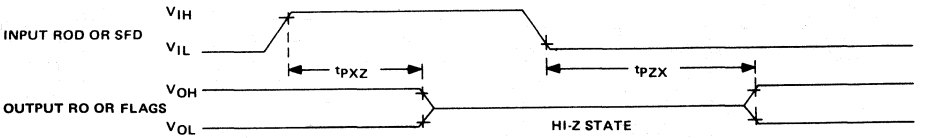
†All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (unless otherwise noted)

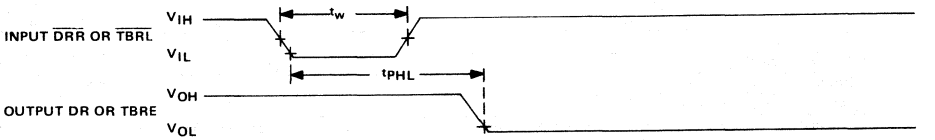
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level DR output from $\overline{DRR}$	1 Series 74 TTL load		800	1000	ns
t_{PHL}	Propagation delay time, high-to-low level TBRE output from $\overline{TBRL}$			800	1000	ns
t_{PZX}	Enable time, receiver output from ROD			300	500	ns
t_{PXZ}	Disable time, receiver output from ROD			300	500	ns
t_{PZX}	Enable time, outputs PE, FE, OE, DR, or TBRE from SFD			300	500	ns
t_{PXZ}	Disable time, outputs PE, FE, OE, DR, or TBRE from SFD			300	500	ns

† All typical values are at $T_A = 25°C$ and nominal voltages.

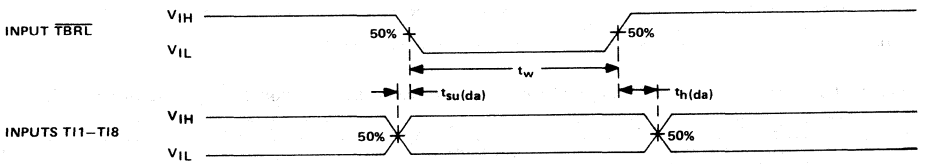
voltage waveforms



ENABLE AND DISABLE TIMES



PROPAGATION DELAY TIMES

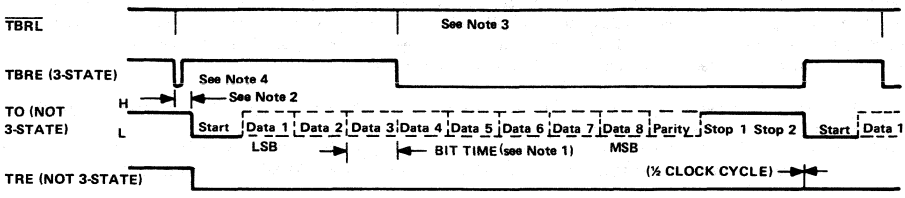


DATA SETUP AND HOLD TIMES

NOTE: All enable, disable, and propagation delay times are referenced to the 90% or 10% points. All pulse widths are referenced to the 50% points.

operation timing diagram

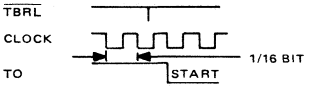
TRANSMITTER TIMING†



† Transmitter initially assumed inactive at start of diagram, shown for 8 level code and parity and 2 stops.

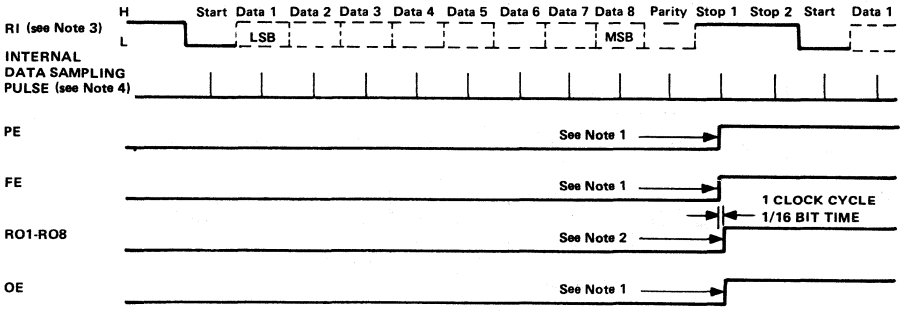
NOTES: 1. Bit time is 16 clock cycles.

2. If transmitter is inactive the start pulse will appear on line within one clock cycle of time data strobe occurs (see detail below).



3. Because transmitter is double buffered, another data strobe can occur anywhere during transmission of character 1.
4. TBRE goes to a low for a period of approximately one clock cycle following a $\overline{\text{TBRL}}$ pulse.

RECEIVER TIMING



NOTES: 1. This is the point at which the error condition is detected, if error occurs.

2. A high-to-low transition on the DR pin indicates that the contents of the receiver register has been transferred to the receiver buffer register and that the three error-flag signals are valid. Output data remains valid until the next word is transferred into the receiver buffer register.
3. The RI waveform illustrates an eight-bit word with parity and two stop bits. If parity is inhibited, the stop bits immediately follow the last data bit. For all word lengths, the data in the buffer register must be right justified, i.e., RO1 (pin 12) is the least significant bit.
4. Data sampling occurs at the center of each data bit (8 clock cycles after the beginning of the bit).

MOS MEMORY SYSTEM COMPATIBILITY

1) POWER SUPPLIES

In P-channel MOS Memories the substrate is normally biased positive with respect to the drain or source nodes. The substrate bias is normally negative for N-channel devices. In order to provide compatible interfaces with bipolar integrated circuits, power supply voltages are translated for most MOS Memory devices of recent design to maintain the recommended substrate bias conditions and to provide input and output voltage levels between ground (0 volts) and V_{CC} (+5 volts), the standard system supply voltage in equipment using TTL integrated circuits.

The chart below shows the recommended supply voltages for the MOS Memory devices in this catalog along with the symbols used for the various supply terminals.

MOS MEMORY NOMINAL POWER SUPPLY VOLTAGES AND TERMINAL SYMBOLOGY

TECHNOLOGY	P-CHANNEL METAL GATE	N-CHANNEL SILICON GATE		
SUPPLY VOLTAGE				
12 V			V_{DD}	V_{DD}
7 V				
5 V	V_{SS}	V_{CC}		V_{CC}
0	V_{DD}	GND	V_{SS}	V_{SS}
−3 V				
−5 V			V_{BB}	V_{BB}
−12 V	V_{GG}			
PRODUCT TYPE	Static and dynamic shift registers, ROM's, UART	Static RAM's	4K Dynamic RAM's	ROM
TYPE NUMBERS	TMS 3101 thru TMS 3409 (all S/R's) TMS 4800 TMS 4103 TMS 6011	TMS 4033 TMS 4034 TMS 4035 TMS 4036 series TMS 4039 series TMS 4042 series TMS 4043 series	TMS 4030 series TMS 4050 series TMS 4051 series TMS 4060 series	TMS 5400

2) INPUT COMPATIBILITY

Figure 1 illustrates how Series 74 TTL circuits are specified to guarantee that any Series 74 circuit will drive or can be driven by any other Series 74 circuit. The 0.4-volt difference in output and input specifications is called the noise margin. These margins guarantee that any Series 74 circuit is compatible with any other Series 74 circuit and that the probability of false data inputs from spurious switching transients or induced voltage levels is minimized.

SERIES 74 TTL INPUT AND OUTPUT SPECIFICATIONS

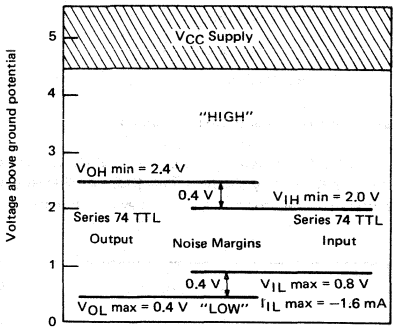
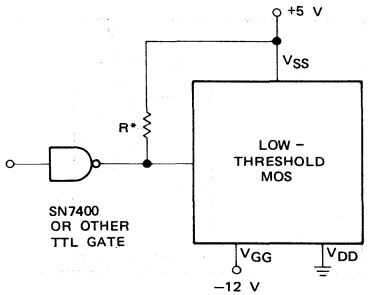


FIGURE 1

All TI shift registers and most ROM's and RAM's are designed with inputs that can be driven directly without level-shifter or amplifier circuits. The phrase "fully TTL-compatible" has been used to indicate that a MOS Memory device will drive or be driven by Series 74 circuits with adequate noise margins without the use of external pull-up or pull-down components. Some P-channel MOS Memories require a pull-up resistor on the input to meet the minimum input voltage high level, V_{IH} min. Figure 2 illustrates the interface with TTL. In all cases, the input of the MOS circuit has a very high impedance. Therefore, TTL input compatibility is easily achieved.



*The value of the R resistor varies depending on speed-power requirements. In many cases this resistor is diffused on the MOS chip. For low-threshold MOS the resistor assures that the worst-case TTL output is pulled up to at least 3.5 V for proper MOS circuit operation.

FIGURE 2

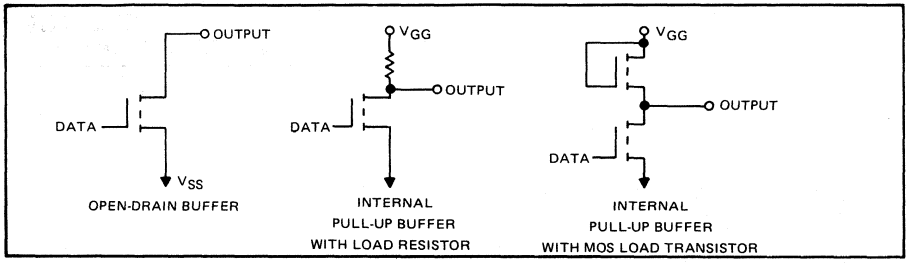
3) OUTPUT COMPATIBILITY

Three types of buffers are commonly used on MOS devices:

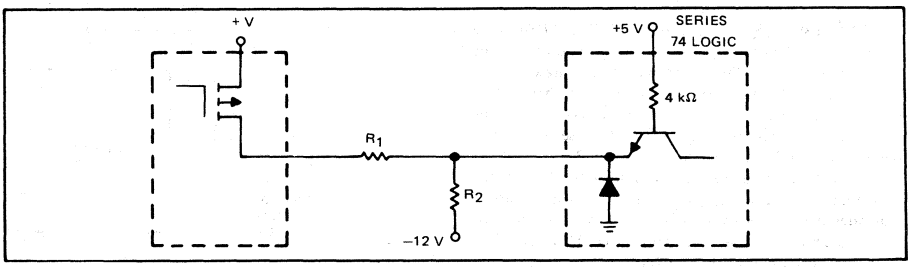
- Open-drain
- Internal pull-up
- Push-pull

a) Open-drain and internal pull-up

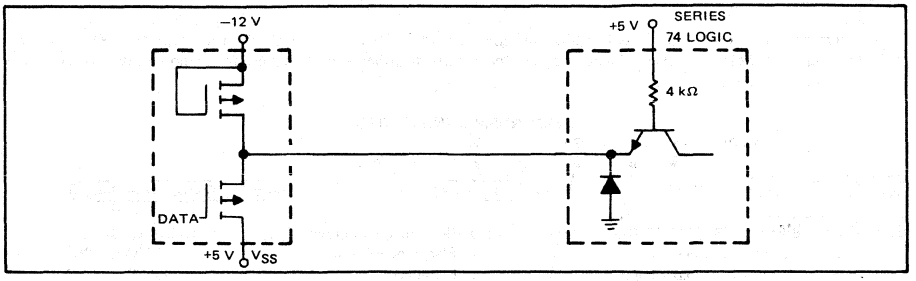
The buffer is simply a current switch. In the "off" state the impedance of the buffer is extremely large, while in the "on" state it is typically under 1 kΩ. A discrete resistor or an MOS transistor may be used as a load with an open-drain buffer. This resistor or transistor may be internal to the MOS circuit.



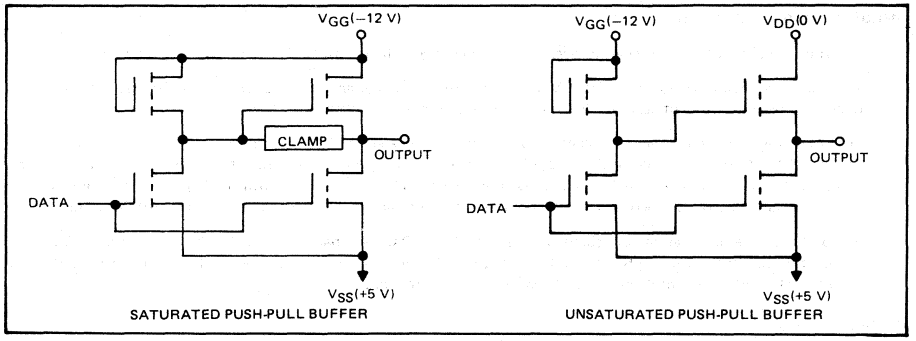
In every case compatibility with MOS is easily achieved. For instance, for an open-drain buffer with MOS:



R_2 provides the necessary current sink for the TTL input; R_1 is sometimes used to limit power dissipation or the positive excursion of the TTL input to +5 V. If R_2 is on the chip, no external components may be necessary.



Two types are common. The unsaturated push-pull buffer is the most commonly used for low-threshold circuits since the smaller drain-source voltage permits the upper output transistor to operate in the unsaturated or low-resistance region of the I_D vs V_{DS} characteristic curve. As a result, the output voltage swings near V_{DD} without going negative and permits direct TTL compatibility without external components.



4) CLOCKS

Depending on the circuit type, there are different clock requirements:

No clocks – Static RAMs, ROMs, etc.
1 clock – with other clocks generated internally
2 clocks – most dynamic shift registers

a) One external clock

An internal circuit generates the clocks from a single outside clock signal. The outside clock signal has the same swing as the data input signal and the compatibility is identical (see preceeding paragraph 3).

Single-clock low-threshold MOS circuits will accept a TTL clock without adding components.

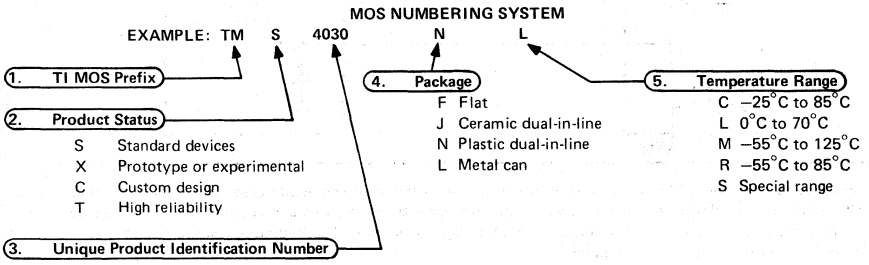
b) Two or four clocks

The clock signals must swing between V_{SS} and V_{GG}. To go from a single-TTL-level clock to a multiple-MOS-level clock, two circuits are required: 1) a clock generator to generate the necessary clock pulses, and 2) a clock driver to bring the clock levels to the required values. In most cases only one clock circuit is needed for an entire MOS LSI system.

MOS LSI MECHANICAL DATA

general

Electrical characteristics presented in this catalog, unless otherwise noted, apply for circuit type(s) listed in the page heading, regardless of package. Factory orders for circuits described should include the complete part-type numbers listed on each page.



3

manufacturing information

Alloying is performed in an inert atmosphere. A silicon gold eutectic is formed during the alloying operation.

Thermal compression bonding is used. Typical bond strength is 5 grams. Bond strength is monitored on a lot-to-lot basis. Any bond strength of less than 2 grams causes rejection of the entire lot of devices.

TI uses a low-temperature alloy brazing to seal ceramic packages. Metal-can packages are welded. Glass leaks are eliminated by testing in a fluorocarbon solution heated to 150°C. Fine-leak elimination is performed through mass spectrometer techniques. All MOS LSI devices produced by TI are capable of withstanding 5×10^{-7} ppm fine-leak inspection, and may be screened to 5×10^{-8} ppm fine leak, if desired by the customer, for special applications.

All packages are capable of withstanding a shock of 3,000 G. All packages are capable of passing a 20,000-G acceleration (centrifuge) test in the Y axis. Pin strength is measured by a pin-shearing test. All pins are able to withstand the application of a force of 6 pounds at 45° in the peel-off direction.

dual-in-line packages

A pin-to-pin spacing of 100 mils has been selected for all dual-in-line packages.

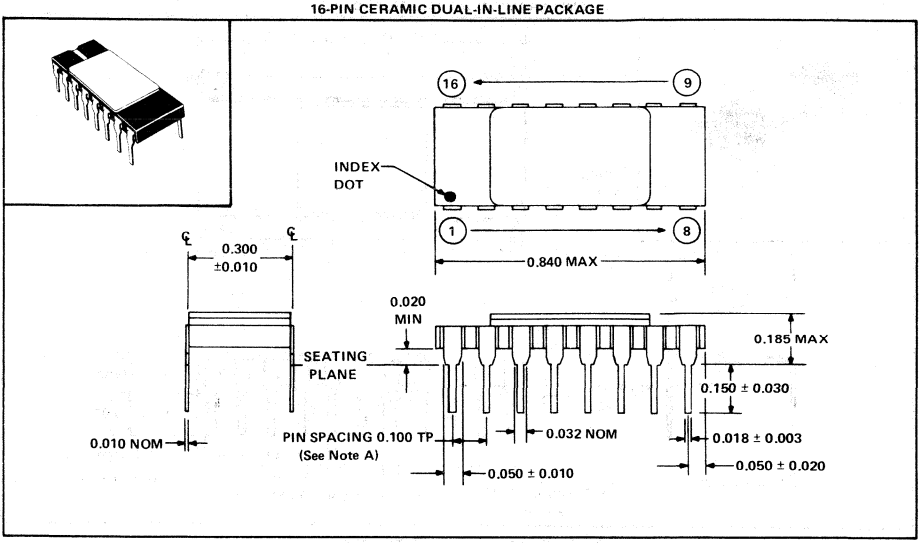
TI uses several hermetically sealed ceramic dual-in-line packages, each of which consist of a ceramic base, plated metal cap, and tin-plated leads.

The following dual-in-line packages are available in plastic or ceramic:

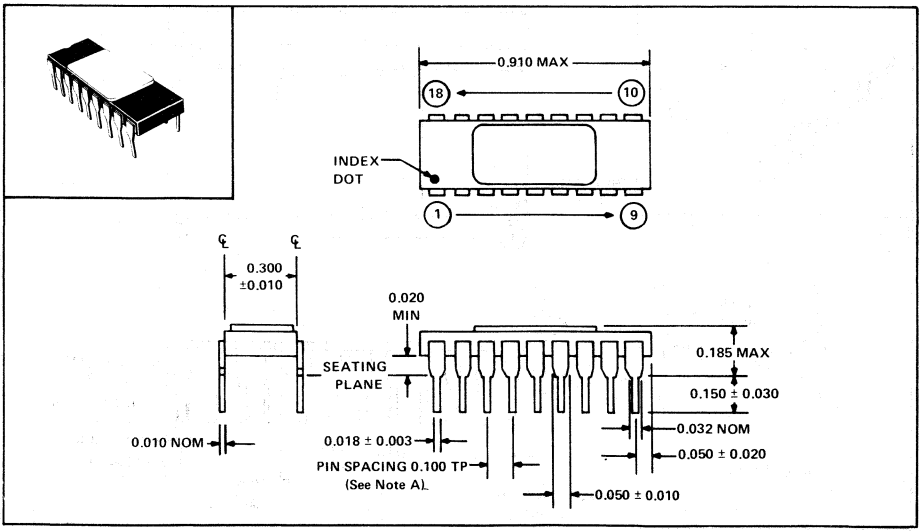
	8 PIN	10 PIN	16 PIN	18 PIN	22 PIN	24 PIN	28 PIN	40 PIN
300 mils between rows	X†	X†	X	X				
400 mils between rows					X	X†		
600 mils between rows						X	X	X

† There are no products shown in this data book in the 8-pin ceramic package or the ceramic or plastic 10-pin or 24-pin, 400-mil package.

16-PIN CERAMIC DUAL-IN-LINE PACKAGE

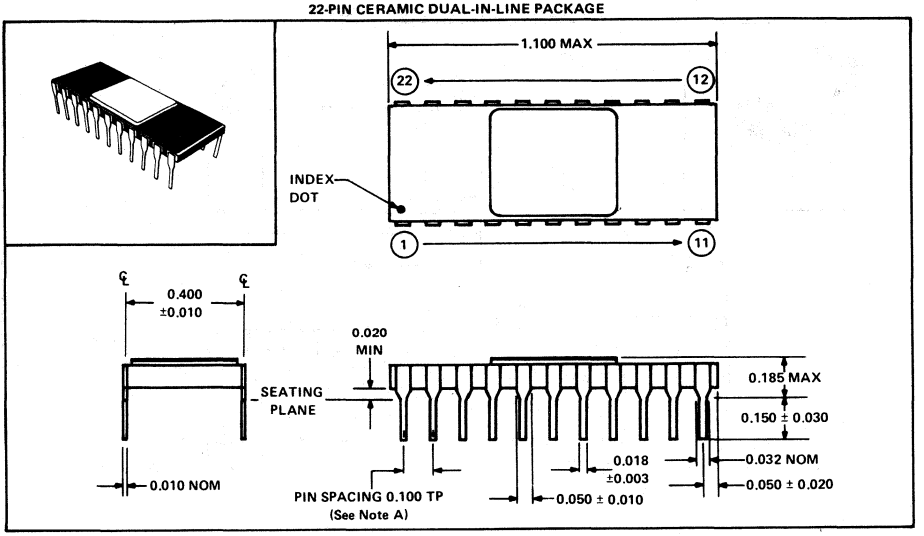


18-PIN CERAMIC DUAL-IN-LINE PACKAGE

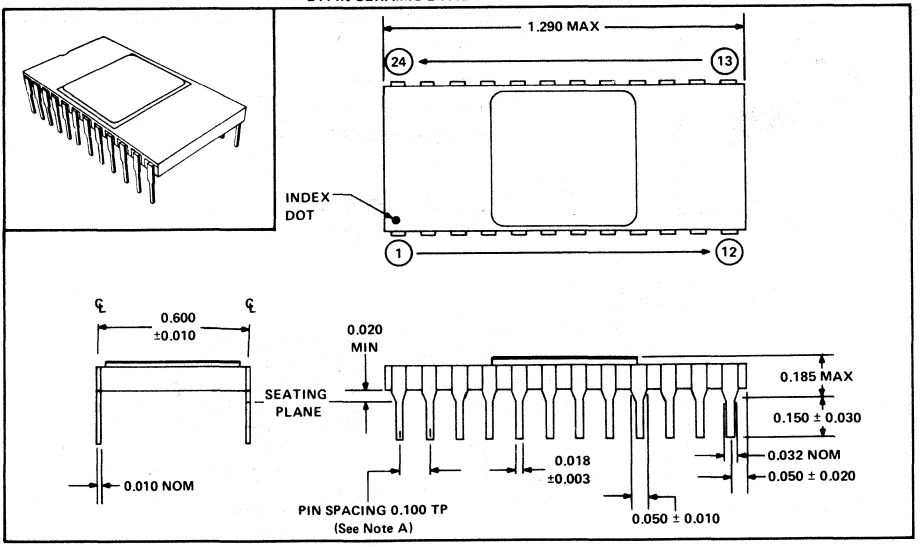


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

22-PIN CERAMIC DUAL-IN-LINE PACKAGE

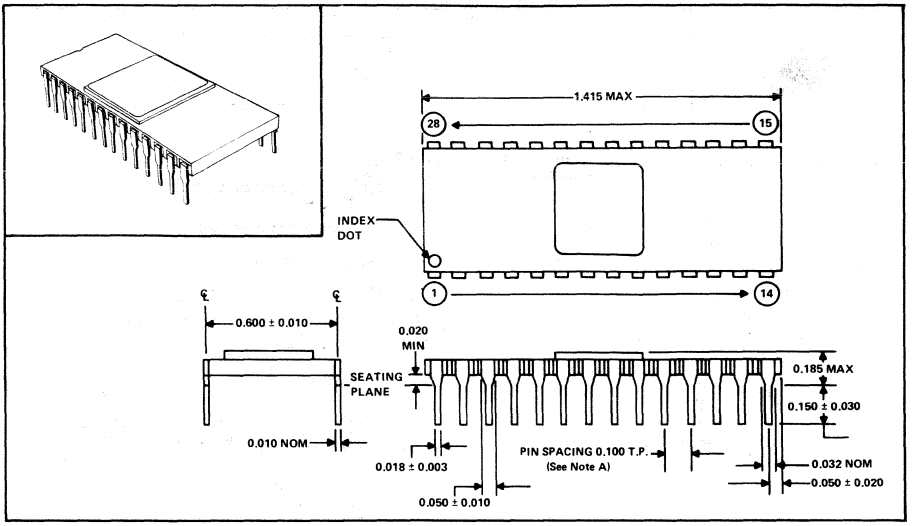


24-PIN CERAMIC DUAL-IN-LINE PACKAGE

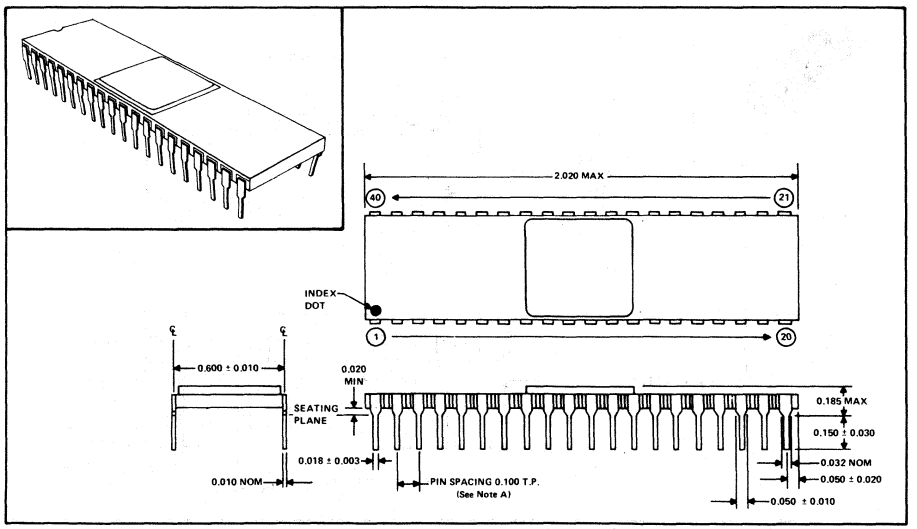


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

28-PIN CERAMIC DUAL-IN-LINE PACKAGE

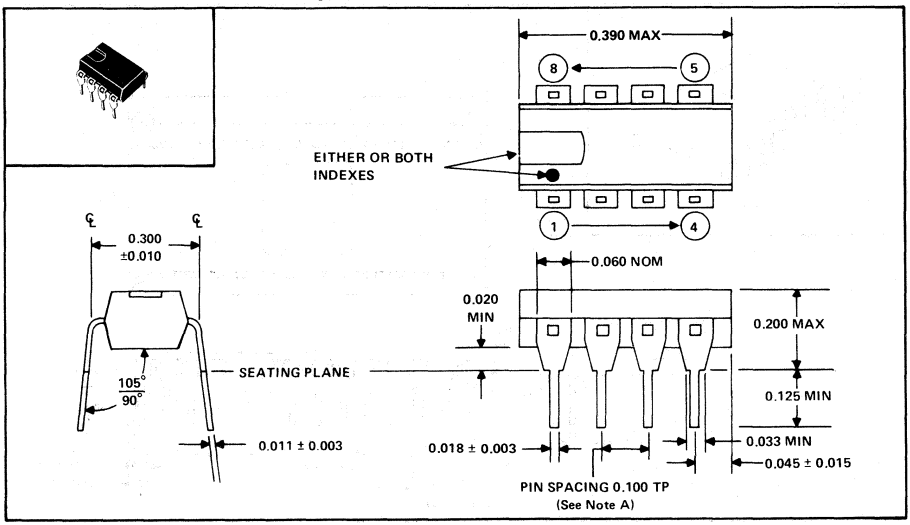


40-PIN CERAMIC DUAL-IN-LINE PACKAGE

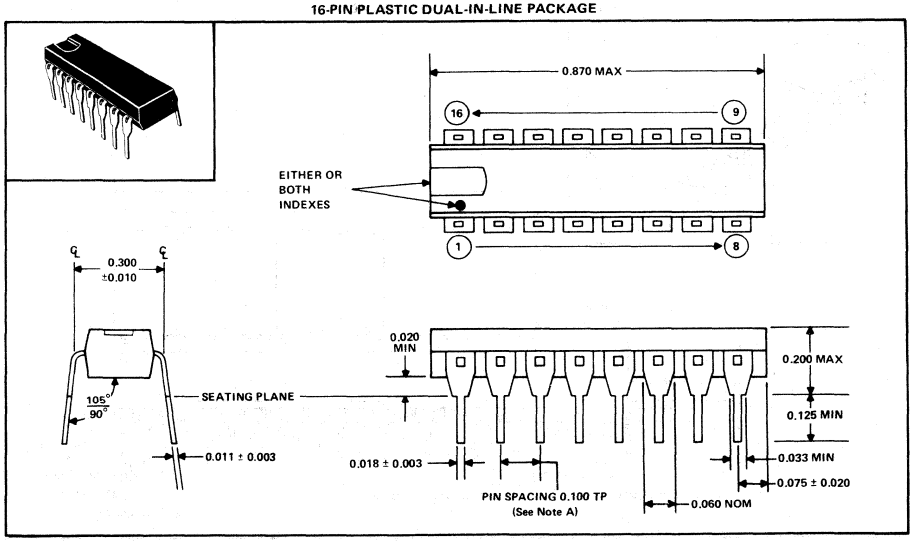


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

8-PIN PLASTIC DUAL-IN-LINE PACKAGE

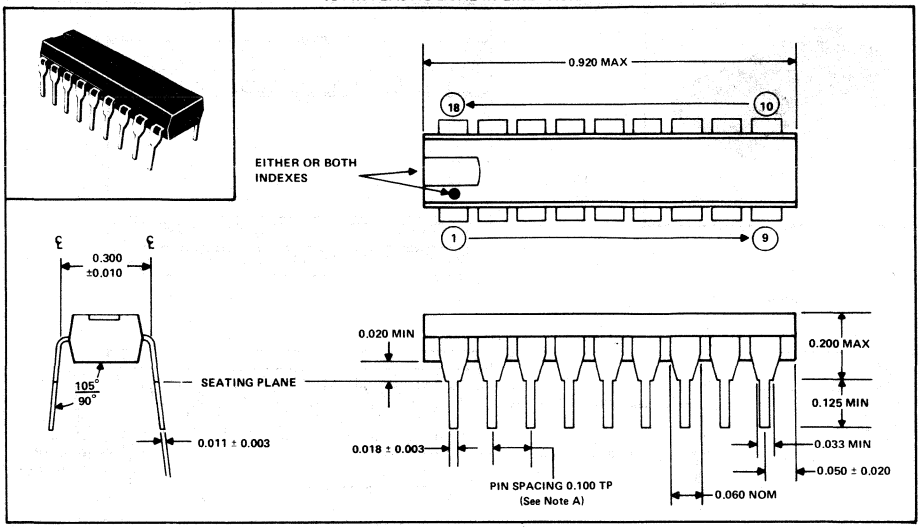


16-PIN PLASTIC DUAL-IN-LINE PACKAGE

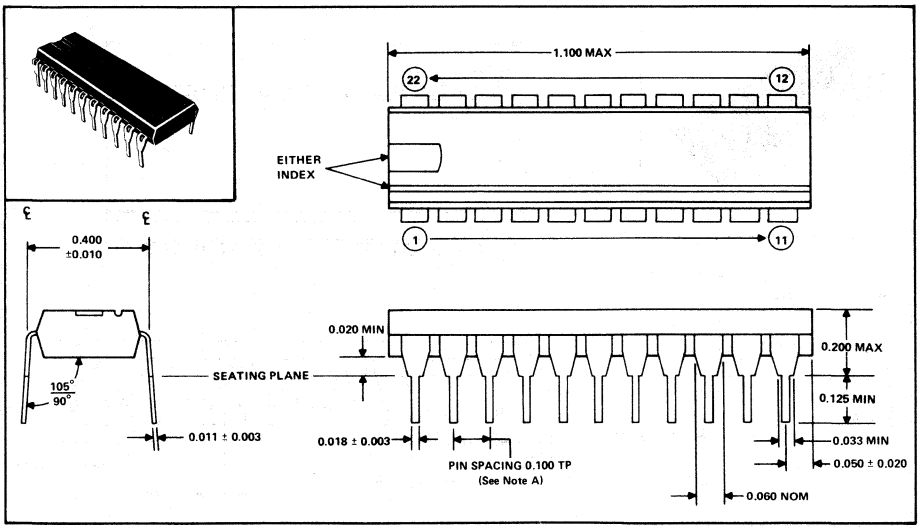


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

18-PIN PLASTIC DUAL-IN-LINE PACKAGE



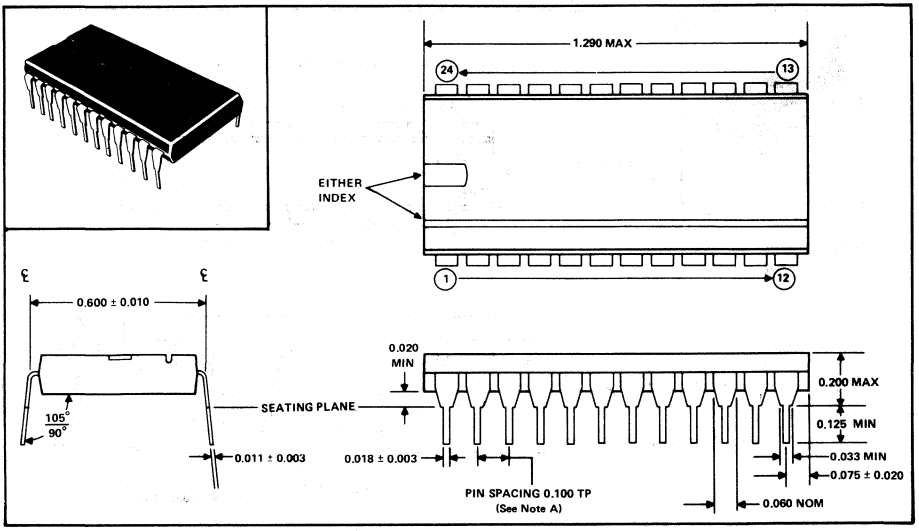
22-PIN PLASTIC DUAL-IN-LINE PACKAGE



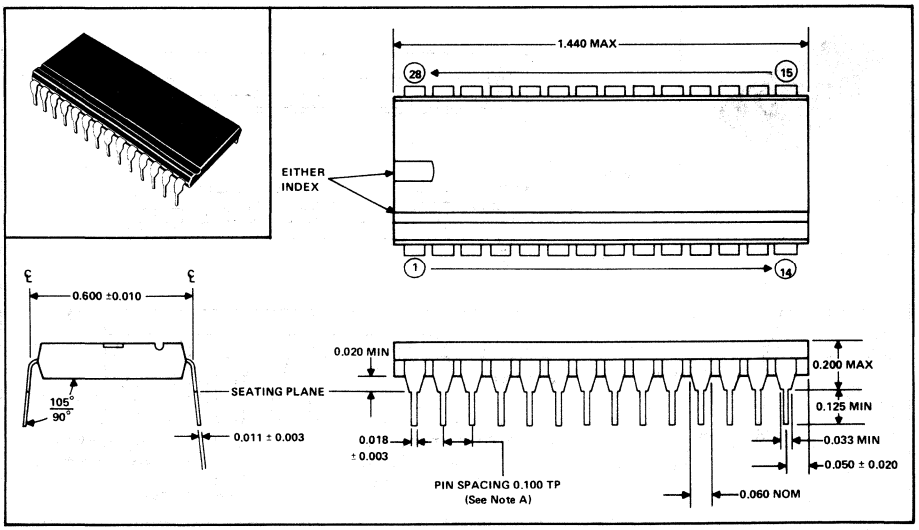
NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

MOS LSI MECHANICAL DATA

24-PIN PLASTIC DUAL-IN-LINE PACKAGE

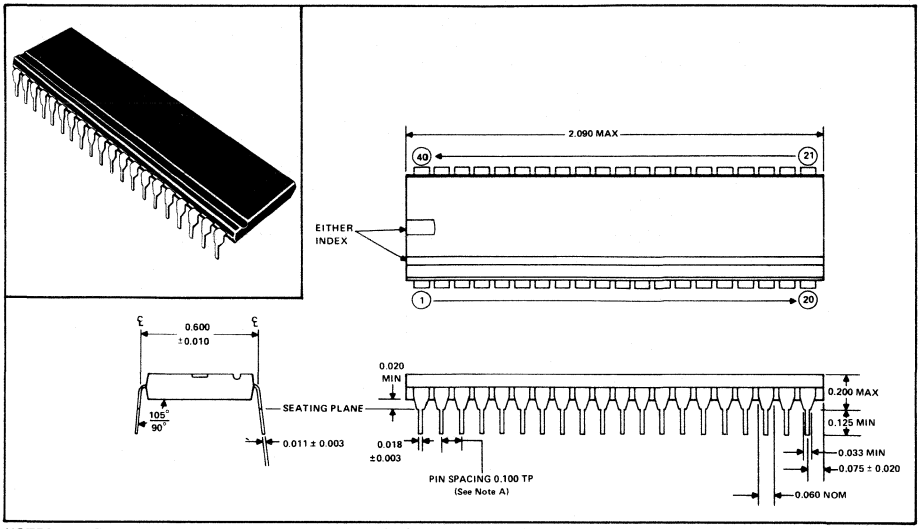


28-PIN PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

40-PIN PLASTIC DUAL-IN-LINE PACKAGE

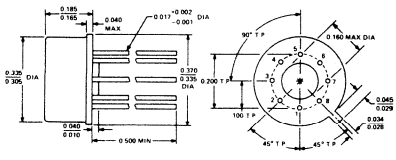


NOTES: A. Each pin centerline is located within 0.010 of its true longitudinal position.
B. All linear dimensions are in inches.

metal-can

For devices such as shift registers requiring few inputs and outputs, TI uses two metal-can packages.

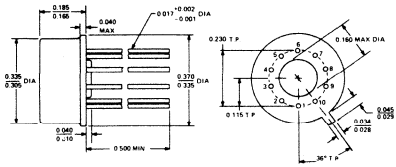
8-PIN METAL CAN



ALL DIMENSIONS ARE IN INCHES
UNLESS OTHERWISE SPECIFIED

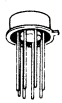
Same as JEDEC TO-99 and MO-002AK except for diameter of standoff

10-PIN METAL CAN



ALL DIMENSIONS ARE IN INCHES
UNLESS OTHERWISE SPECIFIED

Same as JEDEC TO-100 and MO-006AD except for diameter of standoff



Dynamic RAM Interface Circuits

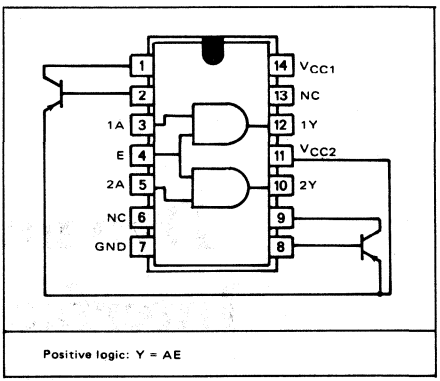
SN75322
DUAL TTL-TO-MOS DRIVER

DECEMBER 1975

4K RAM CHIP ENABLE DRIVER

- Dual Positive-Logic and TTL-to-MOS Driver
- Versatile Interface Circuit for use between TTL and High-Current, High-Voltage Systems
- Operates from Standard Bipolar and MOS Supply Voltages
- High Speed Switching
- TTL and DTL Compatible Inputs
- Separate Driver Address Inputs with Common Strobe
- V_{OH} and V_{OL} Compatible with TMS4030 4K RAM and Other Popular MOS RAMs
- No 12 Volt Supply Current (except leakage) when Output in Low State
- Low 5 Volt Supply Current when Output in Low State
- Output in High Impedance State Upon Loss of 5 Volt Supply
- Requires 2 External PNPs per Package for Operation

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



Positive logic: Y = AE

RECOMMENDED PNP TRANSISTOR
A5T4260 or A5T4261 (Plastic)
or
2N5771 – (Plastic)
or
MM4208A – (Metal Can)

description

The SN75322 is a monolithic integrated Dual TTL-to-MOS driver and interface circuit. The device has separate driver address inputs with common strobe. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. The SN75322 is designed for driving N-Channel RAMs where low power dissipation is desirable when the driver output is in the low state. Specifically, it may be used to drive the chip-enable clock of the TMS4030/50/60 MOS RAMs.

The SN75322 requires two external PNP transistors per package. Suggested PNP transistors are: A5T4260/61, 2N5771, MM4208A.

The SN75322 operates from the TTL 5 volt supply and the MOS V_{DD} supply. With the use of an external pull-down resistor, the driver output of the SN75322 will be forced to the low state upon loss of the 5 volt supply.

The SN75322 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

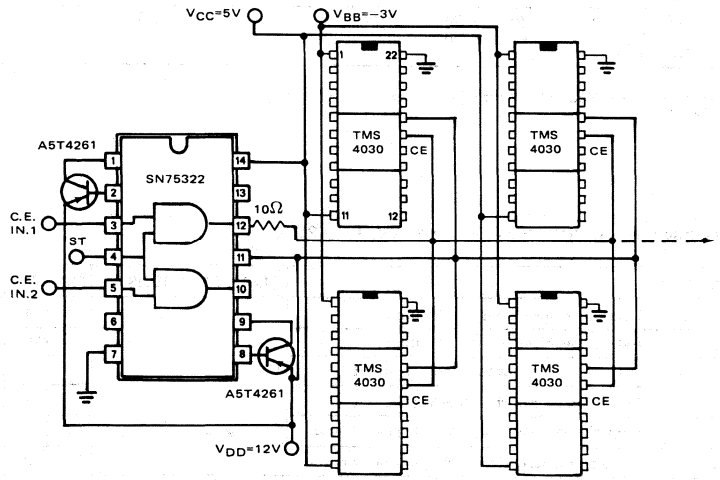
Supply voltage range of V_{CC1} (See Note 1)	−0.5V to 7V
Supply voltage range of V_{CC2}	−0.5V to 15V
Input voltage	5.5V
Inter-input voltage (See Note 2)	5.5V
Continuous total dissipation at (or below) 25°C free-air temperature	1000mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 60 seconds: N package	260°C

Notes: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between any two inputs of any one of the gates.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	12	15	V
Operating free-air temperature, T_A	0		70	°C

SN75322 DRIVING THE TMS4030 MEMORY -- ONLY FOUR TMS4030s SHOWN



NOTE: External PNP Transistor should be located as close as possible to the SN75322.
Recommended minimum load: 200pF

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

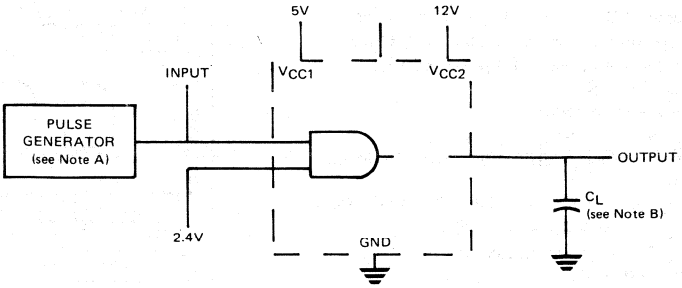
PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{IH} = 2.0V, I_{OH} = −400μA			V_{CC2}−0.25		V
V_{OL}	Low-level output voltage	V_{CC2} = 11.4V, V_{IN} = 0.8V, I_{OL} = 10mA			0.23	0.5	V
I_I	Input current at maximum input voltage	V_{CC1} = 5.25V V_{CC2} = 11.4V, V_I = 5.25V				1	mA
I_{IH}	High-level input current	V_I = 2.4V	A inputs			40	μA
			E input			80	
I_{IL}	Low-level input current	V_I = 0.4V	A inputs		−1	−1.6	mA
			E input		−2	−3.2	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	V_{CC1} = 5.25V, V_I = 0V V_{CC2} = 12.6V, No Load			15.0	20	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low	V_{CC1} = 4.75, V_I = 0V V_{CC2} = 12.6V No Load			.01	5	mA
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	V_{CC1} = 5.25V, V_I = 5.0V V_{CC2} = 12.6V, No Load			24	34	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high	V_{CC1} = 4.75V, V_I = 5.0V V_{CC2} = 12.6V, No Load			9.5	13	mA

†All typical values are at V_{CC1} = 5V, V_{CC2} = 12V and T_A = 25°C unless otherwise noted.
*V_{CC2}−0.5

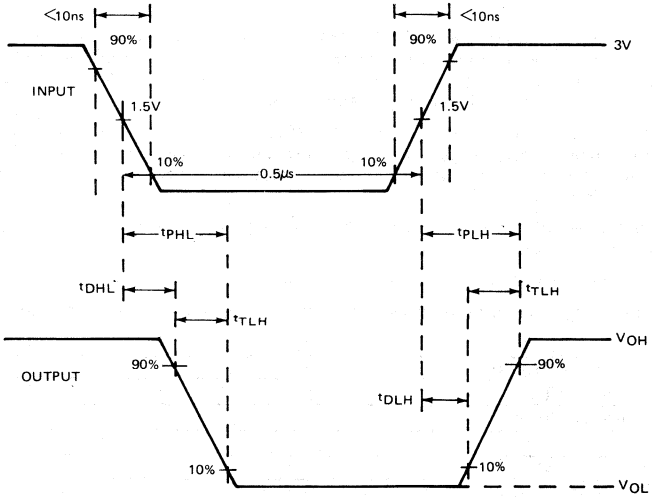
switching characteristics, V_{CC1} = 5V, V_{CC2} = 12V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 300pF See Figure 1		14	21	ns
t_{DHL}	Delay time, high-to-low-level output			16	24	ns
t_{TLH}	Transition time, low-to-high-level output			11	17	ns
t_{THL}	Transition time, high-to-low-level output			13	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output		12	25	38	ns
t_{PHL}	Propagation delay time, high-to-low-level output		14	29	44	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING TIMES, EACH DRIVER

NOTES: A. The pulse generator has the following characteristics: PRR = 1MHz, Z_{out} = 50Ω
B. C_L includes probe and jig capacitance

SN75363
DUAL TTL-TO-MOS DRIVER

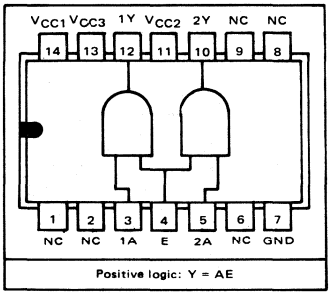
DECEMBER 1975

4K RAM CHIP ENABLE DRIVER

- Dual Positive-Logic and TTL-to-MOS Driver
- Versatile Interface Circuit for use between TTL and High-Current, High-Voltage systems
- Capable of Driving High Capacitance Loads
- Compatible with many popular MOS RAMs
- Operates from Standard Bipolar and MOS Supply Voltages
- High-Speed Switching
- TTL and DTL Compatible Inputs
- Separate Driver Address Inputs with Common Strobe
- V_{CC2} Supply Voltage Variable Over Wide Range
- V_{CC3} Supply Voltage Pin Available
- V_{CC3} Pin can be connected to V_{CC2} Pin in some applications
- Damping Resistor eliminates Undesired Output Transient Overshoot

  Transient Overdrive improves Fall Time

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75363 is a monolithic integrated Dual TTL-to-MOS driver and interface circuit. The device accepts standard TTL and D TL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive the chip-enable clock input of the TMS4030/50/60 MOS RAMs and the address, control and timing inputs for several other types of MOS RAMs.

The SN75363 operates from the TTL 5-volt supply and the MOS V_{SS} and V_{DD} supplies. This device has been optimized for operation with V_{CC2} supply voltage from 11 volts to 15 volts and with nominal V_{CC3} supply voltage from 3 to 4 volts higher than V_{CC2}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

A small series damping resistor has been included in the design to eliminate undesired output transient overshhot due to load or wiring inductance.

The SN75363 is characterized for operation from 0° C to 70° C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5V to 7V
Supply voltage range of V_{CC2}	−0.5V to 16V
Supply voltage range of V_{CC3}	−0.5V to 19V
Input voltage	5.5V
Inter-input voltage (see Note 2)	5.5V
Continuous total dissipation at (or below) 25°C free-air temperature	1300mW
Operating temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 60 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between any two inputs of any one of the gates.

TEXAS INSTRUMENTS

recommended operating conditions

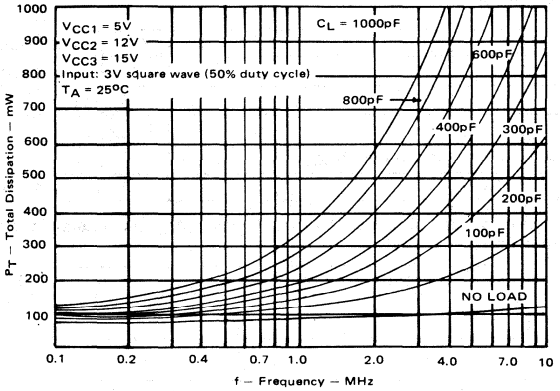
	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	12	15	V
Supply voltage, V_{CC3}	V_{CC2}	15	18	V
Voltage difference between supply voltages: $V_{CC3} - V_{CC2}$	0	3		V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3}, and operating free-air temperature (unless otherwise noted)

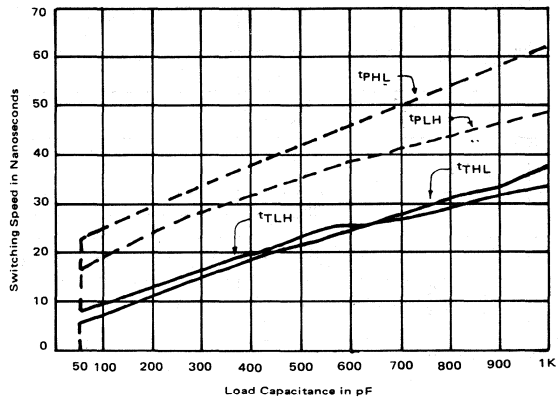
	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	$V_{CC3} = V_{CC2} + 3V$,	$V_{IH} = 2.0V$, $I_{OH} = -100\mu A$	$V_{CC2}-0.3$	$V_{CC2}-0.15$		V
		$V_{CC3} = V_{CC2} + 3V$,	$V_{IH} = 2.0V$, $I_{OH} = -10mA$	$V_{CC2}-1.2$	$V_{CC2}-1.0$		
		$V_{CC3} = V_{CC2}$,	$V_{IH} = 2.0V$, $I_{OH} = -50\mu A$	$V_{CC2}-1.0$	$V_{CC2}-0.7$		
V_{OL}	Low-level output voltage	$V_{CC3} = V_{CC2} = 10.8V$,	$V_{IN} = 0.8V$, $I_{OL} = 10mA$		0.3	0.5	V
I_I	Input current at maximum input voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-level input current	$V_I = 2.4V$	A inputs			40	μA
			E inputs			80	
I_{IL}	Low-level input current	$V_I = 0.4V$	A inputs		−1	−1.6	mA
			E inputs		−2	−3.2	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	$V_{CC1} = 5.25V$, $V_{CC2} = V_{CC3} = 12V$	$V_I = 0V$, No Load		7.5	11.0	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low	$V_{CC1} = 5.0V$, $V_{CC2} = 15V$	$V_I = 0V$		.85	1.2	
$I_{CC3(L)}$	Supply current from V_{CC3}, all outputs low	$V_{CC3} = 18V$	No Load		6.0	9.0	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	$V_{CC1} = 5.25V$, $V_{CC2} = V_{CC3} = 12V$	$V_I = 5.0V$, No Load		17.7	25.0	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high	$V_{CC1} = 5.0V$, $V_{CC2} = 15V$	$V_I = 5.0V$		−.86	−1.2	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high	$V_{CC3} = 18V$	No Load		.86	1.2	

All typical values are at $V_{CC1} = 5V$, $V_{CC2} = 12V$, $V_{CC3} = 15V$ and $T_A = 25°C$ unless otherwise noted.

TOTAL DISSIPATION (BOTH DRIVERS) vs FREQUENCY



TYPICAL SWITCHING SPEEDS vs LOAD CAPACITANCE

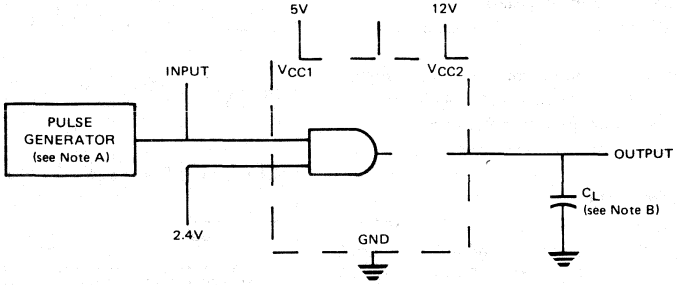


NOTE: Package power dissipation may be exceeded with some combinations of large C_L and high frequency operation.

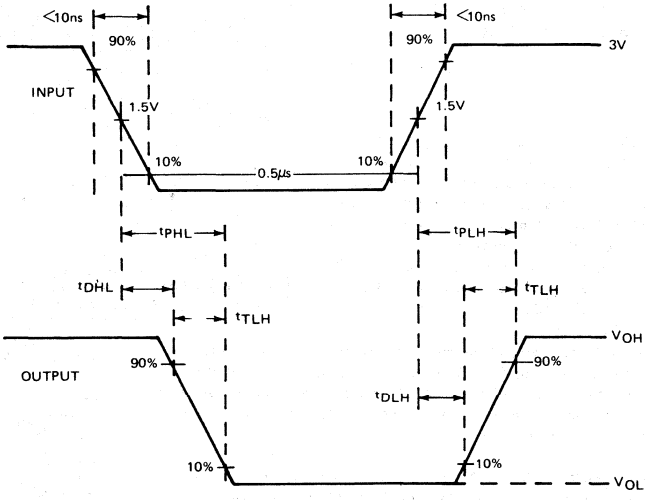
switching characteristics, V_{CC1} = 5V, V_{CC2} = 12V, V_{CC3} = 15V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 300pF See Figure 1	7	12	17	ns
t_{DHL}	Delay time, high-to-low-level output		10	17	24	ns
t_{TLH}	Transition time, low-to-high-level output		10	16	22	ns
t_{THL}	Transition time, high-to-low-level output		10	16	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output		17	29	41	ns
t_{PHL}	Propagation delay time, high-to-low-level output		20	33	46	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING TIMES, EACH DRIVER

NOTES: A. The pulse generator has the following characteristics: PRR = 1MHz, $Z_{out} = 50\Omega$
B. C_L includes probe and jig capacitance

TYPES SN54S240, SN54S241, SN74S240, SN74S241
OCTAL BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

OCTOBER 1975

features:

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading on Data Lines
- Hysteresis at Inputs Improve Noise Margins
- 'S241 Can Be Interconnected With No External Components to Perform as Bi-directional Bus Transceiver

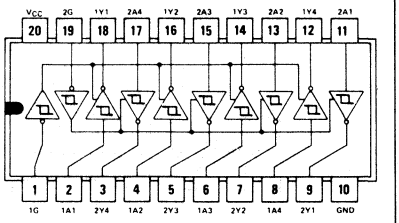
typical characteristics:

- Fan-Out:

	SN74S'	SN54S'
I_{OL} (Sink Current)	64 mA	48 mA
I_{OH} (Source Current)	−15 mA	−12 mA

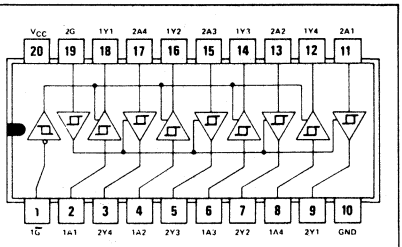
- Typical Propagation Delay Times:
  Data-to-Output:
  'S240 (Inverting) . . . 4.5 ns
  'S241 (Noninverting) . . . 6 ns
- Enable-to-Output . . . 9 ns

SN54S240 . . . J PACKAGE
SN74S240 . . . J OR N PACKAGE
(TOP VIEW)



logic: 1Y = 1$\overline{A}$ when 1$\overline{G}$ is low
2Y = 2$\overline{A}$ when 2$\overline{G}$ is low
When 1$\overline{G}$ is high 1Y outputs are at a high impedance
When 2$\overline{G}$ is high 2Y outputs are at a high impedance

SN54S241 . . . J PACKAGE
SN74S241 . . . J OR N PACKAGE
(TOP VIEW)



logic: 1Y = 1A when 1$\overline{G}$ is low
2Y = 2A when 2G is high
When 1$\overline{G}$ is high 1Y outputs are at a high impedance
When 2G is low 2Y outputs are at a high impedance

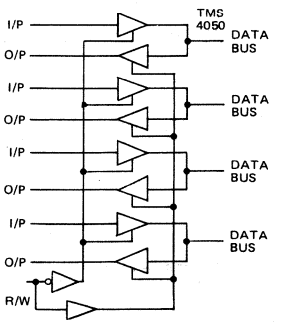
description

These buffers/line drivers are designed specifically to improve both the performance and p-c board density of 3-state buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 millivolts of hysteresis at each low-current p-n-p data-line input, they provide improved noise rejection and high-fan-out outputs to restore Schottky TTL levels completely, or the SN74S' versions can be used to drive terminated lines down to 133 Ω.

Typically, the 'S240 can replace the equivalent of six SN54S04, SN74S04 inverters or four SN54S130, SN74S140 line drivers at their rated drive capabilities with the added benefits of input hysteresis and 3-state outputs. The 'S241 offers the same complexity and drive capability but is designed for use in non-inverting applications.

In bus-organized systems, the 'S241 can be connected with no external components to perform as a non-inverting input/output bus transceiver. With complementing enable inputs, the control function can be connected directly to both enable inputs while the two 4-line data paths can be connected (at adjacent pins) input-to-output on both sides to form the asynchronous transceiver/buffer.

'S241
TMS4050 BUS TRANSCEIVER



TENTATIVE DATA SHEET

TEXAS INSTRUMENTS

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

recommended operating conditions

PARAMETER	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			48			64	mA
Operating free-air temperature, T_A (see Note 2)	−55		125	0		70	°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

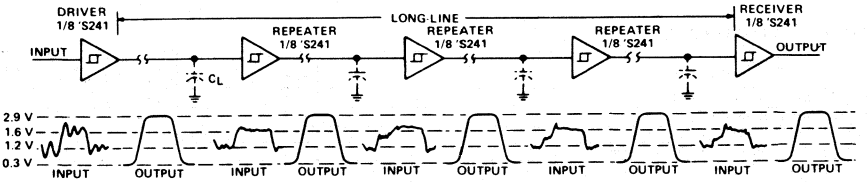
PARAMETER			TEST CONDITIONS†		'S240			'S241			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −3 mA	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
			V_{CC} = MIN, I_{OH} = MAX	V_{IL} = 0.5 V,	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN,	I_{OL} = MAX			0.55			0.55	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.5 V			−50			−50	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current, any input		V_{CC} = MAX,	V_{IH} = 2.7 V			50			50	μA
I_{IL}	Low-level input current	Any A	V_{CC} = MAX,	V_{IL} = 0.5 V			−400			−400	μA
		Any G					−2			−2	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply current	Total, outputs high	V_{CC} = MAX, Outputs open	SN54S'		80	123		95	147	mA
				SN74S'		80	135		95	160	
		Total, outputs low		SN54S'		100	145		120	170	
				SN74S'		100	150		120	180	
		Outputs at Hi-Z		SN54S'		100	145		120	170	
				SN74S'		100	150		120	180	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

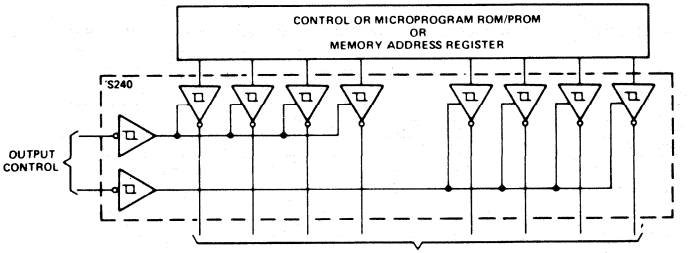
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'S240			'S241			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Note 3	R_L = 90 Ω,		4.5	7		6	9	ns
t_{PHL}	Propagation delay time, high-to-low-level output				4.5	7		6	9	ns
t_{ZL}	Output enable time to low level				10	15		10	15	ns
t_{ZH}	Output enable time to high level				6.5	10		8	12	ns
t_{LZ}	Output disable time from low level	C_L = 5 pF, See Note 3	R_L = 90 Ω,		10	15		10	15	ns
t_{HZ}	Output disable time from high level				6	9		6	9	ns

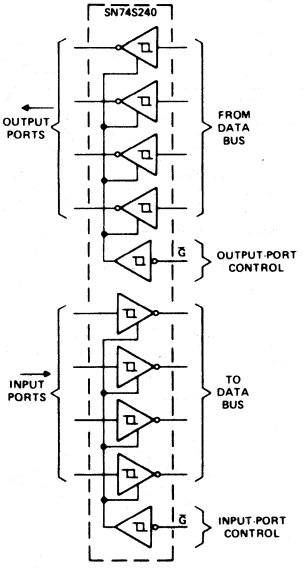
NOTE 3: Load circuit and waveforms are shown on page 148 of *The TTL Data Book for Design Engineers.*



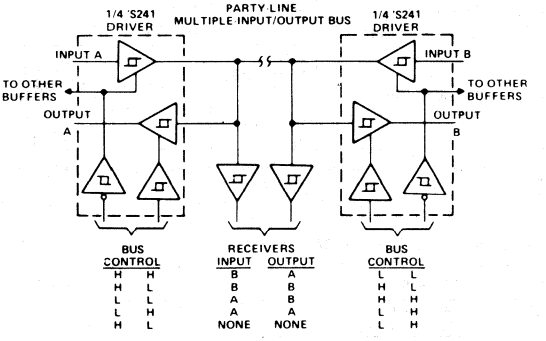
'S241's USED AS REPEATER/LEVEL RESTORER



'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS
IN A SINGLE PACKAGE



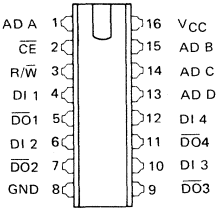
PARTY-LINE BUS SYSTEM
WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

TTL Memories

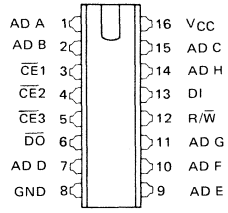
SERIES 54S/74S
RANDOM-ACCESS READ/WRITE MEMORIES

BULLETIN NO. DL-S 7512257, MAY 1975

64 BITS (16 WORDS BY 4 BITS)
'S189, 'S289



256 BITS (256 WORDS BY 1 BIT)
'S201, 'S301



Pin assignments for all of these memories are the same for all packages.

- Schottky-Clamped for High Performance
- Full On-Chip Decoding and Fast Chip-Enable Simplify System Decoding
- P-N-P Inputs Reduce Loading on System Buffers/Drivers
- Choice of 3-State or Open-Collector Outputs

TYPE NUMBER (PACKAGES)		TYPE OF	BIT SIZE	TYPICAL ACCESS TIMES		WRITE CYCLE TIME	
−55°C to 125°C	0°C to 70°C	OUTPUT(S)	(ORGANIZATIONS)	CHIP-SELECT	ADDRESS	SN54S'	SN74S'
SN54S189(J, W)	SN74S189(J, N)	3-State	64 Bits (16 W x 4 B)	12 ns	25 ns	25 ns	25 ns
SN54S289(J, W)	SN74S289(J, N)	Open-Collector					
SN54S201(J, W)	SN74S201(J, N)	3-State	256 Bits (256 W x 1 B)	13 ns	42 ns	100 ns	65 ns
SN54S301(J, W)	SN74S301(J, N)	Open-Collector					

description

These monolithic TTL memories feature Schottky clamping for high performance, a fast chip-select access time to enhance decoding at the system level, and the 'S201 and 'S209 RAMs utilize inverted-cell memory elements to achieve high densities. The memories feature p-n-p input transistors that reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a Series 54S/74S standard load factor.

A three-state-output version and an open-collector-output version are offered for each of the three organizations. A three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristic of the TTL totem-pole output. An open-collector output offers the capability of direct interface with a data line having a passive pull-up.

write cycle

Information to be stored in the memory is written into the selected address (AD) location when the chip-enable ($\overline{CE}$) and the read/write (R/$\overline{W}$) inputs are low. While the read/write input is low, the memory output(s) is(are) off (three-state = Hi-Z, open-collector = high). When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

read cycle

Information stored in the memory (see function table for input/output phase relationship) is available at the output(s) when the read/write input is high and the chip-enable input(s) is(are) low. When one(or more) chip-enable input is(are) high, the output(s) will be off.

FUNCTION TABLE

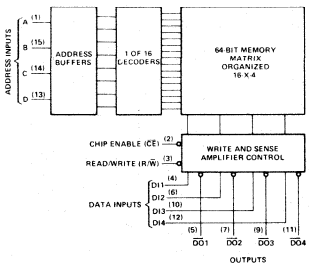
FUNCTION	†INPUTS		OUTPUTS	
	CHIP ENABLE†	READ/ WRITE	'S189 'S201	'S289 'S301
Write	L	L	High Impedance	H
Read	L	H	Complement of Data Entered	Complement of Data Entered
Inhibit	H	X	High Impedance	H

H = high level, L = low level, X = irrelevant

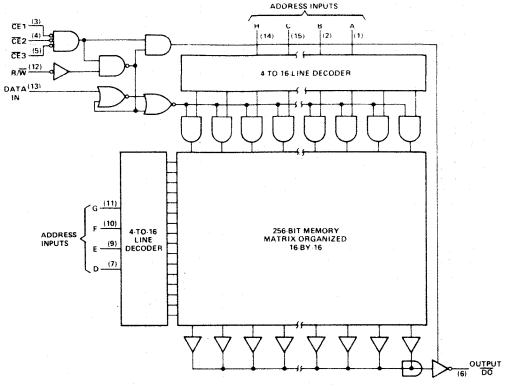
† For chip-enable of 'S201 and 'S301: L = all $\overline{CE}$ inputs low, H = one or more $\overline{CE}$ inputs high.

functional block diagrams

'S189, 'S289

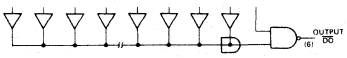


'S201



'S301

Same as 'S201 except output is as shown below.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' Circuits . . . . . −55°C to 125°C
SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S189			SN74S189			SN54S201			SN74S201			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−2			−6.5			−2			−10.3	mA
Low-level output current, I_{OL}				16			16			16			16	mA
Width of write pulse, $t_{w(wr)}$ (see Figure 1)		25			25			100			65			ns
Setup time (see Figure 1)	Address before write pulse, $t_{su(ad)}$	0↓			0↓			0↓			0↓			ns
	Chip enable before write pulse, $t_{su(\overline{CE})}$	0↓			0↓			0↓			0↓			
	Data before end of write pulse, $t_{su(da)}$	25↑			25↑			100↑			65↑			
Hold time (see Figure 1)	Address after write pulse, $t_{h(ad)}$	0↑			0↑			0↑			0↑			ns
	Chip enable after write pulse, $t_{h(\overline{CE})}$	0↑			0↑			0↑			0↑			
	Data after write pulse, $t_{h(da)}$	0↑			0↑			0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	−55		125	0		70	°C

↑↓The arrow indicates the transition of the read/write input used for reference: ↑for the low-to-high-transition, ↓for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			'S189			'S201			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = ♦					−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	Series 54S'		2.4	3.4		2.4	3.3		V
			Series 74S'		2.4	3.2		2.4	2.9		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA	Series 54S'			0.35	0.5		0.38	0.5	V
			Series 74S'			0.35	0.45		0.38	0.45	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 2.4 V					50			40	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 0.4 V					−50			−40	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	Series 54S'	T_A = MAX			110			115	mA
				T_A = 25°C		75	110		100	140	
				T_A = MIN			110			155	
			Series 74S'	Full range		75	110		100	140	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.
♦I_I = −18 mA for 'S189 and 'S201, −12 mA for 'S209.
NOTE 2: For the 'S189 I_{CC} is measured with the read/write and chip-enable inputs grounded, all other inputs at 4.5 V, and the outputs open.
For the 'S201 and SN74S209 I_{CC} is measured with all chip-enable inputs grounded, all other inputs at 4.5 V, and the output open.

recommended operating conditions

		SN54S289			SN74S289			SN54S301			SN74S301			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}				16			16			16			16	mA
Width of write pulse, $t_{w(wr)}$ (see Figure 1)		25			25			100			65			ns
Setup time (see Figure 2)	Address before write pulse, $t_{su(ad)}$	0↓			0↓			0↓			0↓			ns
	Chip enable before write pulse, $t_{su(\overline{CE})}$	0↓			0↓			0↓			0↓			
	Data before end of write pulse, $t_{su(da)}$	25↑			25↑			100↑			65↑			
Hold time (see Figure 2)	Address after write pulse, $t_{h(ad)}$	0↑			0↑			0↑			0↑			ns
	Chip enable after write pulse, $t_{h(\overline{CE})}$	0↑			0↑			0↑			0↑			
	Data after write pulse, $t_{h(da)}$	0↑			0↑			0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	−55		125	0		70	°C

↑↓The arrow indicates the transition of the read/write input used for reference: ↑for the low-to-high-transition, ↓for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			'S289			'S301			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = ♦					−1.2			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V		V_O = 2.4 V			40			40	μA
				V_O = 5.5 V			100			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		Series 54S'			0.5		0.38	0.5	V
				Series 74S'			0.45		0.38	0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−250			−250	μA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3	Series 54S'	T_A = MAX			105			110	mA
				T_A = 25°C		75	105		100	140	
				T_A = MIN			105			155	
			Series 74S'	Full range		75	105		100	140	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦I_I = −18 mA for 'S289 and 'S301, −12 mA for 'S309.
NOTE 3: For the 'S289 I_{CC} is measured with the read/write and chip-enable inputs grounded, all other inputs at 4.5 V, and the outputs open.
For the 'S301 and SN74S309 I_{CC} is measured with all chip-enable inputs grounded, all other inputs at 4.5 V, and the output open.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

random-access memories with three-state outputs

PARAMETER			TEST CONDITIONS	SN54S189		SN74S189		SN54S201		SN74S201		UNIT
				TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{w(wr,min)}$	Minimum width of write pulse		C_L = 30 pF, R_L = 300 Ω, See Figure 1	15	25	15	25	40	100	40	65	ns
$t_{a(ad)}$	Access time from address			25	50	25	35	42	85	42	65	ns
$t_{a(\overline{CE})}$	Access time from chip enable (enable time)			12	25	12	17	13	40	13	30	ns
t_{SR}	Sense recovery time			22	40	22	35	20	50	20	40	ns
t_{PXZ}	Disable time from high or low level	from $\overline{CE}$	C_L = 5 pF, R_{L1} = 300 Ω, See Figure 1	12	25	12	17	9	30	9	20	ns
		from R/$\overline{W}$		12		12		13	45	13	35	

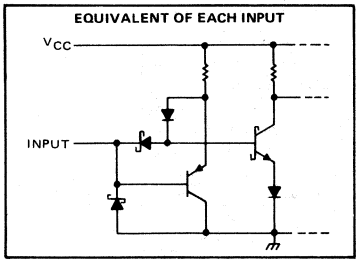
random-access memories with open-collector outputs

PARAMETER			TEST CONDITIONS	SN54S289		SN74S289		SN54S301		SN74S301		UNIT
				TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{w(wr,min)}$	Minimum width of write pulse		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 2	15	25	15	25	40	100	40	65	ns
$t_{a(ad)}$	Access time from address			25	50	25	35	42	85	42	65	ns
$t_{a(\overline{CE})}$	Access time from chip enable (enable time)			12	25	12	17	13	40	13	30	ns
t_{SR}	Sense recovery time			22	40	22	35	20	50	20	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	from $\overline{CE}$		12	25	12	17	8	30	8	20	ns
		from R/$\overline{W}$		12		12		15	45	15	35	

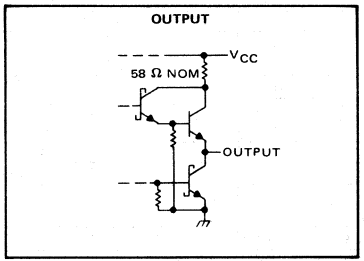
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics of inputs and outputs

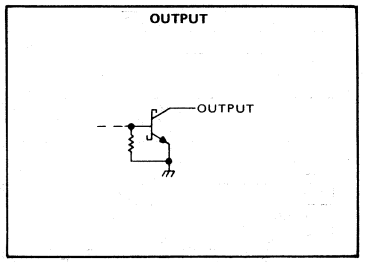
'S189, 'S201
'S289, 'S301



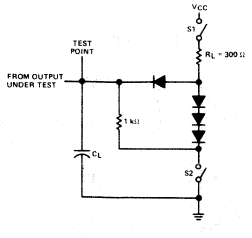
'S189, 'S201



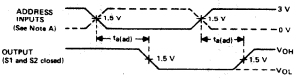
289, 'S301



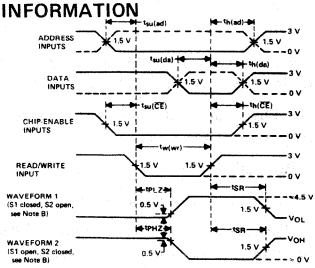
PARAMETER MEASUREMENT INFORMATION



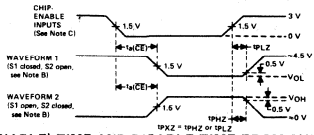
LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



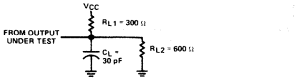
WRITE CYCLE VOLTAGE WAVEFORMS



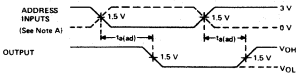
ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP ENABLE VOLTAGE WAVEFORMS

NOTES:
A. When measuring access times from address inputs, the chip enable input(s) is(are) low and the read/write is high.
B. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
C. When measuring access and disable times from chip enable input(s), the address inputs are steady-state and the read/write input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

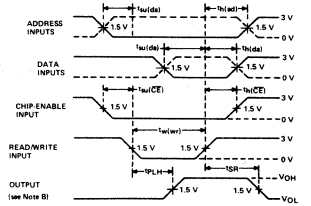
FIGURE 1—TESTING RAM's WITH 3-STATE OUTPUTS



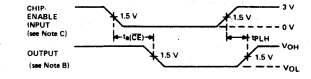
LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



WRITE CYCLE VOLTAGE WAVEFORMS



ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP ENABLE VOLTAGE WAVEFORMS

NOTES:
A. When measuring access times from address inputs, the chip-enable input(s) is(are) low and the read/write input is high.
B. Waveform shown is for the output with internal conditions such that the output is low except when disabled.
C. When measuring access and disable times from chip-enable input(s), the address inputs are steady-state and the read/write input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

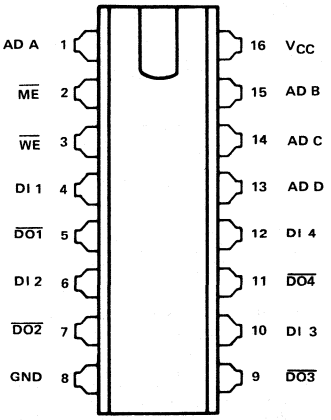
FIGURE 2—TESTING RAM's WITH OPEN-COLLECTOR OUTPUTS

TYPE SN7489
64-BIT RANDOM-ACCESS READ/WRITE MEMORY

BULLETIN NO. DL-S 7511386, DECEMBER 1972—REVISED MAY 1975

- For Application as a "Scratch Pad" Memory with Nondestructive Read-Out
- Fully Decoded Memory Organized as 16 Words of Four Bits Each
- Fast Access Time . . . 33 ns Typical
- Diode-Clamped, Buffered Inputs
- Open-Collector Outputs Provide Wire-AND Capability
- Typical Power Dissipation . . . 375 mW
- Compatible with Most TTL and DTL Circuits

J OR N PACKAGE



description

This 64-bit active-element memory is a monolithic, high-speed, transistor-transistor logic (TTL) array of 64 flip-flop memory cells organized in a matrix to provide 16 words of four bits each. Each of the 16 words is addressed in straight binary with full on-chip decoding.

The buffered memory inputs consist of four address lines, four data inputs, a write enable, and a memory enable for controlling the entry and access of data. The memory has open-collector outputs which may be wire-AND connected to permit expansion up to 4704 words of N-bit length without additional output buffering. Access time is typically 33 nanoseconds; power dissipation is typically 375 milliwatts.

$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

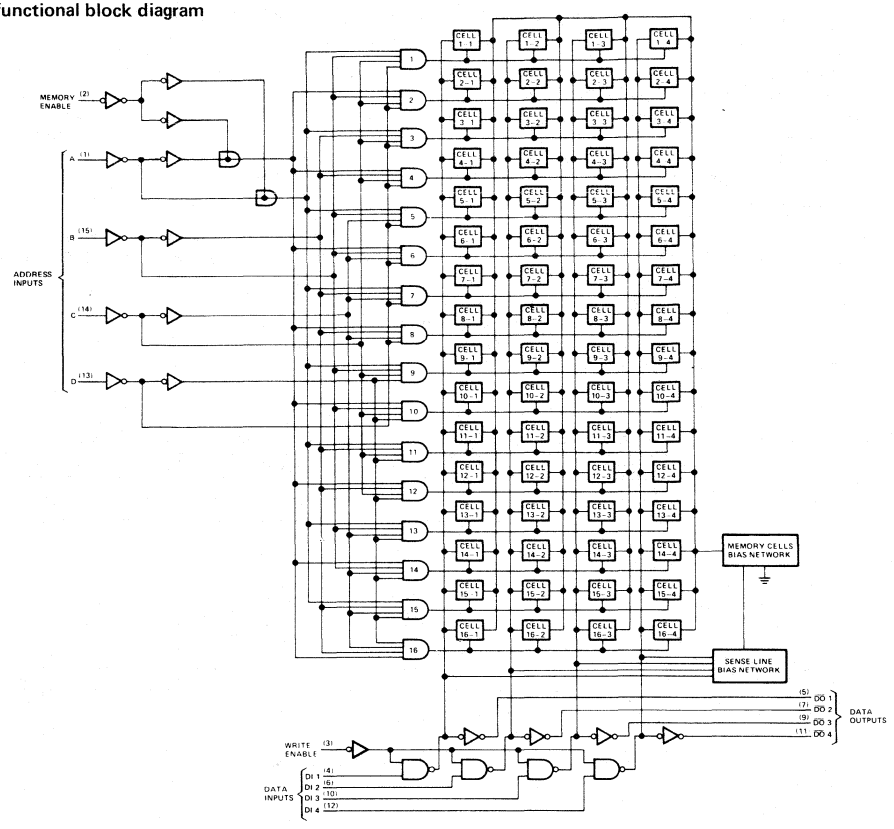
write operation

Information present at the data inputs is written into the memory by addressing the desired word and holding both the memory enable and write enable low. Since the internal output of the data input gate is common to the input of the sense amplifier, the sense output will assume the opposite state of the information at the data inputs when the write enable is low.

read operation

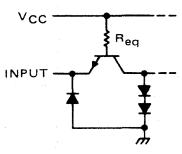
The complement of the information which has been written into the memory is nondestructively read out at the four sense outputs. This is accomplished by holding the memory enable low, the write enable high, and selecting the desired address.

functional block diagram



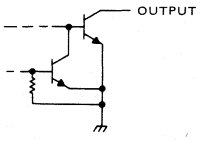
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Data Inputs: R_{eq} = 6 kΩ NOM
All others: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
High-level output voltage, V_{OH} (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage that should be applied to any output when it is in the off state.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Width of write-enable pulse, t_w	40			ns
Setup time, data input with respect to write enable, t_{su} (see Figure 1)	40			ns
Hold time, data input with respect to write enable, t_h (see Figure 1)	5			ns
Select input setup time with respect to write enable, t_{su}	0			ns
Select input hold time after writing, t_h (see Figure 1)	5			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			20	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = 12 mA			0.4	V
			I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		75	105	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 2.4 V,		6.5		pF

NOTE 3: I_{CC} is measured with the memory enable grounded, all other inputs at 4.5 V, and all outputs open.

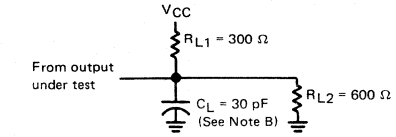
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

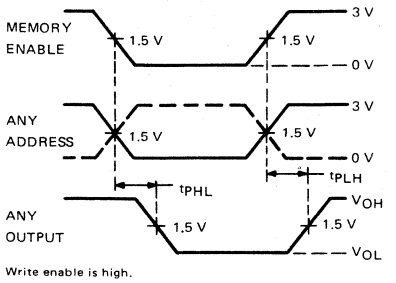
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from memory enable		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1		26	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output from memory enable				33	50	
t_{PLH}	Propagation delay time, low-to-high-level output from any address input				30	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from any address input				35	60	
t_{SR}	Sense recovery time after writing	output initially high			39	70	ns
		output initially low			48	70	

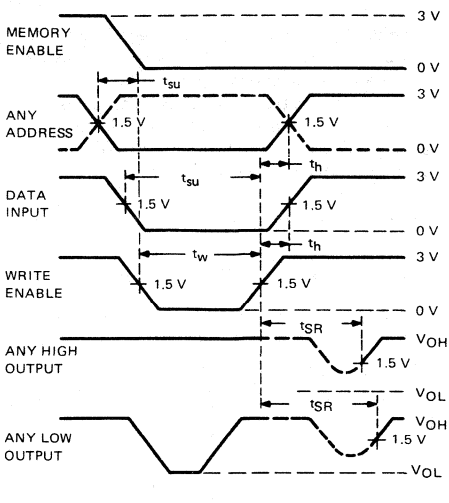
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



READ CYCLE



WRITE CYCLE FROM WRITE ENABLE

NOTES: A. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

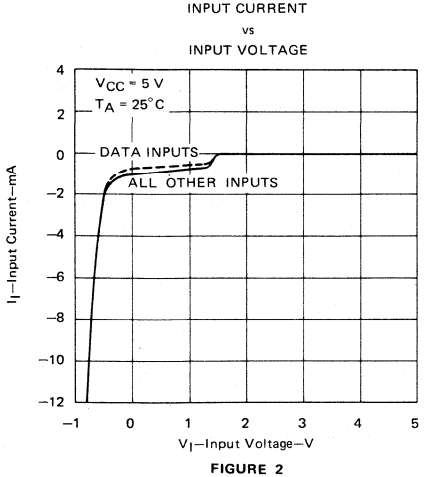


FIGURE 2

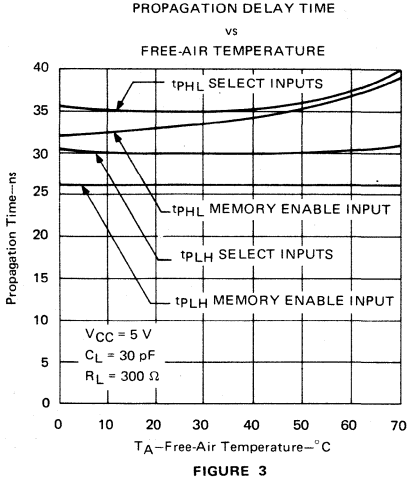
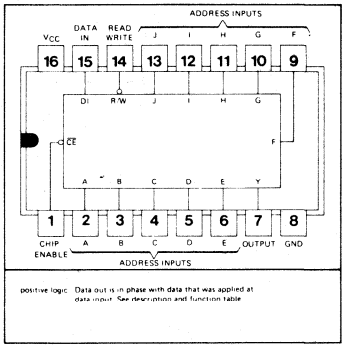


FIGURE 3

SN54S214,SN54S314,SN74S214,SN74S314 1024-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

- Fully Decoded, Organized as 1024 Words of One Bit Each
- Schottky-Clamped for High-Speed Memory Systems:
  Access from Chip-Enable Inputs . . . 15 ns Typical
  Access from Address Inputs . . . 30 ns Typical
  Power Dissipation . . . 0.5 mW/Bit Typical
- Choice of Three-State or Open-Collector Outputs
- Compatible with TTL and I^2L SBP0400
- Chip-Enable Input Simplifies External Decoding

DIP PACKAGE (TOP VIEW)

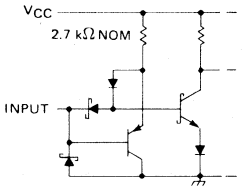


description

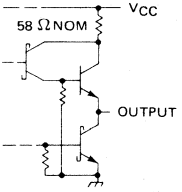
This 1024-bit active-element memory is a monolithic transistor-transistor logic (TTL) array organized as 1024 words of one bit each. It is fully decoded and has a chip-enable input to simplify decoding required to achieve the desired system organization.

schematics of inputs and outputs

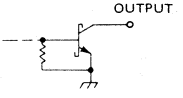
EQUIVALENT OF EACH INPUT



SN54S/74S214 OUTPUT



SN54S/74S314 OUTPUT



write cycle

The information applied at the data input is written into the selected location when the chip-enable input and the read/write input are low. While the read/write input is low, the 'S214 output is in the high-impedance state and the 'S314 output is off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

The stored information (in-phase with that which was applied at the data input during the write cycle) is available at the output when the read/write input is high and the chip-enable input is low. When the chip-enable is high, the 'S214 output will be in the high-impedance state and the 'S314 output will be off.

FUNCTION TABLE

FUNCTION	INPUTS		'LS214 OUTPUT	'LS314 OUTPUT
	CHIP ENABLE	READ/ WRITE		
Write (Store Applied Data)	L	L	High Impedance	Off
Read	L	H	Stored Data	Stored Data
Inhibit	H	X	High Impedance	Off

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Operating free-air temperature range: SN54S' Circuits . . . . . −55°C to 125°C
SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−2			−10.3	mA
Low-level output current, I_{OL}				16			16	mA
Width of write-enable pulse (read/write low), t_w		50			35			ns
Setup time, t_{setup}	Address to read/write	15↓			5↓			ns
	Data to read/write	5↓			5↓			
	Chip-enable to read/write	5↓			5↓			
Hold time, t_{hold}	Address from read/write	5↑			5↑			ns
	Data from read/write	5↑			5↑			
	Chip-enable from read/write	5↑			5↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓ The arrow indicates the transition from the read/write input for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA				−1.2	V
V_{OH}	High-level output voltage SN54S/74S214	V_{CC} =MAX, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = MAX	Series 54S Series 74S	2.4 2.4	3.2 2.9		V
V_{OL}	Low level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} =2V, I_{OL} = 16mA			0.35	0.45	V
I_{OH}	High-level output current SN54S/74S314	V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} =2V	V_O = 2.4V V_O = 5.5V			50 100	μA
I_{OZH}	Off-state output current, high-level voltage applied SN54S/74S214	V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_O = 2.4V				50	μA
I_{OZL}	Off-state output current, low-level voltage applied SN54S/74S214	V_{CC} = MAX, V_{IL} = 0.8V,	V_{IH} = 2V, V_O = 0.4 V				−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−250	μA
I_{OS}	Short-circuit output current* SN54S/74S214	V_{CC} = MAX			−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			95	130	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
*Duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all inputs grounded and the output open.

SN54S/74S214 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

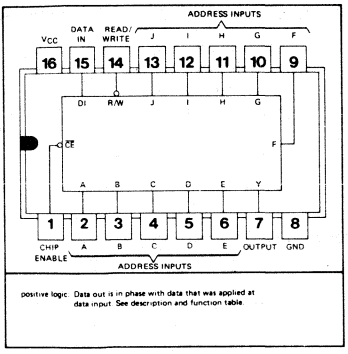
PARAMETER			TEST CONDITIONS	SN54S214			SN74S214			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
tpLH	Propagation delay time, low-to-high-level output	Access times from address	C_L = 30 pF, R_L = 400Ω, See Note 3		30	60		30	45	ns
tpHL	Propagation delay time, high-to-low-level output				30	60		30	45	
tZH	Output enable time to high level	Access times from chip enable			15	40		15	30	ns
tZL	Output enable time to low level				15	40		15	30	
tZH	Output enable time to high level	Sense recovery times from read/write			20	45		20	30	ns
tZL	Output enable time to low level				20	45		20	30	
tHZ	Output disable time from high level	Disable times from chip enable	C_L = 5 pF, R_L = 400Ω, See Note 3		10	30		10	20	ns
tLZ	Output disable time from low level				10	30		10	20	
tHZ	Output disable time from high level	Disable times from read/write			15	40		15	30	ns
tLZ	Output disable time from low level				15	40		15	30	

SN54S/74S314 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S314			SN74S314			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
tPLH	Propagation delay time, low-to-high-level output	Access times from address	C_L = 30 pF, R_{L1} = 300Ω, R_{L2} = 600 Ω, See Note 4		30	60		30	45	ns
tPHL	Propagation delay time, high-to-low-level				30	60		30	45	
tPLH	Propagation delay time, low-to-high-level output (disable time)	From chip enable			15	40		15	30	ns
		From read/write			20	45		20	30	
tPHL	Propagation delay time, high-to-low-level output	Output enable			15	40		15	30	ns
tSR	Sense recovery time	From read/write			20	45		20	30	ns

SN54LS214,SN54LS314,SN74LS214,SN74LS314 1024-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

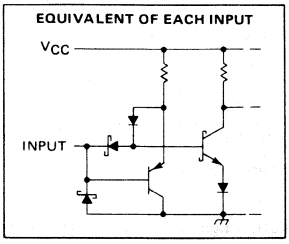
- Fully Decoded, Organized as 1024 Words of One Bit Each
- Schottky-Clamped for High-Speed Memory Systems: Access from Chip-Enable Inputs . . . 20 ns Typical Power Dissipation . . . 0.2 mW/Bit Typical
- Choice of Three-State or Open-Collector Outputs
- Compatible with TTL and I^2L SBP0400
- Chip-Enable input Simplifies External Decoding

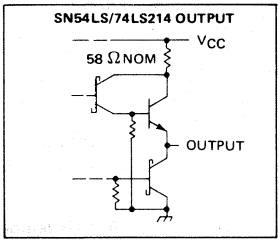


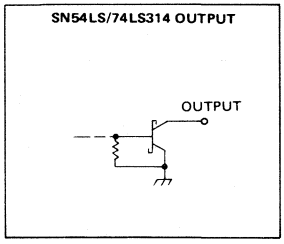
description

This 1024-bit active-element memory is a monolithic transistor-transistor logic (TTL) array organized as 1024 words of one bit each. It is fully decoded and has a chip-enable input to simplify decoding required to achieve the desired system organization.

schematics of inputs and outputs







write cycle

The information applied at the data input is written into the selected location when the chip-enable input and the read/write input are low. While the read/write input is low, the 'LS214 output is in the high-impedance state and the 'LS314 output is off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

The stored information (in-phase with that which was applied at the data input during the write cycle) is available at the output when the read/write input is high and the chip-enable input is low. When the chip-enable input is high, the 'LS214 output will be in the high-impedance state and the 'LS314 output will be off.

FUNCTION TABLE

FUNCTION	INPUTS		'LS214 OUTPUT	'LS314 OUTPUT
	CHIP ENABLE	READ/ WRITE		
Write (Store Applied Data)	L	L	High Impedance	Off
Read	L	H	Stored Data	Stored Data
Inhibit	H	X	High Impedance	Off

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' Circuits . . . . . −55°C to 125°C
SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−5	mA
Low-level output current, I_{OL}				4			8	mA
Width of write-enable pulse (read/write low), t_w		100			80			ns
Setup time, t_{setup}	Address to read/write	40↓			30↓			ns
	Data to read/write	10↓			10↓			
	Chip-enable to read/write	0↓			0↓			
Hold time, t_{hold}	Address from read/write	10↑			10↑			ns
	Data from read/write	10↑			10↑			
	Chip-enable from read/write	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓ The arrow indicates the transition from the read/write input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage, SN54LS/74LS214	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OH} = MAX	Series 54LS	2.4	3.2		V
				Series 74LS	2.4	2.9		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = MAX			0.4	0.5	V
I_{OH}	High-level output current SN54LS/74LS314	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V		V_O = 2.4 V			50	μA
				V_O = 5.5 V			100	
I_{OZH}	Off-state output current, high-level voltage applied SN54LS/74LS214	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V,	V_{OH} = 2.4 V				50	μA
I_{OZL}	Off-state output current, low-level voltage applied SN54LS/74LS214	V_{CC} = MAX V_{IH} = 2 V, V_{IL} = 0.8 V,	V_O = 0.4V				−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−250	μA
I_{OS}	Short-circuit output current* SN54LS/74LS214	V_{CC} = MAX			−15		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2				35	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
*Duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all inputs grounded and the output open.

SN54LS/74LS214 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54LS214			SN74LS214			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	Access times from address	C_L = 30 pF, R_L = 600 Ω, See Note 3			110			90	ns
t_{PLH}	Propagation delay time, high-to-low-level output					110			90	
t_{ZH}	Output enable time to high level	Access times from chip enable				75			60	ns
t_{ZL}	Output enable time to low level					75			60	
t_{ZH}	Output enable time to high level	Sense recovery times from read/write				75			60	ns
t_{ZL}	Output enable time to low level					75			60	
t_{HZ}	Output disable time from high level	Disable times from chip enable	C_L = 5 pF R_L = 600 Ω, See Note 3			65			50	ns
t_{LZ}	Output disable time from low level					65			50	
t_{HZ}	Output disable time from high level	Disable times from read/write				75			60	ns
t_{HZ}	Output disable time from low level					75			60	

SN54LS/74LS314 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54LS314			SN74LS314			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	Access times from address	C_L = 15 pF, R_{L1} = 600 Ω, R_{L2} = 1.2 kΩ, See Note 4			110			90	ns
t_{PHL}	Propagation delay time, high-to-low-level output					110			90	
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	From chip enable				75			60	ns
		From read/write				75			60	
t_{PHL}	Propagation delay time, high-to-low-level output	Output enable				75			60	ns
t_{SR}	Sense recovery time	From read/write				75			60	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

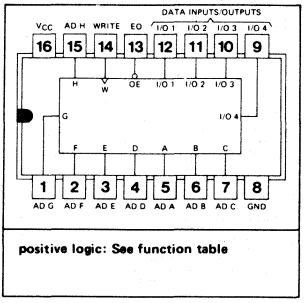
NOTES: 3. Load circuit and voltage waveforms are the same as those shown in Figure , page number of the *Semiconductor Memory Data Book*. The data out is in phase with data in.

4. Load circuit and voltage waveforms are the same as those shown in Figure , page number of the *Semiconductor Memory Data Book*. The data out is inphase with data in.

SN54S207,SN54S208,SN74S207,SN74S208 1024-BIT EDGE-TRIGGERED RANDOM-ACCESS MEMORIES WITH 3-STATE OUTPUTS

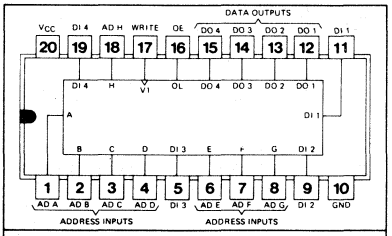
- Fully Decoded, Organized as 256 Words of Four Bits Each
- Schottky-Clamped for High-Speed Memory Systems:
  - Access from Chip-Enable Inputs ... 15 ns Typical
  - Access from Address Inputs ... 35 ns Typical
- Edge-triggered Write Control
- 'S207 Data and Address are Same Pins as 1K ROM/PROM
- High-Density Packages have Pin-Row Spacing of 0.3-inch
- Three-State Output for Driving Bus-Organized Systems and/or Highly Capacitive Loads
- Compatible with Most TTL and I^2L Microprocessor Circuits

SN54S207, SN74S207
J, N, OR W PACKAGE (TOP VIEW)



positive logic: See function table

SN54S208, SN74S208
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

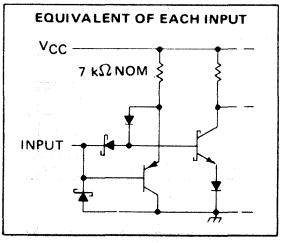


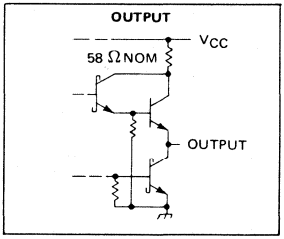
positive logic: See function table

description

These 1024-bit active-element memories are monolithic transistor-transistor logic (TTL) arrays organized as 256 words of four bits each. They are fully decoded with output enable inputs to simplify decoding required to achieve the desired system organization. Read and write times are virtually equal, which simplifies control implementation.

schematics of inputs and outputs





write cycle

While the output-enable input of the 'S207 is high, data applied to the input/output (I/O) is written into the selected location on a positive transition at the write input. Information at the data input of the 'S208 memory is written into the selected location on a positive transition at the write input regardless of the state of the output-enable input. While the output-enable input is high, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

read cycle

The stored information is available at the output when the output-enable input is low.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range, SN54S207, SN54S208 . . . . . −55°C to 125°C
SN74S207, SN74S208 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−.2			−6.5	mA
Low-level output current, I_{OL}				16			16	mA
Width of write-enable pulse (high), t_w		35			25			ns
Setup time, t_{setup} (see Figure 1)	Address to write	0↑			0↑			ns
	Data to write	0↑			0↑			
Hold time, t_{hold} (See Figure 1)	Address from write	70↑			50↑			ns
	Data from write	70↑			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑ ↓ The arrow indicates the transistion of the read/write input for reference: ↑for the low-to-high transition, ↓for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54S'			SN74S'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.2		2.4	2.9		V
V_{OL}	Low-level output voltages		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.5			0.45	V
I_{OZH}	Off-state output current, high-level voltage applied	SN54S/74S207	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 2.4 V			25			25	μA
		SN54S/74S208				50			50	
I_{OZL}	Off-state output current, low-level voltage applied	SN54S/74S207	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 0.5 V			−250			−250	μA
		SN54S/74S208				−50			−50	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4 V, See Note 2			25			25	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current*		V_{CC} = MAX,	−30		−100	−30		−100	mA
I_{CC}	Supply current	SN54S/74S207	V_{CC} = MAX, See Note 3		120	160		120	180	mA
		SN54S/74S208			120	160		120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
* Duration of the short-circuit should not exceed one second.
NOTES: 2. For the 'S207, I_{IL} is measured with the output enable at 4.5V.
3. I_{CC} is measured with the write high, output enable grounded, all other inputs at 4.5 V, and all outputs open.

PARAMETER MEASUREMENT INFORMATION

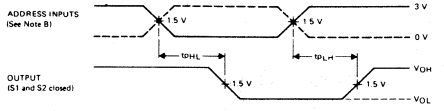


FIGURE 1 – ACCESS TIME FROM ADDRESS INPUTS
VOLTAGE WAVEFORMS

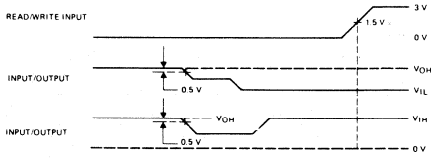


FIGURE 2 – SN54S/74S207 WRITE WHILE READ VOLTAGE WAVEFORMS

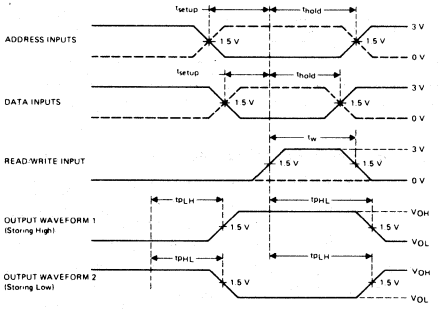


FIGURE 3 – SN54S/74S208 WRITE WHILE READ VOLTAGE WAVEFORMS
OUTPUT DISABLE/ENABLE IS LOW

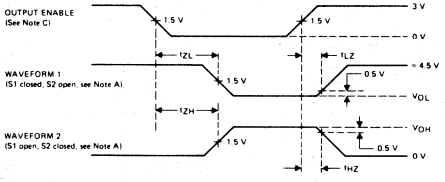
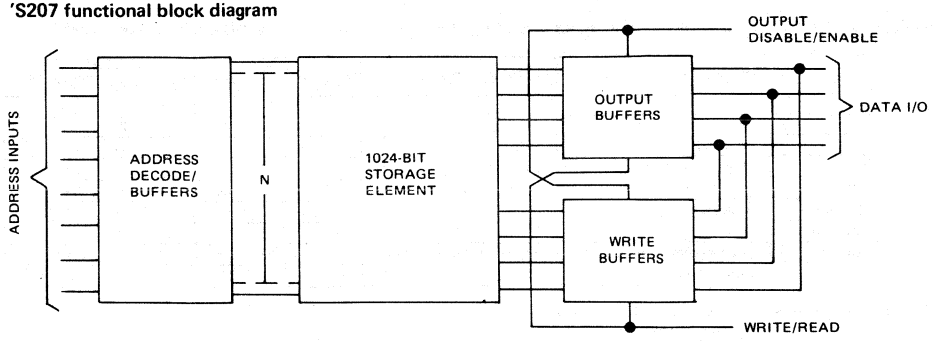


FIGURE 4 – ACCESS (ENABLE) TIME AND DISABLE TIME FROM OUTPUT ENABLE
VOLTAGE WAVEFORMS

NOTES: A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the output-enable and the write/read inputs are low.
C. When measuring delay times from the output-enable input, the address inputs are steady-state and the write/read input is low.
D. Input waveforms are supplied by the pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR $\leq$ 1 MHz, and $Z_{out} \approx 50\ \Omega$

'S207 functional block diagram

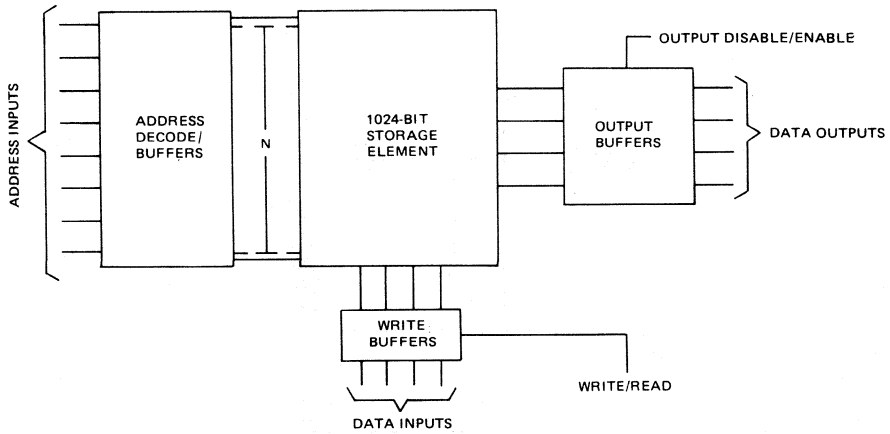


FUNCTION TABLE

FUNCTION	READ/WRITE	ENABLE	OUTPUTS
WRITE	↑	H	Hi-Z (USE AS DATA INPUTS)
READ	H or L	L	DATA ADDRESSED
DO NOTHING	H or L	H	Hi-Z

H = HIGH, L = LOW, ↑ = LOW-TO-HIGH TRANSITION

'S208 functional block diagram



FUNCTION TABLE

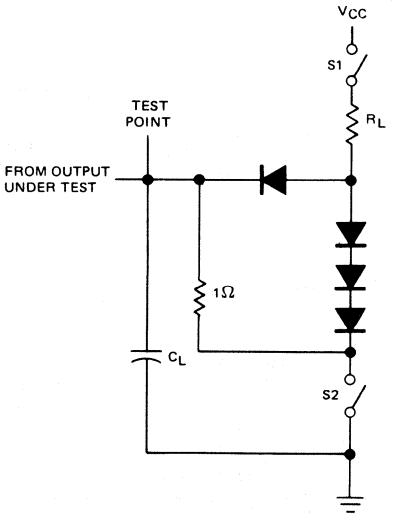
FUNCTION	READ/WRITE	ENABLE	OUTPUTS
WRITE AND READ	↑	L	DATA ADDRESSED
READ	H or L	L	DATA ADDRESSED
DO NOTHING	H or L	H	Hi-Z
WRITE ONLY	↑	H	Hi-Z

H = HIGH, L = LOW, ↑ = LOW-TO-HIGH TRANSITION

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER†		TEST CONDITIONS	SN54S'			SN74S'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{w(min)}$		C_L = 30 pF, R_L = 400 Ω, See Figure 1		10	35		10	25	ns
tpLH	Access times from address			35	70		35	50	ns
tpHL				35	70		35	50	
tZH	Access times from output enable			15	35		15	25	ns
tZL				15	35		15	25	
tZH or tpLH	Access times from write			25	60		25	45	ns
tZL or tpHL				25	60		25	45	
tHZ	Disable times from output enable	C_L = 5 pF, R_L = 400 Ω, See Figure 1		10	30		10	20	ns
tLZ				10	30		10	20	

†$t_{w(min)}$ = minimum write-enable pulse-width (read/write low)
t_{PLH} = propagation delay time, low-to high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{ZH} = output enable time to high level
t_{ZL} = output enable time to low level
t_{HZ} = output disable time from high level
t_{LZ} = output disable time from low level
‡All typical values are at V_{CC} = 5 V, T_A = 25°C



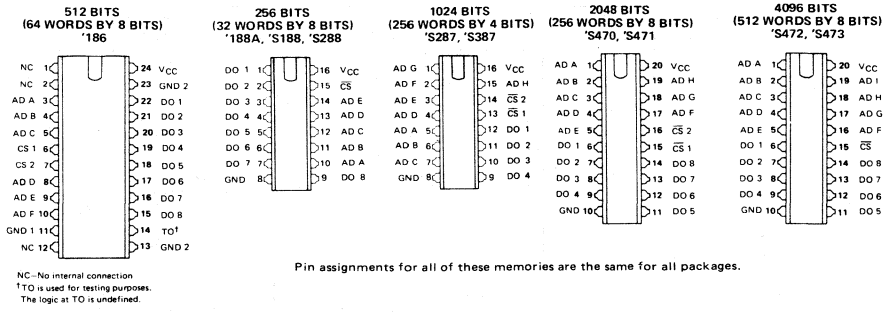
LOAD CIRCUIT

SERIES 54/74, 54S/74S
PROGRAMMABLE READ-ONLY MEMORIES

BULLETIN NO. DL-S 7512258, MAY 1975

- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  Fast Chip Select to Simplify System Decode
  Choice of Three-State or Open-Collector Outputs
  P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE	OUTPUT	TYPICAL ACCESS TIME (ns)	
−55°C to 125°C	0°C to 70°C	(ORGANIZATION)	CONFIGURATION	FROM ADDRESS	FROM CHIP SELECT
SN54186(J, W)	SN74186(J, N)	512 bits (64 W x 8 B)	open-collector	50	55
SN54188A(J, W)	SN74188A(J,N)	256 bits (32 W x 8 B)	open-collector	30	34
SN54S188(J, W)	SN74S188(J, N)		open-collector	25	12
SN54S288(J, W)	SN74S288(J, N)		three-state	25	12
SN54S287(J, W)	SN74S287(J, N)	1024 bits (256 W x 4 B)	three-state	42	15
SN54S387(J, W)	SN74S387(J, N)		open-collector	42	15
SN54S470(J)	SN74S470(J, N)	2048 bits (256 W x 8 B)	open-collector	50	20
SN54S471(J)	SN74S471(J, N)		three-state	50	20
SN54S472(J)*	SN74S472(J, N)	4096 bits (512 W x 8 B)	three-state	55	20
SN54S473(J)*	SN74S473(J, N)		open-collector	55	20



NC—No internal connection
†TO is used for testing purposes. The logic at TO is undefined.

Pin assignments for all of these memories are the same for all packages.

description

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in one millisecond or less. The Schottky-clamped versions of these PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit PROM's can be used to significantly improve system density for fixed memories as all are offered in the 20-pin dual-in-line package having pin-row spacings of 0.300 inch.

*24 Pin versions of this function will be available in July 1976

description (continued)

Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387, are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

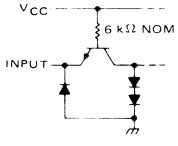
A low level at the chip-select input(s) enables each PROM except the '186, which is enabled by a high level at both chip-select inputs. The opposite level at any chip-select input causes the outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs

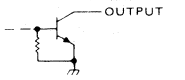
'186, '188A

EQUIVALENT OF EACH INPUT



'186, '188A

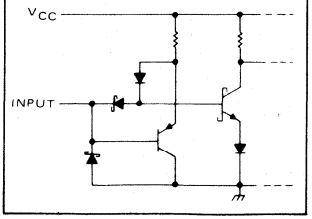
TYPICAL OF ALL OUTPUTS



Programming circuit not shown

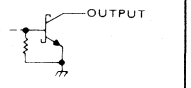
'S188, 'S287, 'S288, 'S387 'S470, 'S471, 'S472, 'S473

EQUIVALENT OF EACH INPUT



'S188, 'S387, 'S470, 'S473

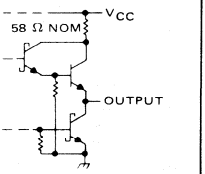
TYPICAL OF ALL OUTPUTS



Programming circuit not shown

'S287, 'S288 'S471, 'S472

TYPICAL OF ALL OUTPUTS



Programming circuit not shown

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54', SN54S' Circuits	−55°C to 125°C
SN74', SN74S' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal (GND 2 of '186),. For '186 GND 1 and both GND 2 terminals are all connected to system ground except during programming. The supply-voltage rating does not apply during programming of the '188, '188A, or the 54S/74S PROM's.

recommended conditions for programming

		MIN	NOM	MAX	UNIT
Supply voltages (see Note 2)	V_{CC}	4.75	5	5.25	V
	GND 1	−5		−6†	
Input conditions (see Note 3 and 4)	High level	Open circuit or equivalent			
	Low level	−5		−6†	V
Output voltage				−6.5†‡	V
Output current, output being programmed		−95	−120	−130	mA
Duration of programming pulse (see Note 5)		1			ms
Programming duty cycle			25	35	%
Free-air temperature		0		55	°C

†Absolute maximum ratings. ‡Clamp to ensure output does not exceed −0.5 V with respect to GND 1.

NOTES: 2. Voltage values are with respect to the GND 2 terminals.
3. The high-level (off) output of a Series 54/74 or 54S/74S open-collector gate with no pull-up resistor meets the requirements for a high-level input condition.
4. The low-level input voltage must be within ±0.5 volts of the applied voltage at GND 1.
5. Programming is guaranteed if the pulse is applied to the output for 10 ms. Typically, programming occurs in less than 1 ms.

step-by-step programming procedure

Programming the SN54186 or SN74186 is performed individually for each of the 512 bit locations and consists basically of applying a current pulse to each output terminal where a low logic level is to be changed to a high (off) level. The power supply and ground connections described below are designed to ensure that alteration of the memory content occurs during the programming procedure only.

1. Connect the memory as shown in Figure 1. To address a particular word in the memory, set the input switches to the binary equivalent of that word where a low logic level is as specified under "recommended conditions for programming" and a high logic level is either an open circuit or connection to an open-collector TTL gate with no pull-up resistor.
2. Apply a programming current pulse as specified to the pin associated with the first bit to be changed from a low-level to a high-level output.
3. Repeat Step 2 for each high-level output desired in the word addressed (program only one bit at a time). Any bit that is to remain at a low level should have its respective output open-circuited during the entire programming cycle for the addressed word.
4. Set the next input address and repeat steps 2 and 3 at a programming duty cycle of 35% maximum. This procedure is repeated for each input address for which a specific output word pattern is desired. A low logic level can always be changed to a high logic level simply by repeating Steps 1 and 2. Once programmed to provide a high logic level, the output cannot be changed to supply a low logic level.

NOTE: When verification indicates that a bit did not program the procedure should not be repeated.

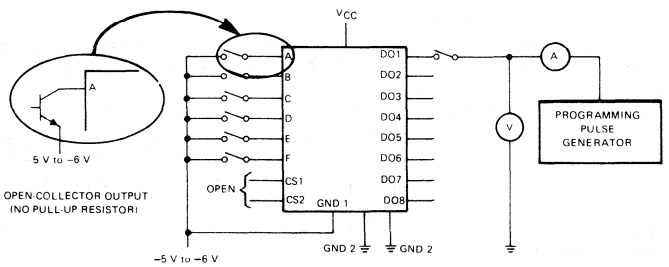


FIGURE 1—PROGRAMMING CONNECTIONS

recommended conditions for programming

		'188A			SN54S', SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 6)	Steady state	4.75	5	5.75	4.75	5	5.75	V
	Program pulse	10	10.5	11†	10	10.5	11†	
Input voltage	High level, V_{IH}	2.4		5	2.4		5	V
	Low level, V_{IL}	0		0.5	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 2)			See load circuit (Figure 2)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 7)			0.25	+0.3 −0.8	0	0.25	0.3	V
Duration of V_{CC} programming pulse Y (see Figure 3 and Note 8)		1			1			ms
Programming duty cycle			25	35		25	35	%
Free-air temperature		0		55	0		55	°C

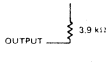
†Absolute maximum ratings.

NOTES: 6. Voltage values are with respect to the GND 2 terminals.
7. The '188A, 'S188, 'S288, 'S470, 'S471, 'S472, and 'S473 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
8. Programming is guaranteed if the pulse applied is 10 ms long. Typically, programming occurs in 1 ms.

step-by-step programming procedure

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9 kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current out of the programming output supply during programming is 150 mA.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 10 μs and 1 ms after V_{CC} has reached its 10.5-V level. See programming sequence of Figure 3.
7. After the X pulse time (1 ms) is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within 10 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.

NOTES: A) V_{CC} should be removed between program pulses to reduce dissipation and chip temperatures. See Figure 3.
B) When verification indicates that a bit did not program the procedure should not be repeated.



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION
FIGURE 2

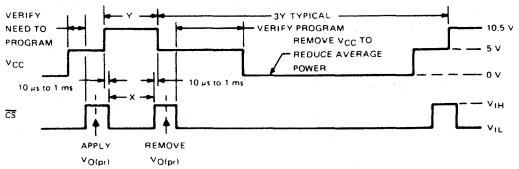


FIGURE 3–VOLTAGE WAVEFORMS FOR PROGRAMMING

recommended operating conditions

	SN54186 SN54188A			SN74186 SN74188A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'186			'188A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			100				µA
			V_{OH} = 5.5 V			200			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 12 mA				0.4			0.45	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40			40	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1			−1	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 9	Both CS at 0 V		47	95				mA
			Both CS at 4.5 V		80	120				
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX	See Note 10					50	80	mA
I_{CCL}	Supply current, all outputs low		See Note 11					82	110	
C_o	Off-state output capacitance	V_{CC} = 5 V, V_O = 2 V, f = 1 MHz			6.5			6.5		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 9. I_{CC} of '186 is measured with all outputs open and the address inputs at 4.5 V. Typical values are for 50% of the bits programmed.
10. I_{CCH} of '188A is measured with all inputs at 4.5 V, all outputs open.
11. I_{CCL} of '188A is measured with the chip-select input grounded, all other inputs at 4.5 V, and all outputs open. The typical value shown is for the worst-case condition of all eight outputs low at one time. This condition may not be possible after the device has been programmed.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(CS/\overline{CS})}$ (ns) Access time from chip select (enable time)		t_{PLH} (ns) Propagation delay time, low-to-high-level output from chip select (disable time)	
		TYP	MAX	TYP	MAX	TYP	MAX
'186	C_L = 30 pF, R_{L1} = 400 Ω,	50	75	55	75	40	75
'188A	R_{L2} = 600 Ω, See Figure 4	30	50	34	50	23	50

recommended operating conditions

		'S188			'S387, 'S470, 'S473			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				20			16	mA
Operating free-air temperature, T_A	Series 54S	−55		125	−55		125◆	°C
	Series 74S	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V				50	μA
			V_{OH} = 5.5 V				100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−250	μA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 12		'S188		80	110	mA
				'S387		100	135	
				'S470		110	155	
				'S473		120		

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{CS})}$ (ns) Access time from chip select (enable time)		t_{PLH} (ns) Propagation delay time, low-to-high-level output from chip select (disable time)	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MAX
SN54S188	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 4	25	50	12	30	12	30
SN74S188		25	40	12	25	12	25
SN54S387		42	75	15	40ǂ	15	40ǂ
SN74S387		42	65	15	35	15	35
SN54S470		50	80	20	40	15	35
SN74S470		50	70	20	35	15	30
SN54S473		55		20		15	
SN74S473		55		20		15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
◆An SN54S387 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 42 °C/W.
ǂTentative specifications.
NOTE 12: The typical values of I_{CC} shown are with all outputs low.

recommended operating conditions

		'287, 'S471, 'S472			'S288			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	Series 54S			−2			−2	mA
	Series 74S			−6.5			−6.5	
Low-level output current, I_{OL}				16			20	mA
Operating free-air temperature, T_A	Series 54S	−55		125	−55		125◆	°C
	Series 74S	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

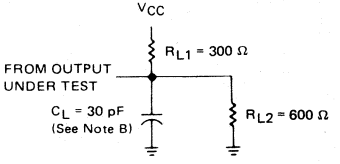
PARAMETER		TEST CONDITIONS†		SN54S'			SN74S'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 12	'S287		100	135		100	135	mA
			'S288		80	110		80	110	
			'S471		110	155		110	155	
			'S472		120			120		

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

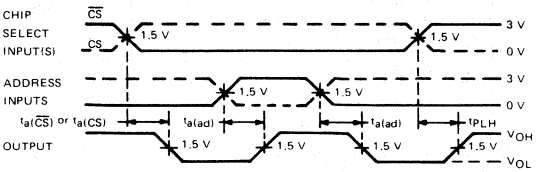
TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{CS})}$ (ns) Access time from chip select (enable time)		t_{PXZ} (ns) Disable time from high or low level	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MAX
SN54S287	C_L = 30 pF for $t_{a(ad)}$ and $t_{a(\overline{CS})}$, 5 pF for t_{PXZ}; R_L = 300 Ω; See Figure 5	42	75ʄ	15	40ʄ	12	
SN74S287		42	65	15	35	12	
SN54S288		25	50	12	30	8	30
SN74S288		25	40	12	25	8	20
SN54S471		50	80	20	40	15	35
SN74S471		50	70	20	35	15	30
SN54S472		55		20		15	
SN74S472		55		20		15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
◆An SN54S287 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 12: The typical values of I_{CC} shown are with all outputs low.
ʄTentative specifications

PARAMETER MEASUREMENT INFORMATION



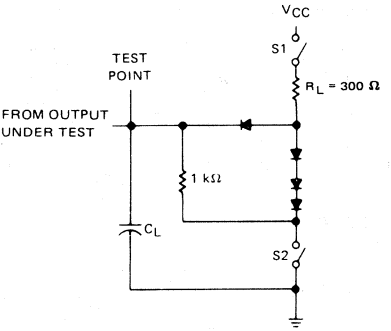
LOAD CIRCUIT



VOLTAGE WAVEFORMS

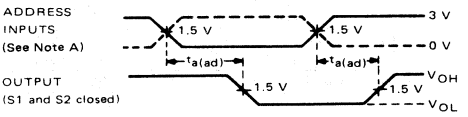
NOTES: A. The input pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR ⩽ 1 MHz. For Series 54/74, $t_r \leqslant 7$ ns, $t_f \leqslant 7$ ns. For Series 54S/74S, $t_r \leqslant 2.5$ ns, $t_f \leqslant 2.5$ ns.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 4–SWITCHING TIMES OF '186, '188A, 'S188, 'S470, 'S387, AND 'S473

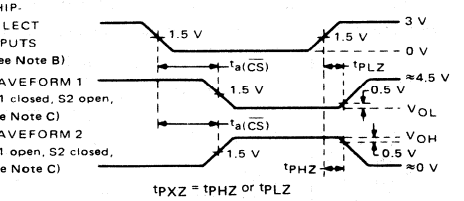


CL includes probe and jig capacitance.
All diodes are 1N3064.

LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



$t_{PXZ} = t_{PHZ}$ or t_{PLZ}

ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP SELECT VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the chip-select input(s) is(are) low.
B. When measuring access and disable times from chip-select input(s), the address inputs are steady-state.
C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leqslant 2.5$ ns, $t_f \leqslant 2.5$ ns, PRR ⩽ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

FIGURE 5–SWITCHING TIMES OF 'S287, 'S288, 'S471, AND 'S472

TEXAS INSTRUMENTS

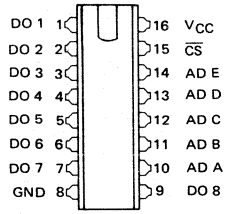
SERIES 54/74, 54S/74S
READ-ONLY MEMORIES

BULLETIN NO. DL-S 7512259, MAY 1975

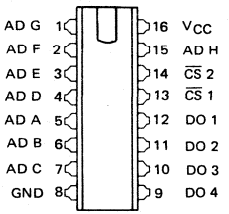
- Mask-Programmed Memories That Can Replace PROMs
- Full On-Chip Decoding and Fast Chip Select(s) Simplify System Decoding
- All Schottky-Clamped ROMs Offer
  - —Choice of 3-State or Open-Collector Outputs
  - —P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Applications Include:
  - —Microprogramming Firmware/Firmware Loaders
  - —Code Converters/Character Generators
  - —Translators/Emulators
  - —Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		TYPE OF	BIT SIZE	TYPICAL ACCESS TIMES	
−55°C to 125°C	0°C to 70°C	OUTPUT(S)	(ORGANIZATION)	CHIP-SELECT	ADDRESS
SN5488A(J, W)	SN7488A(J, N)	Open-Collector	256 Bits (32 W x 8 B)	22 ns	26 ns
SN54187(J, W)	SN74187(J, N)	Open-Collector	1024 Bits (256 W x 4 B)	20 ns	40 ns
SN54S270(J)	SN74S270(J, N)	Open-Collector	2048 Bits (512 W x 4 B)	15 ns	45 ns
SN54S370(J)	SN74S370(J, N)	3-State			
SN54S271(J)	SN74S271(J, N)	Open-Collector	2048 Bits (256 W x 8 B)	15 ns	45 ns
SN54S371(J)	SN74S371(J, N)	3-State			

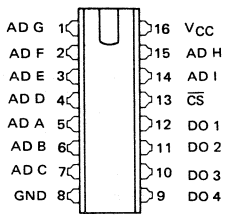
256 BITS (32 WORDS BY 8 BITS)
'88A



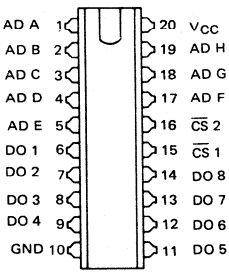
1024 BITS (256 WORDS BY 4 BITS)
'187



2048 BITS (512 WORDS BY 4 BITS)
'S270, 'S370



2048 BITS (256 WORDS BY 8 BITS)
'S271, 'S371



Pin assignments for all of these memories are the same for all packages.

description

These monolithic TTL custom-programmed read-only memories (ROMs) are particularly attractive for applications requiring medium to large quantities of the same bit pattern. Plug-in replacements can be obtained for most of the popular TTL PROMs.

The high-complexity 2048-bit ROMs can be used to significantly improve system bit density for fixed memory as all are offered in compact 16- or 20-pin dual-in-line packages having pin-row spacings of 0.300-inch.

The Schottky-clamped versions offer considerable flexibility for upgrading existing designs or improving new designs as they feature improved performance; plus, they offer low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

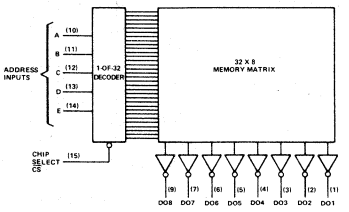
Data from a sequenced deck of data cards punched according to the specified format are permanently programmed by the factory into the monolithic structure for all bit locations. Upon receipt of the order, Texas Instruments will assign a special identifying number for each pattern programmed according to the order. The completed devices will be marked with the appropriate TI special device number. It is important that the customer specify not only the output levels desired at all bit locations, but also the other information requested under ordering instructions.

The three-state outputs offer the convenience of an open-collector output with the speed of a totem-pole output: they can be bus-connected to other similar outputs yet they retain the fast rise time characteristic of the TTL totem-pole output. The open-collector outputs offer the capability of direct interface with a data line having a passive pull-up.

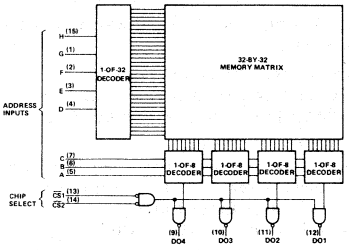
Word-addressing is accomplished in straight positive-logic binary and the memory may be read when all $\overline{CS}$ inputs are low. A high at any $\overline{CS}$ input causes the outputs to be off.

functional block diagrams

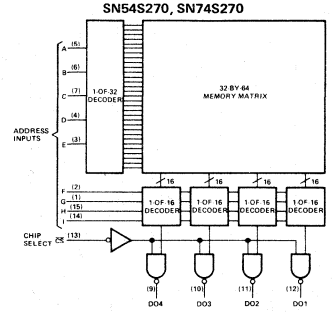
SN5488A, SN7488A



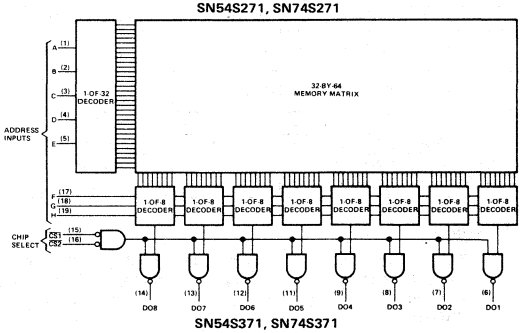
SN54187, SN74187



SN54S270, SN74S270

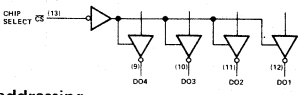


SN54S271, SN74S271



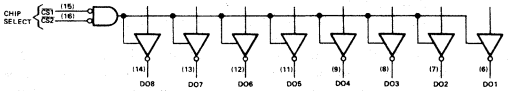
SN54S370, SN74S730

Same as SN54S270, SN74S270 except outputs are as shown below:



SN54S371, SN74S371

Same as SN54S271, SN74S271 except outputs are as shown below:



word addressing

'88A

WORD ADDRESS TABLE

WORD	INPUTS E	D	C	B	A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
	Words 9 thru 26 omitted				
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

'187, 'S271, 'S371

WORD ADDRESS TABLE

WORD	INPUTS H	G	F	E	D	C	B	A
0	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	H	L
3	L	L	L	L	L	L	H	H
4	L	L	L	L	L	H	L	L
5	L	L	L	L	L	H	L	H
6	L	L	L	L	L	H	H	L
7	L	L	L	L	L	H	H	H
8	L	L	L	L	H	L	L	L
	Words 9 thru 250 omitted							
251	H	H	H	H	H	L	H	H
252	H	H	H	H	H	H	L	L
253	H	H	H	H	H	H	L	H
254	H	H	H	H	H	H	H	L
255	H	H	H	H	H	H	H	H

'S270, 'S370

WORD ADDRESS TABLE

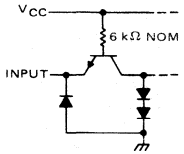
WORD	INPUTS I	H	G	F	E	D	C	B	A
0	L	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	L	H	L
3	L	L	L	L	L	L	L	H	H
4	L	L	L	L	L	L	H	L	L
5	L	L	L	L	L	L	H	L	H
6	L	L	L	L	L	L	H	H	L
7	L	L	L	L	L	L	H	H	H
8	L	L	L	L	L	H	L	L	L
	Words 9 thru 506 omitted								
507	H	H	H	H	H	H	L	H	H
508	H	H	H	H	H	H	H	L	L
509	H	H	H	H	H	H	H	L	H
510	H	H	H	H	H	H	H	H	L
511	H	H	H	H	H	H	H	H	H

Word selection is accomplished in a conventional positive-logic binary code with the A address input being the least-significant bit progressing alphabetically through the address inputs to the most-significant bit.

schematics of inputs and outputs

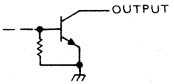
'88A, '187

EQUIVALENT OF EACH INPUT



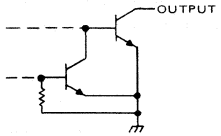
'88A

TYPICAL OF ALL OUTPUTS



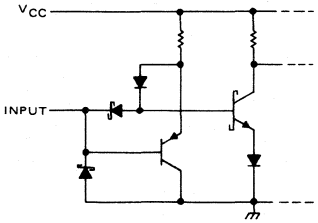
'187

TYPICAL OF ALL OUTPUTS



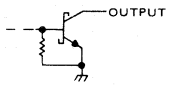
'S270, 'S271, 'S370, 'S371

EQUIVALENT OF EACH INPUT



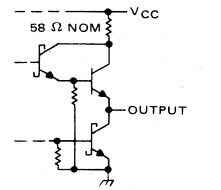
'S270, 'S271

TYPICAL OF ALL OUTPUTS



'S370, 'S371

TYPICAL OF ALL OUTPUTS



4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54', SN54S' Circuits (see Note 2)	−55°C to 125°C
SN74', SN74S' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54187 in the W package operating at free-air temperatures above 111°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 46°C/W.

recommended operating conditions

	SN5488A			SN7488A			SN54187			SN74187			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}			12			12			16			16	mA
Operating free-air temperature, T_A (see Note 2)	−55		125	0		70	−55		125	0		70	°C

NOTE 2: An SN54187 in the W package operating at free-air temperatures above 111°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 46°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'88A			'187			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			40			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA		0.2	0.4			0.4	V
			I_{OL} = 16 mA						0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			25			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1			−1	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		64	80		92	130	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 5 V,		6.5			6.5		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 3: With outputs open and $\overline{CS}$ input(s) grounded, I_{CC} is measured first by selecting a word that contains the maximum number of programmed high-level outputs, then by selecting a word that contains the maximum number of programmed low-level outputs.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'88A		'187		UNIT
			TYP	MAX	TYP	MAX	
$t_{a(ad)}$	Access time from address	C_L = 30 pF,	26	45	40	60	ns
$t_{a(\overline{CS})}$	Access time from chip select (enable time)	R_{L1} = 400 Ω ('88A) 300 Ω ('187)	22	35	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select (disable time)	R_{L2} = 600 Ω, See Figure 1	22	35	20	30	ns

recommended operating conditions

	SN54S270 SN54S271			SN74S270 SN74S271			SN54S370 SN54S371			SN74S370 SN74S371			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5							V
High-level output current, I_{OH}									−2			−6.5	mA
Low-level output current, I_{OL}			16			16			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'S270, 'S271			'S370, 'S371			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX				2.4			V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50				μA
			V_{OH} = 5.5 V			100				μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,						50	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,						−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX					−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 4		105	155		105	155	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 5 V,		6.5			6.5		pF

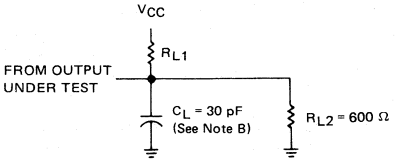
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 4: With outputs open and $\overline{CS}$ input(s) grounded, I_{CC} is measured first by selecting a word that contains the maximum number of programmed high-level outputs; then by selecting a word that contains the maximum number of programmed low-level outputs.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

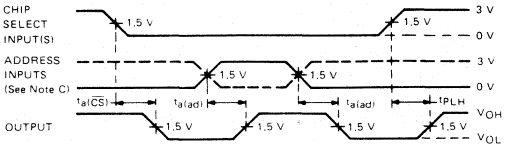
PARAMETER		TEST CONDITIONS	SN54270 SN54271		SN74270 SN74271		SN54370 SN54370		SN74370 SN74370		UNIT
			TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address	R_{L2} = 600 Ω, See Figure 1	45	95	45	70					ns
$t_{a(\overline{CS})}$	Access time from chip select (enable time)		15	45	15	30					ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select (disable time)		15	40	15	25					ns
$t_{a(ad)}$	Access time from address	C_L = 30 pF, See Figure 2					45	95	45	70	ns
$t_{a(\overline{CS})}$	Access time from chip select (enable time)						15	45	15	30	ns
t_{PXZ}	Disable time from high or low level	C_L = 5 pF, See Figure 2					10	40	10	25	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



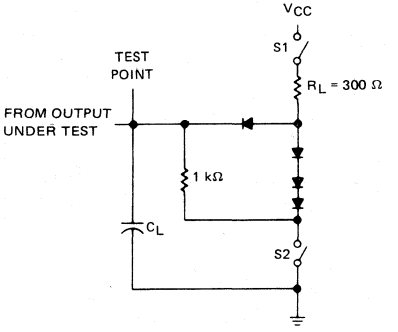
LOAD CIRCUIT



VOLTAGE WAVEFORMS

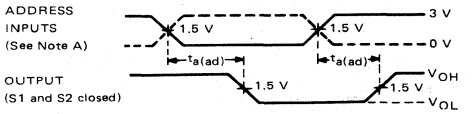
NOTES: A. The input pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$. For Series 54/74, $t_r \leq 7$ ns, $t_f \leq 7$ ns, for Series 54S/74S, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 1–SWITCHING TIMES OF '88A, '187, 'S270, AND 'S271 (OPEN-COLLECTOR OUTPUTS)

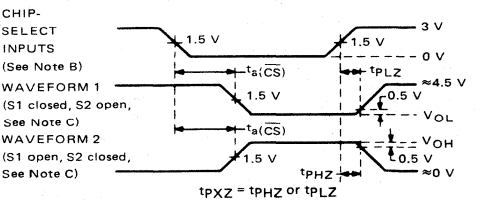


C_L includes probe and jig capacitance.
All diodes are 1N3064.

LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP SELECT VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the chip-select input(s) is(are) low.
B. When measuring access and disable times from chip-select input(s) the address inputs are steady-state.
C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

FIGURE 2–SWITCHING TIMES OF 'S370 AND 'S371 (3-STATE OUTPUTS)

ORDERING INSTRUCTIONS

Programming instructions for these read-only memories are solicited in the form of a sequenced deck of standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table for the requested part. This function table, showing output conditions for each of the words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the words specified and describes the levels at the outputs for each of those words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

The following information will be furnished to the customer by Texas Instruments:

a) TI part number
b) TI sales order number
c) Date received.

'88A DATA CARD FORMAT (32 CARDS)

Column	
1-2	Punch a right-justified integer representing the positive-logic binary input address (00-31) for the word described on the card.
3-4	Blank
5	Punch "H" or "L" for output Y8. H = high-voltage-level output, L = low-voltage-level output
6-9	Blank
10	Punch "H" or "L" for output DO 7.
11-14	Blank
15	Punch "H" or "L" for output DO 6.
16-19	Blank
20	Punch "H" or "L" for output DO 5.
21-24	Blank
25	Punch "H" or "L" for output DO 4.
26-29	Blank
30	Punch "H" or "L" for output DO 3.
31-34	Blank
35	Punch "H" or "L" for output DO 2.
36-39	Blank
40	Punch "H" or "L" for output DO 1.
41-49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "SN"
62-66	Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.
67-68	Blank
69-80	Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

'187 DATA CARD FORMAT (32 CARDS)

Column	
1- 3	Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.
8- 9	Blank

ORDERING INSTRUCTIONS

10-13 Punch "H", "L", or "X" for bits four, three, two, and one (outputs DO 4, DO 3, DO 2 and DO 1 in that order) for the first set of outputs specified on the card. H = high-voltage-level output, L = low-voltage-level output, X = output level irrelevant.

14 Blank

15-18 Punch "H", "L", or "X" for the second set of outputs.

19 Blank

20-23 Punch "H", "L", or "X" for the third set of outputs.

24 Blank

25-28 Punch "H" "L", or "X" for the fourth set of outputs.

29 Blank

30-33 Punch "H", "L", or "X" for the fifth set of outputs.

34 Blank

35-38 Punch "H", "L", or "X" for the sixth set of outputs.

39 Blank

40-43 Punch "H", "L", or "X" for the seventh set of outputs.

44 Blank

45-48 Punch "H", "L", or "X" for the eighth set of outputs.

49 Blank

50-51 Punch a right-justified integer representing the current calendar day of the month.

52 Blank

53-55 Punch an alphabetic abbreviation representing the current month.

56 Blank

57-58 Punch the last two digits of the current year.

59 Blank

60-61 Punch "SN"

62-66 Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.

67-68 Blank

69-80 Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

'S270, 'S370 DATA CARD FORMAT (64 CARDS)

Column

1-3 Punch a right-justified integer representing the binary input address (000-504) for the first set of outputs described on the card.

4 Punch a "—" (Minus sign)

5-7 Punch a right-justified integer representing the binary input address (007-511) for the last set of outputs described on the card.

8-80 Same as the '187 data card format.

'S271, 'S371 DATA CARD FORMAT (64 CARDS)

Column

1- 3 Punch a right-justified integer representing the binary input address (000-252) for the first set of outputs described on the card.

4 Punch a "—" (Minus sign)

5- 7 Punch a right-justified integer representing the binary input address (003-255) for the last set of outputs described on the card.

8- 9 Blank

10-17 Punch "H", "L", or "X" for bits eight, seven, six, five, four, three, two, and one (outputs DO 8, DO 7, DO 6, DO 5, DO 4, DO 3, DO 2, and DO 1 in that order) for the first set of outputs specified on the card. H = high-voltage-level output, L = low-voltage-level output, X = output level irrelevant.

18 Blank

19-26 Punch "H", "L", or "X" for the second set of outputs.

27 Blank

28-35 Punch "H", "L", or "X" for the third set of outputs.

36 Blank

37-44 Punch "H", "L", or "X" for the fourth set of outputs.

45-49 Blank

50-80 Same as the '187 data card format.

SN74S262N
ROW OUTPUT CHARACTER GENERATOR

features

- Static operation
- 5760 bit capacity
- 128 characters of 45 bits (5x9)
- 7 input character decoder
- 4 input row decoder
- Character format chosen to allow rounding on all characters
- High speed – 280ns character access time
- Lower power – 250mW
- Single + 5V supply
- 2 enable inputs for system expansion
- 20 pin DIL N-pack
- Compatible with most TTL and DTL logic circuits

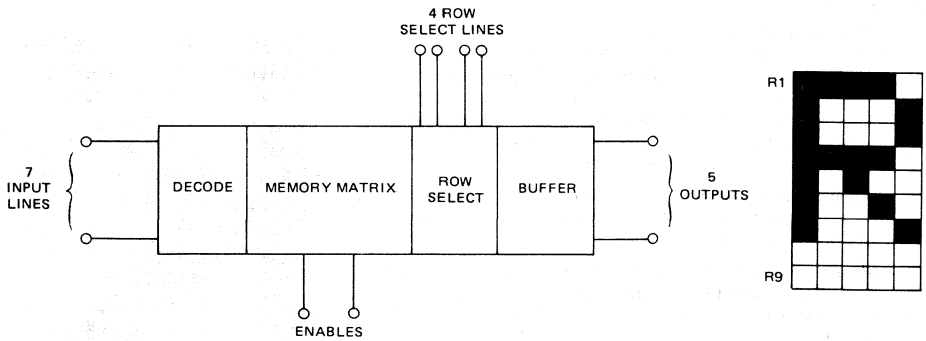
description

The SN74S262N Character Generator ROM is a fast, low power, dedicated IC developed by Texas Instruments Limited as part of the TIFAX Teletext decoder module, XM-11. The memory data is permanently stored by programming a single mask during manufacture, hence, other patterns can be provided.

The outputs are open collector, totempole or tri-state mask programmeable. The ROM is also mask programmable to inhibit outputs for invalid row addresses.

The SN74S262N specifically meets the needs of scanned video display systems. It can also be used in other ROM usages where it capacity, speed and low power features are of advantage.

functional diagram



operation

The SN74S262N series features static operation. No clocks are required. The output data will remain valid as long as the the input address (including chip enable) remains unchanged.

Access time is defined as the time required for all outputs to reach the minimum level, or maximum 0 level, with the correct data. This time is measured from the point at which all address inputs and chip enable inputs are valid.

SN74S262N
ROW OUTPUT CHARACTER GENERATOR

character scanning

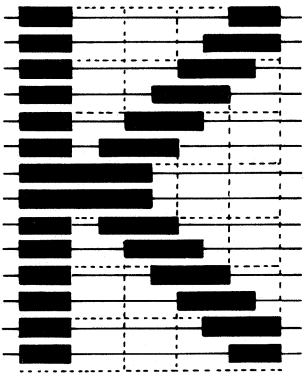
The output character appears as a 9-word sequence on each of the 5 output lines. The sequence is controlled by the 4 row-select lines. The five outputs represent a row in a 5 x 9 character matrix. The row address can remain fixed while the character address changes (scanned display), or the character address may remain fixed while the row address changes (x — y or character scan).

ROW SELECT TRUTH TABLE

ROW SELECT				SELECTS ROW
R_d	R_c	R_b	R_a	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	Data Outputs Forced to Logical '0'
to				
1	1	1	1	

character rounding

In scanned display systems using line interlacing, economy of design requires a repetition of the displayed ROM pattern on alternate lines. This results in coursely stepped diagonals which appear fainter than verticals or horizontals. A system which looks at the preceding or succeeding character row and interpolates intermediate extensions to the display, by reducing the coarseness of diagonals, makes the display visually more acceptable.



Methods requiring the reading of a character row and its preceding or succeeding row in one character display period, greatly reduce circuit complexity and component cost.

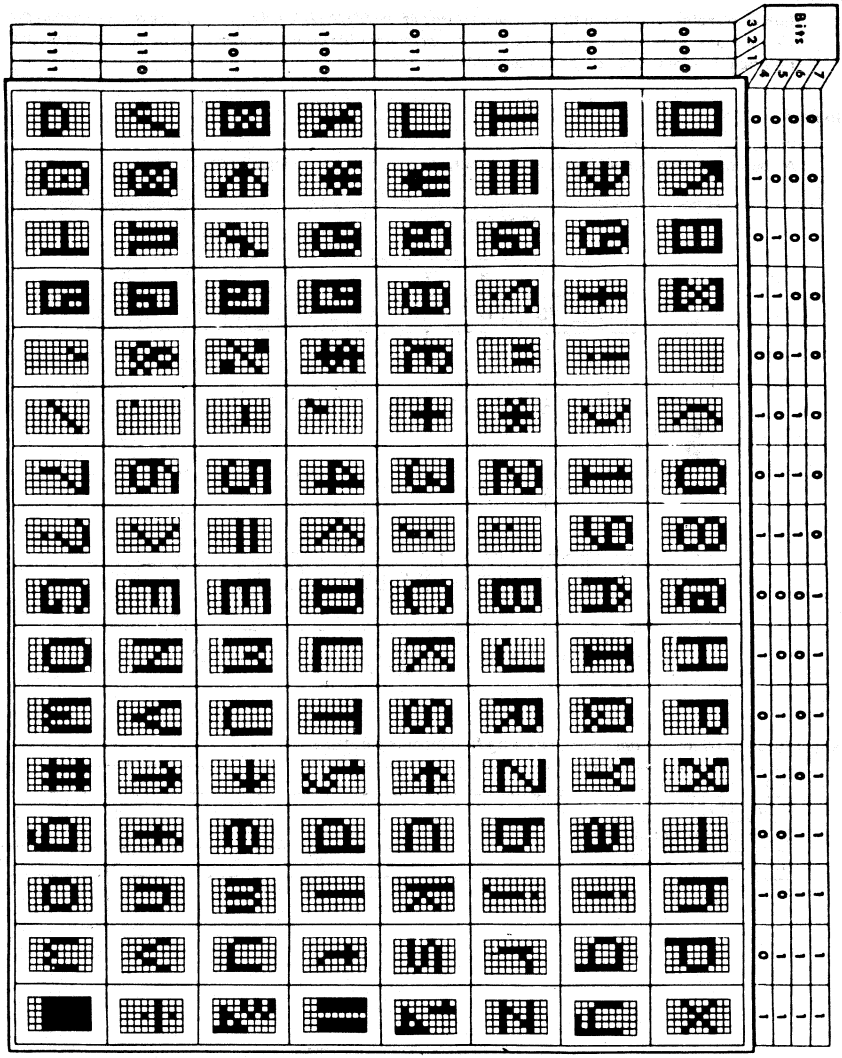
Teletext reception requires a 40 character display on a 625 line/50Hz system. This requires the ROM row access time to be better than about 400ns. The exact requirement is related to the speed and complexity of the associated logic.

Even with 80 characters/row, 625/525 line, 50/60Hz scanned VDU display systems, SN74S262N ROM is usable, especially since an improvement of its row access time specification is planned.

output buffers

The Teletext ROM, SN74S262N, has tri-state outputs.

SN74S262N ROM CHARACTER FORMAT



4

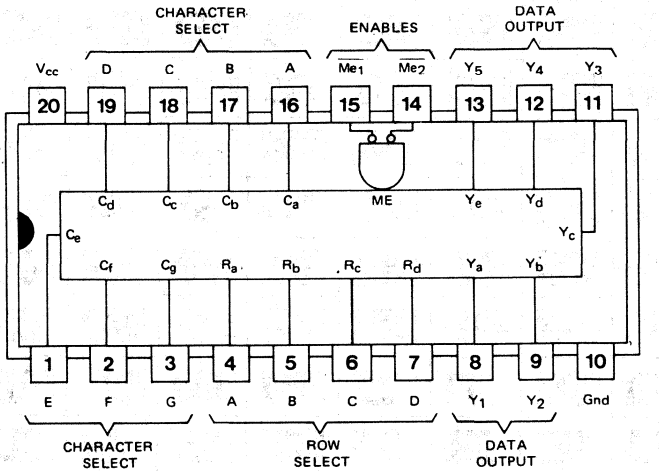
SN74S262N
ROW OUTPUT CHARACTER GENERATOR

chip enable

Both chip enable inputs need to be at logic 0 to enable the SN74S262N. The facility of two chip enables provides for the selection of one out of four ROMs. The mask programmable option of open collector or tri-state outputs makes it possible to wire OR the outputs of several ROMs.

logic definition

Positive logic is assumed on the inputs.
An output blank is defined as a logic 0. An output dot is defined as a logic 1 output level.



absolute maximum ratings over operating free-air temperature

Supply Voltage (V_{CC})	7V
Input Voltage	5.5V
Operating free air temperature	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
High Level Output Current $I_{(OH)}$			−1	mA
Low Level 'Output' Current $I_{(OL)}$			4	mA
Operating Free Air Temperature (T_A)	0		70	°C

electrical characteristics over recommended free air temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH} High level input voltage			2			V
V_{IL} Low level input voltage					0.8	V
V_{OH} High level output voltage	V_{IH} = 2V I_{OH} = -0.2mA	V_{CC} = MIN V_{IL} = 0.8V	2.7	3.4		V
V_{OL} Low level output voltage	V_{IH} = 2V I_{OL} = 4mA	V_{CC} = MIN V_{IL} = 0.8V			0.5	V
I_{IH} High level input current	V_{CC} = MAX	V_I = 2.7V			20	μA
I_{IL} Low level input current	V_{CC} = MAX	V_I = 0.4V			−360	μA
Output leakage	V_O = 2.7V	V_{IL} = 0.8V V_{IH} = 2V		20		μA
I_{CC} Supply current	V_{CC} = 5.0V			50		mA
Access time	Worst path			200	280	ns

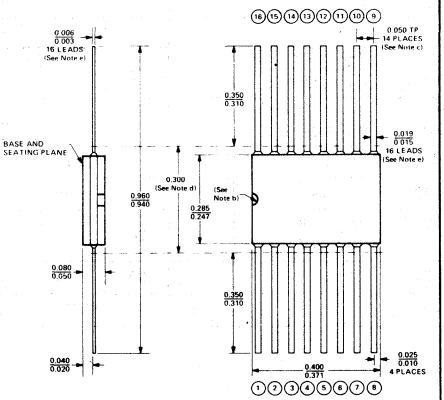
general

The availability of a particular TTL memory in a particular package is denoted by an alphabetical reference in a table on the data sheet for that type of memory, or above the pin-connection diagram. These letters refer to mechanical outline drawings shown in this section. Orders for these memories should include the package outline letter at the end of the circuit type number; e.g., SN54S287W, SN74S470J

W ceramic flat packages

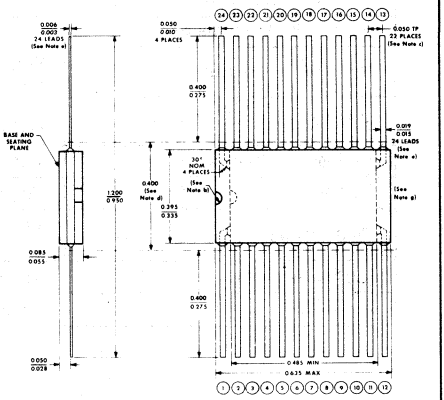
These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 16- or 24-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

16-PIN W CERAMIC



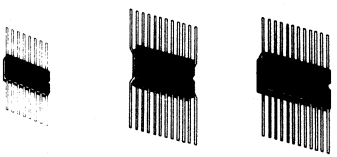
Falls Within
JEDEC MO-004AG Dimensions

24-PIN W CERAMIC



Falls Within
JEDEC MO-019AA Dimensions

NOTES:
a. All dimensions are in inches.
b. Index point is provided on cap for terminal identification only.
c. Leads are within 0.005 radius of true position (TP) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.
e. Not applicable for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area extends from lead tip to within 0.050 of package body.
g. End configuration of 24-pin package is at the option of TI.

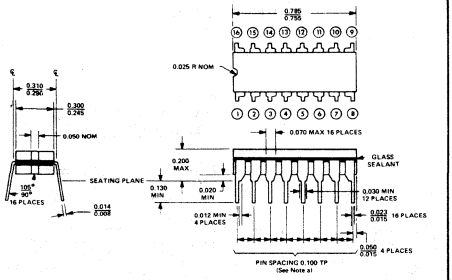


16 PIN | 24 PIN | 24 PIN

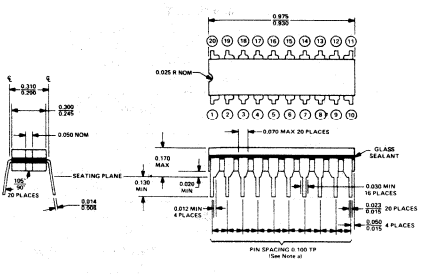
J ceramic dual-in-line packages

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 16-, 20-, or 24-lead frame. The packages are intended for insertion in mounting-hole rows on 0.300-inch or 0.600-inch centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

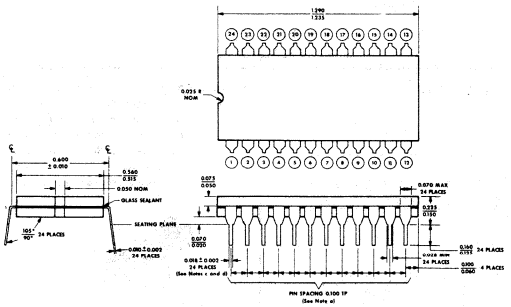
16-PIN J CERAMIC



20-PIN J CERAMIC

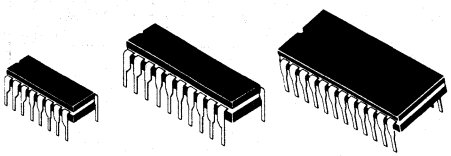


24-PIN J CERAMIC



Falls Within
JEDEC MO-015AA Dimensions

NOTES: a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.

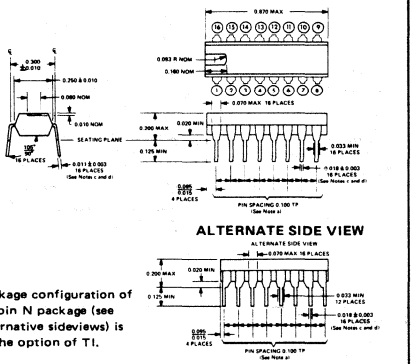


16-PIN 20-PIN 24-PIN

N plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a 16-, 20-, or 24-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300-inch or 0.600-inch centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

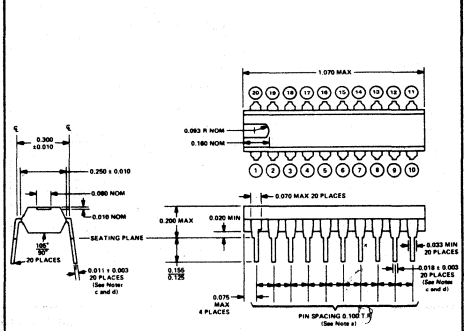
16-PIN N PLASTIC



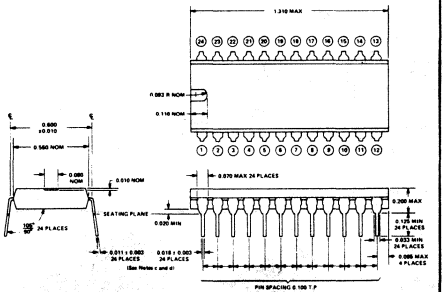
ALTERNATE SIDE VIEW

Package configuration of 16-pin N package (see alternative sideviews) is at the option of TI.

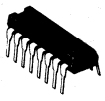
20-PIN N PLASTIC



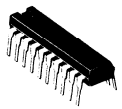
24-PIN N PLASTIC



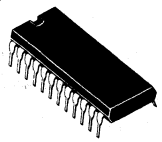
NOTES:
a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.



16-PIN



20-PIN



24-PIN

ECL Memories

BULLETIN NO. DL-S 7512255, MAY 1975

- Full On-Chip Address Decoding and Output-Sense Amplification
- Constant Current Drain Over a Wide Supply Voltage Range
- Logic Levels Compatible with Series SN10000 Logic Levels
- Compatible for Wired-OR Word Expansion

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SN10145	16 X 4 Bit Random-Access Memory	212
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Mechanical Data and Ordering Instructions		220

5

absolute maximum ratings over operating ambient temperature range† (unless otherwise noted)

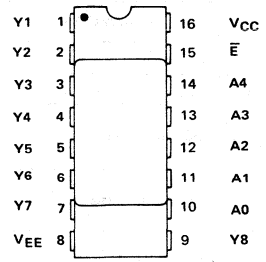
Supply voltage V_{EE} (see Note 1)	−7 V
Input voltage range	0 V to V_{EE}
Output current	−50 mA
Operating ambient temperature range	0°C to 85°C
Storage temperature range	−55°C to 125°C
Lead temperature 1/16 inch from case for 10 seconds	300°C

NOTE 1: Unless otherwise noted all voltage values are with respect to the V_{CC} terminals and all V_{CC} terminals must be connected in parallel.

†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

- 32-Word-by-Eight-Bit Organization
- Full On-Chip Address Decoding and Output-Sensing Amplification
- Capability for Wired-OR Connections
- Easy Programming

J OR JE
DUAL-IN-LINE PACKAGE (TOP VIEW)

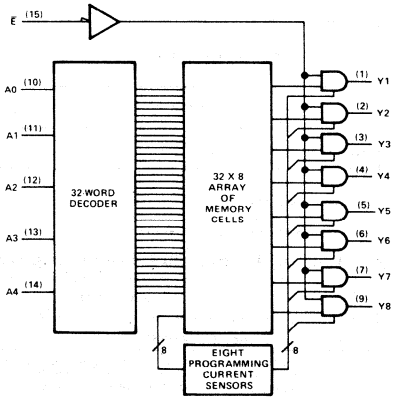


description

The SN10139 is a field-programmable, 256-bit read-only memory organized as 32 words of eight bits each. Full address decoding and output sense amplification are included on the chip. Each of the 32 words is addressed by the binary address inputs A0 through A4. The outputs Y1 through Y8 can be connected to other emitter-follower outputs to achieve wired-OR word expansion. An enable input, $\overline{E}$, is provided for ease in expansion. The device is enabled when the enable input is low. When the enable input is high, all outputs are forced low.

Data can be electronically programmed, as desired, at any of the 256 bit locations in accordance with the programming procedure specified. Prior to programming, the memory contains a low-logic-level output condition at all bit locations. The programming procedure open-circuits metal links, which results in a high-logic-level output at the selected locations. The procedure is irreversible; once altered, the output for that bit is permanently programmed to provide a high logic level. Outputs never having been altered may later be programmed to supply a high-level output. Operation of the device within the recommended operating conditions will not alter the memory content.

functional block diagram



recommended operating conditions

	B	NOM	A	UNIT
	(SEE NOTE 3)			
Supply voltage, V_{EE}	−5.72	−5.2	−4.68	V
Operating ambient temperature, T_A	0		85	°C

electrical characteristics at specified ambient temperature†

PARAMETER		TEST CONDITIONS (SEE NOTES 1 AND 2)		B	TYP	A	UNIT
				(SEE NOTE 3)			
V_{IH}	High-level input voltage		0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
$V_{IH'}$	High-level input voltage		0°C	−1145			mV
			25°C	−1105			
			85°C	−1035			
V_{IL}	Low-level input voltage		0°C	V_{EE}		−1645	mV
			25°C	V_{EE}		−1630	
			85°C	V_{EE}		−1595	
$V_{IL'}$	Low-level input voltage		0°C			−1490	mV
			25°C			−1475	
			85°C			−1440	
V_{OH}	High-level output voltage	$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1000		−840	mV
			25°C	−960		−810	
			85°C	−890		−700	
V_{OL}	Low-level output voltage	$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1870		−1665	mV
			25°C	−1850		−1650	
			85°C	−1825		−1615	
$V_{OH'}$	High-level output voltage	$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
$V_{OL'}$	Low-level output voltage	$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1870		−1645	mV
			25°C	−1850		−1630	
			85°C	−1825		−1595	
I_{IH}	High-level input current	V_I = −810 mV, Other inputs open	25°C			265	μA
I_{IL}	Low-level input current	V_I = −1850 mV, Other inputs open	25°C	0.5			μA
I_{EE}	Supply current	All inputs and outputs open	25°C	−145		−107	mA
		All inputs at −810 mV, All outputs open		−145		−110	

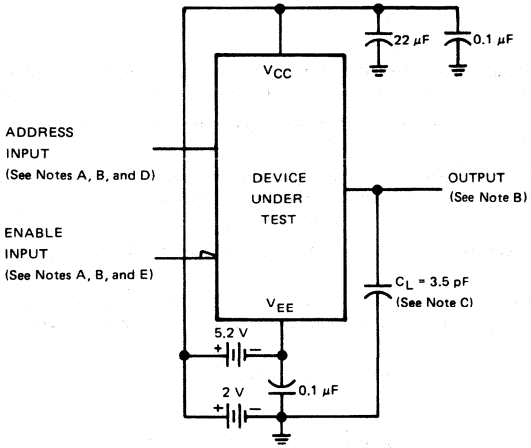
switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	B	A	UNIT
			(SEE NOTE 3)		
$t_{a(ad)}$	Access time from address	C_L = 3.5 pF, R_L = 50 Ω, See Figures 1 and 2		20	ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{E}$ (enable time)			15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{E}$ (disable time)			15	ns

NOTES: 1. All parameters are measured with V_{EE} = −5.200 V, V_{CC} = 0 V, and (unless otherwise noted) the output is connected to −2.000 V through 50 Ω.
2. Test conditions stating $V_{IH} = V_{IHB}$ (or $V_{IH'B}$) and/or $V_{IL} = V_{ILA}$ (or $V_{IL'A}$) mean that the high-level input voltages are equal to the B limit of V_{IH} (or $V_{IH'}$) specified for the particular temperature (see note 3) and/or the low-level input voltages are equal to the appropriate A limit of V_{IL} (or $V_{IL'}$). The output voltage limits are guaranteed for any appropriate combination of input conditions for the desired output.
3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

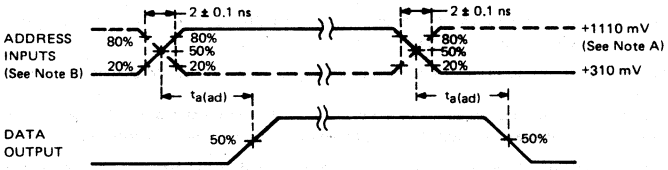
†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

PARAMETER MEASUREMENT INFORMATION

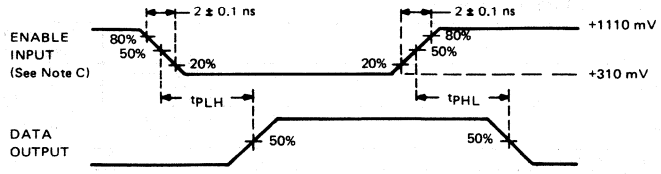


NOTES: A. The input waveforms are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 2 MHz. Transition times of input waveforms are 2 ± 0.1 ns between the 20% and 80% levels and are determined with no device in the socket.
B. The waveforms are monitored on an oscilloscope having the following characteristics: $t_r \leq 0.35$ ns, R_{in} = 50 Ω. Input and output cables are equal lengths of 50-Ω coaxial cable.
C. C_L includes jig capacitance.
D. All address lines not under test must be biased to select a memory cell.
E. If the enable line is not under test, it must be at a low logic level.

FIGURE 1–TEST CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS



ENABLE AND DISABLE TIMES

NOTES: A. Voltage values on input waveforms are with respect to ground.
B. The enable input is low.
C. The bit location addressed contains high-level data.

FIGURE 2–VOLTAGE WAVEFORMS

step-by-step programming procedure

manual

1. Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to 5.2 V. See Figure 3. Address the word to be programmed by applying to the appropriate address inputs 4 to 4.6 V for a high level and 0 to 1 V for a low level.
2. Raise V_{CC} (Pin 16) to 12 V. This level must not be maintained longer than 1 second. Maximum supply current during programming is 250 mA.
3. After V_{CC} has stabilized at 12 V (including any ringing that may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output corresponding to the bit to be programmed to a high.
4. Return V_{CC} to 5.2 V.
   CAUTION: To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at 12 V for more than 1 second.
5. Verify that the selected bit has programmed by connecting a 460-Ω resistor to ground and measuring the voltage at the output. If a high level ($V_O \geq 4.2$ V) is not detected at the output, the programming procedure should be repeated once.
6. If verification is positive, proceed to next bit to be programmed.

automatic

1. Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to 5.2 V. See Figure 3. Address the word to be programmed by applying to the appropriate address inputs 4 to 4.6 V for a high level and 0 to 1 V for a low level.
2. Raise V_{CC} (Pin 16) to 12 V. This level must not be maintained longer than 1 second. Maximum supply current during programming is 250 mA.
3. After a delay of 100 μs minimum, 1 ms maximum, apply a 2.5-mA current pulse to the output corresponding to the first bit to be programmed to a high. This output pulse is maintained between 0.5 and 1 ms. See Figure 4.
4. Repeat step 3 for each bit of the selected word specified as a high. (Program only one bit at a time; the delay between output programming pulses should not be greater than 1 ms.)
5. After all the desired bits of the selected word have been programmed, change address data and repeat the preceeding two paragraphs.
   NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissable for V_{CC} to remain at 12 V during the entire programming time.
6. After stepping through all address words, return V_{CC} to 5.2 V and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire programming procedure once.

recommended conditions for programming

		B	NOM	A (SEE NOTE 3)	UNIT
Supply voltage, V_{CC}	To program	11.5	12	12.5	V
	To verify	5	5.2	5.4	
Input voltage	High level	4		4.6	V
	Low level	0		1	
Output current during programming		2	2.5	3	mA
Programming pulse width, $t_{w(p)}$ (See Note 4)		0.5		1	ms
Programming pulse rise time				10	μs
Programming pulse delay (See Note 4)	Following V_{CC} change, $t_{d(1)}$	0.1		1	ms
	Between output pulses, $t_{d(2)}$	0.01		1	

NOTES: 3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.
4. These maximum times are specified to minimize the amount of time V_{CC} is at 12 V.

PROGRAMMING INFORMATION

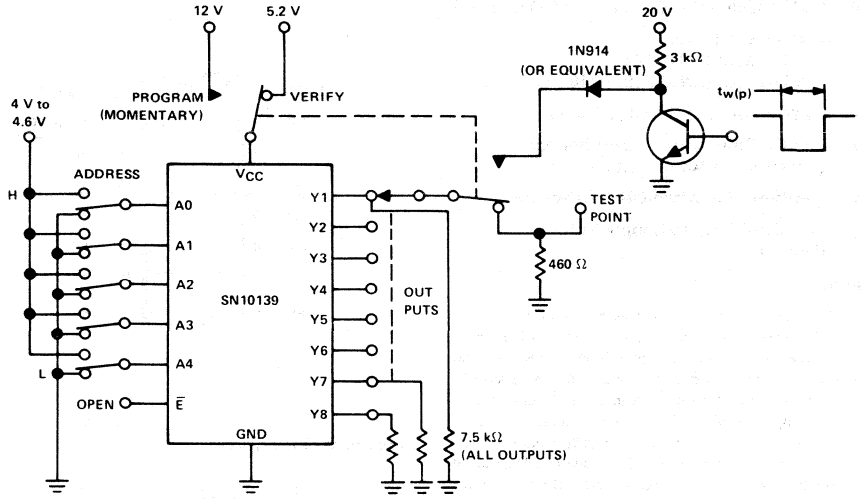


FIGURE 3–PROGRAMMING CIRCUIT

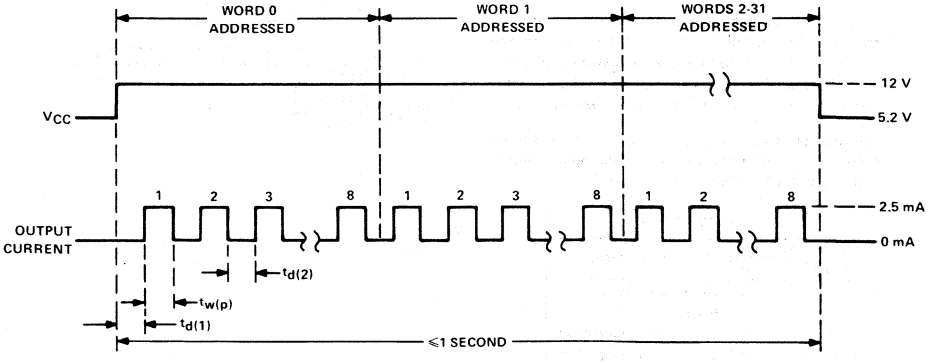


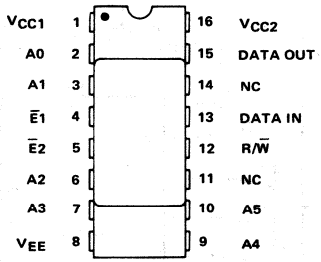
FIGURE 4–TIMING DIAGRAM FOR AUTOMATIC PROGRAMMING

TYPES SN10140, SN10142, SN10148
64-BIT RANDOM-ACCESS MEMORIES

MAY 1975

- SN10140 Drives 90-Ohm Loads
- SN10142 and SN10148 Drive 50-Ohm Loads
- Fast Access Times:
  10 ns Max (SN10142)
  15 ns Max (SN10140, SN10148)
- 64-Word-by-One-Bit Organization
- Full On-Chip Address Decoding and Output-Sense Amplification
- Capability for Wired-OR Connections
- Low Sensitivity to Supply Voltage Variation

J OR JE
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

These 64-bit active-element memories are monolithic, high-speed, emitter-coupled-logic (ECL) arrays of 64 storage cells organized to provide 64 words of one bit each. Full address decoding and output sense amplification are included on the chip. An additional level of decoding is provided for memory systems by the two enable inputs. Each of the 64 words is addressed by the binary address inputs A0 through A5. The output can be connected to other emitter-follower outputs to achieve wired-OR word expansion. The SN10140, SN10142, and SN10148 are fully compatible with the SN10000 logic family. The SN10148 and SN10142 are specified to meet SN10000 levels when driving 50-ohm loads and the SN10140 is specified to drive a 90-ohm load.

Information at the data input is written into the memory by addressing the desired word with the address lines and taking the read/write input low while both enable inputs are held low. The output is forced low while the memory is in the write mode.

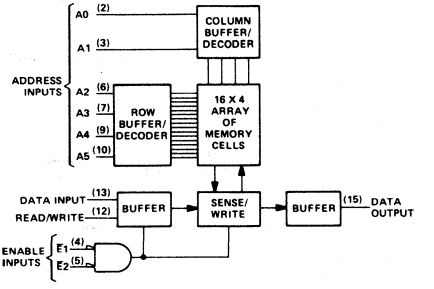
Information stored in the memory is read out by holding the read/write line high, selecting the desired address, and taking both enable inputs low.

FUNCTION TABLE

READ/ WRITE	ENABLE $\overline{E}1$	ENABLE $\overline{E}2$	OPERATION
L	L	L	Write (output low)
H	L	L	Read
X	H	X	Chip disabled (output low)
X	X	H	Chip disabled (output low)

H = high level, L = low level, X = irrelevant

functional block diagram



recommended operating conditions

		B	NOM	A (SEE NOTE 3)	UNIT
Supply voltage, V_{EE}		−5.72	−5.2	−4.68	V
Width of write pulse, $t_{w(wr)}$ (see Figure 9)		10			ns
Setup time, t_{su} (see Figure 9)	Address before write pulse	5			ns
	Enable before write pulse	3			
	Data before end of write pulse	10			
Hold time, t_h (see Figure 9)	Address after write pulse	3			ns
	Enable after write pulse	0			
	Data after write pulse	3			
Operating ambient temperature, T_A		0		85	°C

electrical characteristics at specified ambient temperature†

PARAMETER		TEST CONDITIONS (SEE NOTES 1 AND 2)		B	TYP	A (SEE NOTE 3)	UNIT
V_{IH} High-level input voltage			0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
$V_{IH'}$ High-level input voltage			0°C	−1145			mV
			25°C	−1105			
			85°C	−1035			
V_{IL} Low-level input voltage			0°C	V_{EE}		−1645	mV
			25°C	V_{EE}		−1630	
			85°C	V_{EE}		−1595	
$V_{IL'}$ Low-level input voltage			0°C			−1490	mV
			25°C			−1475	
			85°C			−1440	
V_{OH} High-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1000		−840	mV
			25°C	−960		−810	
			85°C	−890		−700	
V_{OL} Low-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−2000		−1665	mV
			25°C	−1990		−1650	
			85°C	−1920		−1615	
$V_{OH'}$ High-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
$V_{OL'}$ Low-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−2000		−1645	mV
			25°C	−1990		−1630	
			85°C	−1920		−1595	
I_{IH} High-level input current	Read/Write	$V_I = -810$ mV, Other inputs open	25°C			355	μA
	Other inputs					265	
I_{IL} Low-level input current		$V_I = -1990$ mV, Other inputs open	25°C	0.5			μA
I_{EE} Supply current		All inputs and the output open	25°C	−103		−85	mA

NOTES: 1. All parameters are measured with $V_{EE} = -5.200$ V, $V_{CC1} = V_{CC2} = 0$ V, and (unless otherwise noted) the output is connected to −2.000 V through 50 Ω for SN10142 and SN10148, or 90 Ω for SN10140.

2. Test conditions stating $V_{IH} = V_{IHB}$ (or $V_{IH'B}$) and/or $V_{IL} = V_{ILA}$ (or $V_{IL'A}$) mean that the high-level input voltages are equal to the B limit of V_{IH} (or $V_{IH'}$) specified for the particular temperature (see note 3) and/or the low-level input voltages are equal to the appropriate A limit of V_{IL} (or $V_{IL'}$). The output voltage limits are guaranteed for any appropriate combination of input conditions specified by the function table for the desired output.

3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

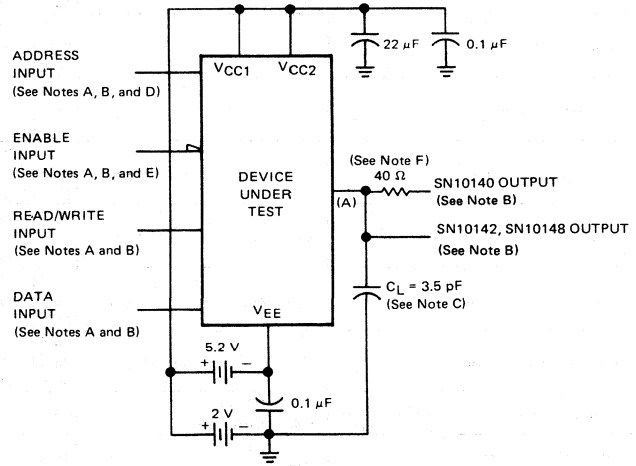
†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	SN10140 SN10148 (SEE NOTE 3)			SN10142 (SEE NOTE 3)			UNIT
			B	TYP	A	B	TYP	A	
$t_{a(ad)}$	Access time from address	C_L = 3.5 pF, R_L = 90 Ω (SN10140) 50 Ω (SN10142, SN10148), See Figures 5 and 9		10	15		8	10	ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{E}$ (enable time)			7	12		7	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{E}$ (disable time)			7	12		7	12	ns
t_{TLH}	Transition time, low-to-high-level output (20% to 80%)				2.5			2.5	ns
t_{THL}	Transition time, high-to-low-level output (80% to 20%)				2.5			2.5	ns
t_{SR}	Sense recovery time				10			10	ns

NOTE 3: This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less neagtive) limit; the B limit is the less positive (more negative) limit.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveforms are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 2 MHz. Transition times of input waveforms are 2 ± 0.1 ns between the 20% and 80% levels and are determined with no device in the socket.

B. The waveforms are monitored on an oscilloscope having the following characteristics: $t_r \leq 0.35$ ns, R_{in} = 50 Ω. Input and output cables are equal lengths of 50-Ω coaxial cable.

C. C_L includes jig capacitance.

D. All address lines not under test must be biased to select a memory cell.

E. Enable line(s) not under test must be at a low logic level.

F. 40-Ω external resistor shown is used for SN10140 only. When testing SN10142 or SN10148, connect point (A) directly to 50-Ω output cable.

FIGURE 5–TEST CIRCUIT

- Fast Access Time . . . 18 ns Typical
- 256-Word-by-One-Bit Organization
- Drives 50-Ohm Loads
- Full On-Chip Address Decoding and Output-Sense Amplification
- Capability for Wired-OR Connections
- Low Sensitivity to Supply Voltage Variation

description

This 256-bit active-element memory is a monolithic high-speed, emitter-coupled-logic (ECL) array of 256 storage cells organized to provide 256 words of one bit each. Full address decoding and output sense amplification are included on the chip. An additional level of decoding is provided for memory systems by the three enable inputs. Each of the 256 words is addressed by the binary address inputs A0 through A7. The output can be connected to other emitter-follower outputs to achieve wired-OR word expansion.

Information at the data input is written into the memory by addressing the desired word with the address lines and taking the read/write input low while all enable inputs are held low. The output is forced low while the memory is in the write mode.

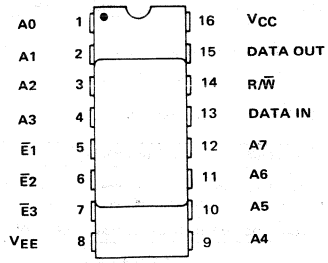
Information stored in the memory is read out by holding the read/write line high, selecting the desired address, and taking all enable inputs low.

FUNCTION TABLE

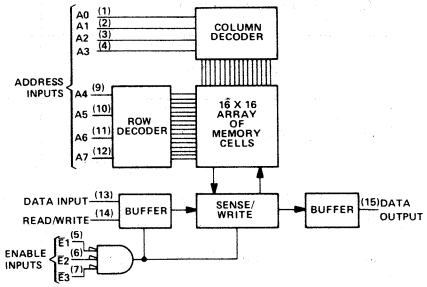
READ/ WRITE	ENABLE $\overline{E1}$	$\overline{E2}$	$\overline{E3}$	OPERATION
L	L	L	L	Write (output low)
H	L	L	L	Read
X	H	X	X	Chip disabled (output low)
X	X	H	X	Chip disabled (output low)
X	X	X	H	Chip disabled (output low)

H = high level, L = low level, X = irrelevant

J OR JE
DUAL-IN-LINE PACKAGE (TOP VIEW)



functional block diagram



5

recommended operating conditions

		B	NOM	A	UNIT
		(SEE NOTE 3)			
Supply voltage, V_{EE}		−5.72	−5.2	−4.68	V
Width of write pulse, $t_{w(wr)}$ (see Figure 9)		25			ns
Setup time, t_{su} (see Figure 9)	Address before write pulse	8			ns
	Enable before write pulse	2			
	Data before end of write pulse	27†			
Hold time, t_h (see Figure 9)	Address after write pulse	2			ns
	Enable after write pulse	2			
	Data after write pulse	2			
Operating ambient temperature, T_A		0		85	°C

†Note that this setup time is referenced to the end of the write pulse. With a minimum-width (25-ns) write pulse, this limit is equivalent to a 2-ns setup time referenced to the start of the write pulse. The setup-time requirement is thus made independent of write pulse width.

electrical characteristics at specified ambient temperature‡

PARAMETER		TEST CONDITIONS (SEE NOTES 1 AND 2)		B	TYP	A	UNIT
				(SEE NOTE 3)			
V_{IH} High-level input voltage			0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
$V_{IH'}$ High-level input voltage			0°C	−1145			mV
			25°C	−1105			
			85°C	−1035			
V_{IL} Low-level input voltage			0°C	V_{EE}		−1645	mV
			25°C	V_{EE}		−1630	
			85°C	V_{EE}		−1595	
$V_{IL'}$ Low-level input voltage			0°C			−1490	mV
			25°C			−1475	
			85°C			−1440	
V_{OH} High-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1000		−840	mV
			25°C	−960		−810	
			85°C	−890		−700	
V_{OL} Low-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1870		−1665	mV
			25°C	−1850		−1650	
			85°C	−1825		−1615	
$V_{OH'}$ High-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
$V_{OL'}$ Low-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1870		−1645	mV
			25°C	−1850		−1630	
			85°C	−1825		−1595	
I_{IH} High-level input current	$\overline{E}$ inputs	V_I = −810 mV, Other inputs open	25°C			265	µA
	Other inputs					50	
I_{IL} Low-level input current	$\overline{E}$ inputs	V_I = −1850 mV, Other inputs open	25°C	0.5			µA
	Other inputs			−50			
I_{EE} Supply current		All inputs and the output open	25°C	−125		−90	mA

NOTES: 1. All parameters are measured with V_{EE} = −5.200 V, V_{CC} = 0 V, and (unless otherwise noted) the output is connected to −2.000 V through 50 Ω.

2. Test conditions stating $V_{IH} = V_{IHB}$ (or $V_{IH'B}$) and/or $V_{IL} = V_{ILA}$ (or $V_{IL'A}$) mean that the high-level input voltages are equal to the B limit of V_{IH} (or $V_{IH'}$) specified for the particular temperature (see note 3) and/or the low-level input voltages are equal to the appropriate A limit of V_{IL} (or $V_{IL'}$). The output voltage limits are guaranteed for any appropriate combination of input conditions specified by the function table for the desired output.

3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

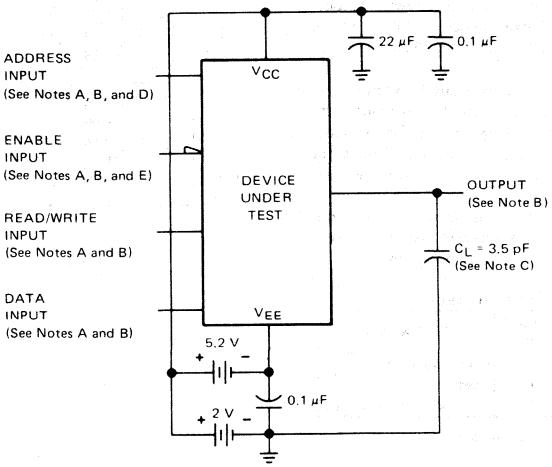
‡The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	B	TYP	A (SEE NOTE 3)	UNIT
$t_{a(ad)}$	Access time from address		C_L = 3.5 pF, R_L = 50 Ω, See Figures 6 and 9 and Note 4		18	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{E}$ (enable time)				8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{E}$ (disable time)				8	12	
t_{PHL}	Propagation delay time, high-to-low-level output from read/write				8	17	ns
t_{TLH}	Transition time, low-to-high-level output (20% to 80%)				2.5		ns
t_{THL}	Transition time, high-to-low-level output (80% to 20%)				2.5		
t_{SR}	Sense recovery time				8	17	ns
$t_{w(wr,min)}$	Minimum width of write pulse				15	25	ns
$t_{su(min)}$	Minimum setup time	Address before write pulse			−15	8	ns
		Enable before write pulse			−8	2	
		Data before end of write pulse			8	27	
$t_{h(min)}$	Minimum hold time	Address after write pulse			−3	2	ns
		Enable after write pulse			−8	2	
		Data after write pulse			−7	2	

NOTES: 3. This data sheet uses the algebraic limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.
4. Actual values for the minimum width of write pulse, the three minimum setup times, and the three minimum hold times can each be determined separately by setting the other six intervals at their A-limit values.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveforms are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 2 MHz. Transition times of input waveforms are 2 ± 0.1 ns between the 20% and 80% levels and are determined with no device in the socket.
B. The waveforms are monitored on an oscilloscope having the following characteristics: $t_r \leq 0.35$ ns, R_{in} = 50 Ω. Input and output cables are equal lengths of 50 Ω coaxial cable.
C. C_L includes jig capacitance.
D. All address lines not under test must be biased to select a memory cell.
E. Enable lines not under test must be at a low logic level.

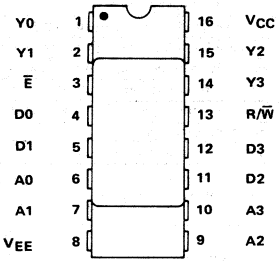
FIGURE 6—TEST CIRCUIT

TYPE SN10145
64-BIT RANDOM-ACCESS MEMORY

MAY 1975

- Fast Access Time . . . 9 ns Typical
- 16-Word-by-Four-Bit Organization
- Drives 50-Ohm Loads
- Full On-Chip Address Decoding and Output-Sense Amplification
- Capability for Wired-OR Connections
- Low Sensitivity to Supply Voltage Variation

J OR JE
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

This 64-bit active-element memory is a monolithic high-speed, emitter-coupled-logic (ECL) array of 64 storage cells organized to provide 16 words of four bits each. This organization and the high speed makes the SN10145 particularly useful in register file or small scratch-pad applications. Full address decoding and output sense amplification are included on the chip. Each of the 16 words is addressed by the binary address inputs A0 through A3. The output can be connected to other emitter-follower outputs to achieve wired-OR word expansion. The SN10145 is fully compatible with the SN10000 logic family.

Information at the data input is written into the memory by addressing the desired word with the address lines and taking the read/write input low while the enable input is held low. The output is forced low while the memory is in the write mode.

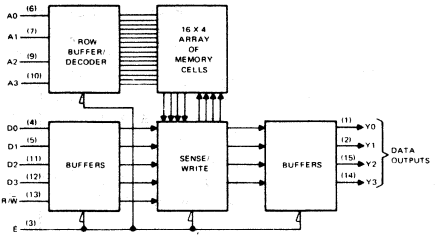
Information stored in the memory is read out by holding the read/write line high, selecting the desired address, and taking the enable input low.

FUNCTION TABLE

READ/WRITE R/W̄	ENABLE Ē	OPERATION
L	L	Write (output low)
H	L	Read
X	H	Chip disabled (output low)

H = high level, L = low level, X = irrelevant

functional block diagram



recommended operating conditions

		B	NOM	A	UNIT
		(SEE NOTE 3)			
Supply voltage, V_{EE}		−5.72	−5.2	−4.68	V
Width of write pulse, $t_{w(wr)}$ (see Figure 9)			7.5		ns
Setup time, t_{su} (see Figure 9)	Address before write pulse		3.5		ns
	Enable before write pulse		3		
	Data before end of write pulse		7.5		
Hold time, t_h (see Figure 9)	Address after write pulse		3.5		ns
	Enable after write pulse		3		
	Data after write pulse		3		
Operating ambient temperature, T_A		0		85	°C

electrical characteristics at specified ambient temperature†

PARAMETER		TEST CONDITIONS (SEE NOTES 1 AND 2)		B	A	UNIT
				(SEE NOTE 3)		
V_{IH} High-level input voltage			0°C	−1020	−840	mV
			25°C	−980	−810	
			85°C	−910	−700	
$V_{IH'}$ High-level input voltage			0°C	−1145		mV
			25°C	−1105		
			85°C	−1035		
V_{IL} Low-level input voltage			0°C	V_{EE}	−1645	mV
			25°C	V_{EE}	−1630	
			85°C	V_{EE}	−1595	
$V_{IL'}$ Low-level input voltage			0°C		−1490	mV
			25°C		−1475	
			85°C		−1440	
V_{OH} High-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1000	−840	mV
			25°C	−960	−810	
			85°C	−890	−700	
V_{OL} Low-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1870	−1665	mV
			25°C	−1850	−1650	
			85°C	−1825	−1615	
$V_{OH'}$ High-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1020	−840	mV
			25°C	−980	−810	
			85°C	−910	−700	
$V_{OL'}$ Low-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1870	−1645	mV
			25°C	−1850	−1630	
			85°C	−1825	−1595	
I_{IH} High-level input current	Any Data input	V_I = −810 mV, Other inputs open	25°C		220	μA
	Read/Write input				470	
	Any Address or $\overline{E}$ input				200	
I_{IL} Low-level input current		V_I = −1850 mV, Other inputs open	25°C	0.5		μA
I_{EE} Supply current		All inputs and outputs open	25°C	−150		mA

NOTES: 1. All parameters are measured with V_{EE} = −5.200 V, V_{CC} = 0 V, and (unless otherwise noted) the output is connected to −2.000 V through 50 Ω.

2. Test conditions stating $V_{IH} = V_{IHB}$ (or $V_{IH'B}$) and/or $V_{IL} = V_{ILA}$ (or $V_{IL'A}$) mean that the high-level input voltages are equal to the B limit of V_{IH} (or $V_{IH'}$) specified for the particular temperature (see note 3) and/or the low-level input voltages are equal to the appropriate A limit of V_{IL} (or $V_{IL'}$). The output voltage limits are guaranteed for any appropriate combination of input conditions specified by the function table for the desired output.

3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

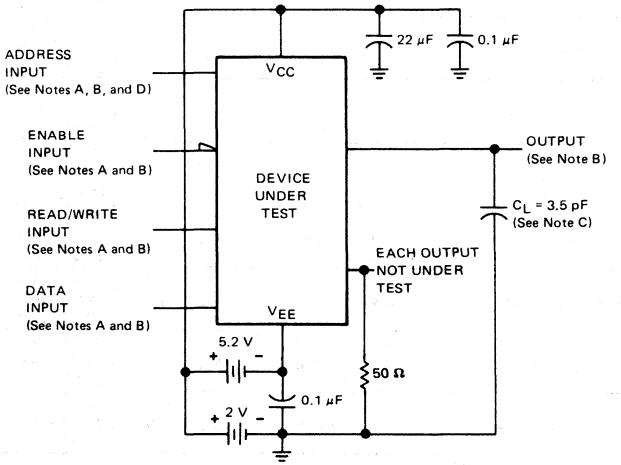
†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	B TYP A (SEE NOTE 3)	UNIT
$t_{a(ad)}$	Access time from address	C_L = 3.5 pF, R_L = 50 Ω, See Figures 7 and 9	6	ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{E}$ (enable time)		6	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{E}$ (disable time)		9	
t_{TLH}	Transition time, low-to-high-level output (20% to 80%)		2.5	ns
t_{THL}	Transition time, high-to-low-level output (80% to 20%)		2.5	
t_{SR}	Sense recovery time		7.5	ns

NOTE 3: This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveforms are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 2 MHz. Transition times of input waveforms are 2 ± 0.1 ns between the 20% and 80% levels and are determined with no device in the socket.

B. The waveforms are monitored on an oscilloscope having the following characteristics: $t_r \leq 0.35$ ns, R_{in} = 50 Ω. Input and output cables are equal lengths of 50-Ω coaxial cable.

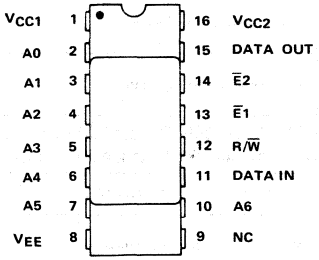
C. C_L includes jig capacitance.

D. All address lines not under test must be biased to select a memory cell.

FIGURE 7—TEST CIRCUIT

- Fast Access Time . . . 15 ns Maximum
- 128-Word-by-One-Bit Organization
- Full On-Chip Address Decoding and Output-Sense Amplification
- Capability for Wired-OR Connections
- Low Sensitivity to Supply Voltage Variation

J OR JE
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

This 128-bit active-element memory is a monolithic, high-speed, emitter-coupled-logic (ECL) array of 128 storage cells organized to provide 128 words of one bit each. Full address decoding and output sense amplification are included on the chip. An additional level of decoding is provided for memory systems by the two enable inputs. Each of the 128 words is addressed by the binary address inputs A0 through A6. The output can be connected to other emitter-follower outputs to achieve wired-OR word expansion.

Information at the data input is written into the memory by addressing the desired word with the address lines and taking the read/write input low while both enable inputs are held low. The output is forced low while the memory is in the write mode.

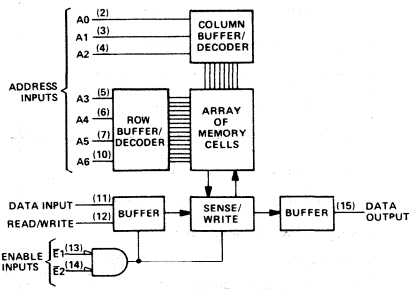
Information stored in the memory is read out by holding the read/write line high, selecting the desired address, and taking both enable inputs low.

FUNCTION TABLE

READ/ WRITE	ENABLE $\overline{E1}$	ENABLE $\overline{E2}$	OPERATION
L	L	L	Write (output low)
H	L	L	Read
X	H	X	Chip disabled (output low)
X	X	H	Chip disabled (output low)

H = high level, L = low level, X = irrelevant

functional block diagram



5

recommended operating conditions

		B	NOM (SEE NOTE 3)	A	UNIT
Supply voltage, V_{EE}		−5.72	−5.2	−4.68	V
Width of write pulse, $t_{w(wr)}$ (see Figure 9)		8			ns
Setup time, t_{su} (see Figure 9)	Address before write pulse	4			ns
	Enable before write pulse	1			
	Data before end of write pulse	8			
Hold time, t_h (see Figure 9)	Address after write pulse	3			ns
	Enable after write pulse	1			
	Data after write pulse	1			
Operating ambient temperature, T_A		0		85	°C

electrical characteristics at specified ambient temperature†

PARAMETER		TEST CONDITIONS (SEE NOTES 1 AND 2)		B	TYP (SEE NOTE 3)	A	UNIT
V_{IH} High-level input voltage			0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
$V_{IH'}$ High-level input voltage			0°C	−1145			mV
			25°C	−1105			
			85°C	−1035			
V_{IL} Low-level input voltage			0°C	V_{EE}		−1645	mV
			25°C	V_{EE}		−1630	
			85°C	V_{EE}		−1595	
$V_{IL'}$ Low-level input voltage			0°C			−1490	mV
			25°C			−1475	
			85°C			−1440	
V_{OH} High-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1000		−840	mV
			25°C	−960		−810	
			85°C	−890		−700	
V_{OL} Low-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−2000		−1665	mV
			25°C	−1990		−1650	
			85°C	−1920		−1615	
$V_{OH'}$ High-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
$V_{OL'}$ Low-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−2000		−1645	mV
			25°C	−1990		−1630	
			85°C	−1920		−1595	
I_{IH} High-level input current	Read/Write	$V_I = -810$ mV, Other inputs open	25°C			355	μA
	Other inputs					265	
I_{IL} Low-level input current		$V_I = -1990$ mV, Other inputs open	25°C	0.5			μA
I_{EE} Supply current		All inputs and the output open	25°C	−100	−85	−50	mA

NOTES: 1. All parameters are measured with $V_{EE} = -5.200$ V, $V_{CC1} = V_{CC2} = 0$ V, and (unless otherwise noted) the output is connected to −2.000 V through 50 Ω.

2. Test conditions stating $V_{IH} = V_{IHB}$ (or $V_{IH'B}$) and/or $V_{IL} = V_{ILA}$ (or $V_{IL'A}$) mean that the high-level input voltages are equal to the B limit of V_{IH} (or $V_{IH'}$) specified for the particular temperature (see note 3) and/or the low-level input voltages are equal to the appropriate A limit of V_{IL} (or $V_{IL'}$). The output voltage limits are guaranteed for any appropriate combination of input conditions specified by the function table for the desired output.

3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

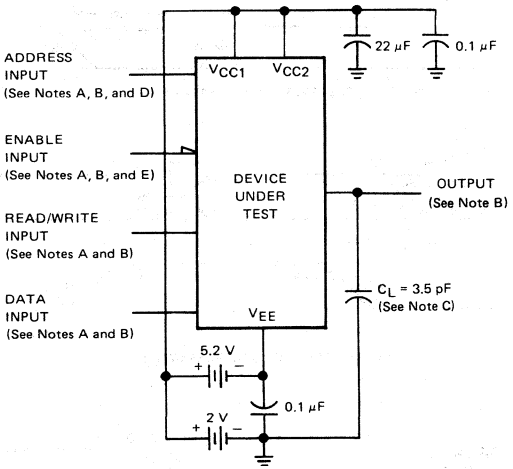
†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	B (SEE NOTE 3)	A (SEE NOTE 3)	UNIT
$t_{a(ad)}$	Access time from address	C_L = 3.5 pF, R_L = 50 Ω, See Figures 8 and 9		15	ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{E}$ (enable time)		3	8.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output from E (disable time)		3	8.5	
t_{TLH}	Transition time, low-to-high-level output (20% to 80%)		1	2.5	ns
t_{THL}	Transition time, high-to-low-level output (80% to 20%)		1	2.5	
t_{SR}	Sense recovery time			10	ns

NOTE 3: This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveforms are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 2 MHz. Transition times of input waveforms are 2 ± 0.1 ns between the 20% and 80% levels and are determined with no device in the socket.

B. The waveforms are monitored on an oscilloscope having the following characteristics: $t_r \leq 0.35$ ns, R_{in} = 50 Ω. Input and output cables are equal lengths of 50-Ω coaxial cable.

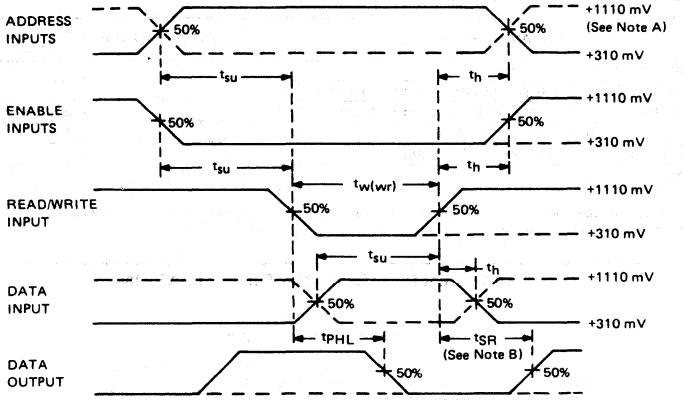
C. C_L includes jig capacitance.

D. All address lines not under test must be biased to select a memory cell.

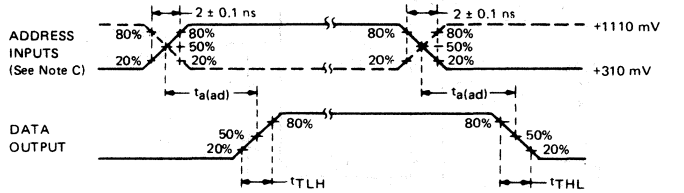
E. Enable line(s) not under test must be at a low logic level.

FIGURE 8—TEST CIRCUIT

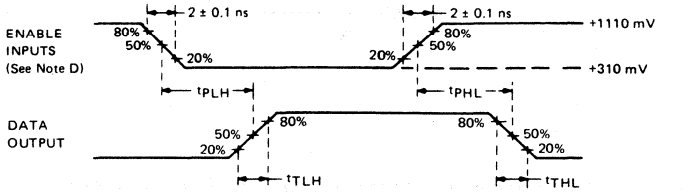
PARAMETER MEASUREMENT INFORMATION



WRITE CYCLE VOLTAGE WAVEFORMS



ACCESS TIME FROM ADDRESS INPUTS



ENABLE AND DISABLE TIMES

NOTES: A. Voltage values on input waveforms are with respect to ground.
B. Sense recovery time can only be measured following the writing of a high-level input.
C. All enable inputs are low, read/write input is high.
D. Read/write input is high, other enable input(s) is(are) low, bit location addressed contains high-level data.

FIGURE 9–VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS†

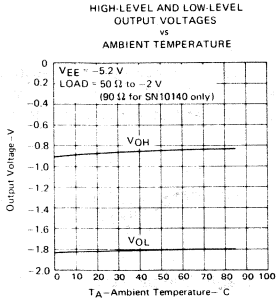


FIGURE 10

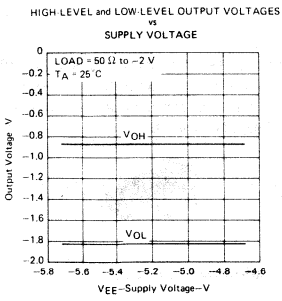


FIGURE 11

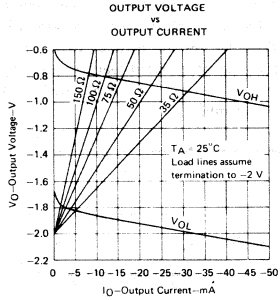


FIGURE 12

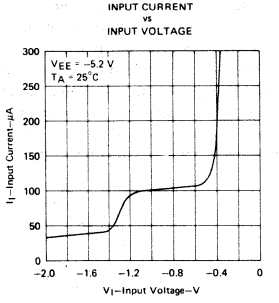


FIGURE 13

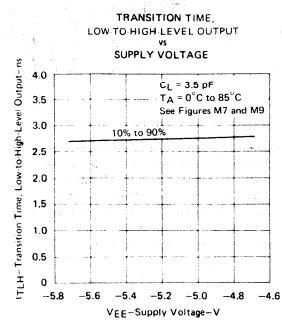


FIGURE 14

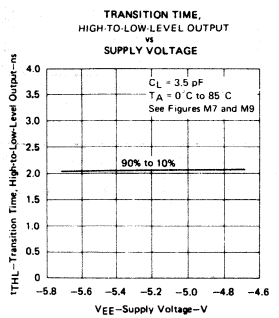


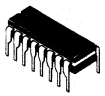
FIGURE 15

†The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

MECHANICAL DATA AND ORDERING INSTRUCTIONS

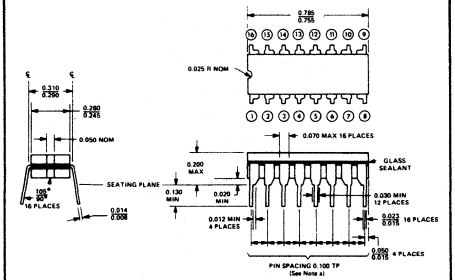
general

The availability of a particular Series SN10000 part in a particular package is denoted by an alphabetical reference above the pin-connection diagrams. Series SN10000 memories are available in the J and JE ceramic packages. Orders for these circuits should include the package outline letter(s) (J or JE) at the end of the circuit type number; e.g., SN10139J, SN10145JE.



J ceramic dual-in-line package

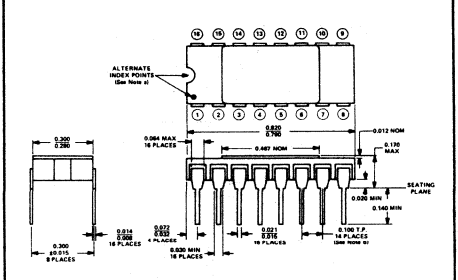
This hermetically sealed, dual-in-line package consists of a ceramic base, ceramic cap, and 16-lead frame. The package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (bright-dipped) leads require no additional cleaning or processing when used in soldered assembly.



NOTES: a. Each pin centerline is located within 0.010 inch of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.

JE ceramic dual-in-line package

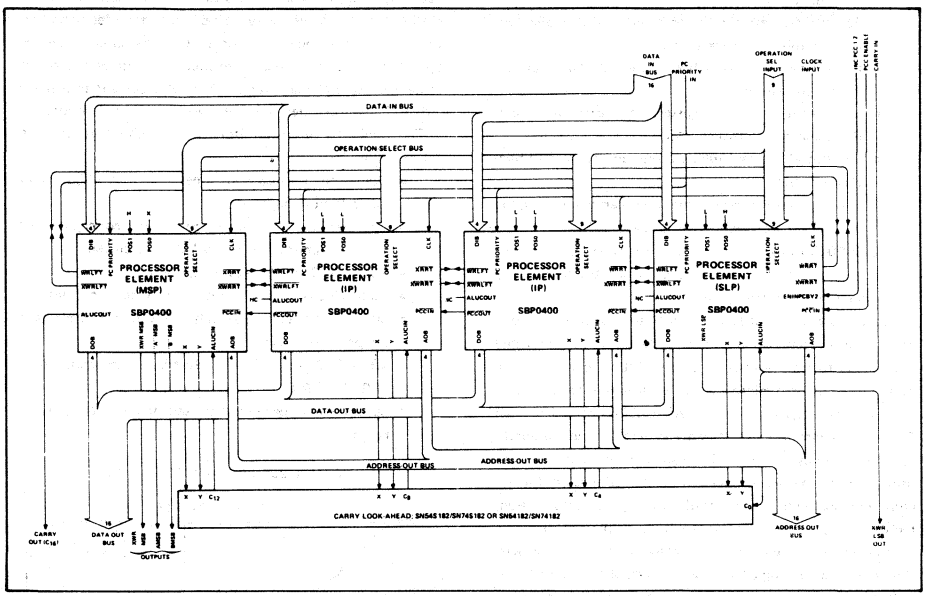
This ceramic dual-in-line package has 16 leads attached by brazing and a gold-plated lid hermetically sealed to the header at relatively low temperature using a solder preform. The package is intended for insertion in mounting-hole rows on 0.300-inch centers. The gold-plated leads require no additional cleaning or processing when used in soldered or welded assembly.



NOTES: a. Terminal identification is provided by either a notch with a nominal radius of 0.032 inch or a dot on the body near the number-one terminal.
b. Each pin centerline is located within 0.010 inch of its true longitudinal position.
c. All dimensions are in inches.

Microprocessors and Microcomputers

SBP0400
4-Bit Parallel
Binary Processor Element



Four SBP0400 Processor Elements Configured for 16-Bit Parallel Machine with Full Carry Look-Ahead

TENTATIVE DATA

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

SBP0400
4-BIT PARALLEL BINARY PROCESSOR ELEMENT

DESCRIPTION

The SBP0400 is a 4-bit parallel binary processor element monolithically integrating >1450 gates and mounted in a single 40-pin package. This versatile processor building block is implemented in a highly advanced bipolar technology which achieves a new level of performance/cost efficiency in the design and manufacture of digital processors.

Primary among the SBP0400's architectural features are:

- **Full parallel access to all control, data and address I/O functions**
- **16-operation arithmetic/logic unit (ALU) implemented with full carry look-ahead**
- **8-word general register file including program counter with incrementor**
- **Two 4-bit working registers for both single- and double-length operations**
- **Scaled-shifting multiplexers with end conditions handled on-chip**
- **On-chip control transformation generated by versatile factory programmable logic array (PLA).**

The SBP0400's logic is fully static and expandable in 4-bit multiples with full carry look-ahead for construction of any size processor or control element.

Featuring a powerful standard repertoire of 512 one-clock operations programmed into its PLA, the SBP0400 is designed specifically to provide a cost-effective solution to a wide range of applications from micro-controllers thru mini-computers to multi-processor systems. The added flexibility of designing an SBP0400 system to emulate other systems provides a significant cost-savings potential that can be realized through the utilization of existing software. Potential savings are further compounded by the economics of ultra-large scale integration, reduced package requirements, and reduced power levels.

Unlike processor elements containing fixed instruction sets, direct user sequencing of the operation set allows user synthesis/emulation of virtually any instruction/instruction set when sequential controls are provided. The functional power of the SBP0400 is characterized in its ability to perform, in a single clock cycle, any one of 459 nonredundant operations:

- **Operand modifications or combination via 8 arithmetic or 8 Boolean functions of the ALU**
- **Data transfers . . . register-to-memory, memory-to-register, register-to-register**
- **Single- or double-precision arithmetic shifts of single- or double-signed binary words**
- **Single- or double-precision logical shifts or circulates**
- **Single-clock ALU/shift combinations to simplify implementation of single- or double-signed iterative multiply and non-restore divide algorithms**
- **Additional features include:**
  - **Instruction "Look-ahead" capability to overlap instruction fetch and execute**
  - **Relative position control establishes "End" conditions for definition of multifunction pins.**

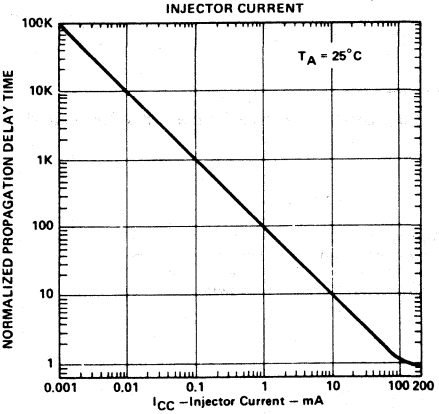
INTEGRATED INJECTION LOGIC, I^2L

I^2L is a highly efficient new bipolar technology which reduces a basic gate function to a single current injected transistor switch. The logical simplicity of a single geometry gate requiring no isolation, no load resistors and no ground metalization, achieves gate component densities 10 times those of conventional TTL or CMOS. I^2L circuits can be operated along a virtually constant speed/power product value over several magnitudes of injector current to achieve either nanosecond speeds or microwatt power dissipation.

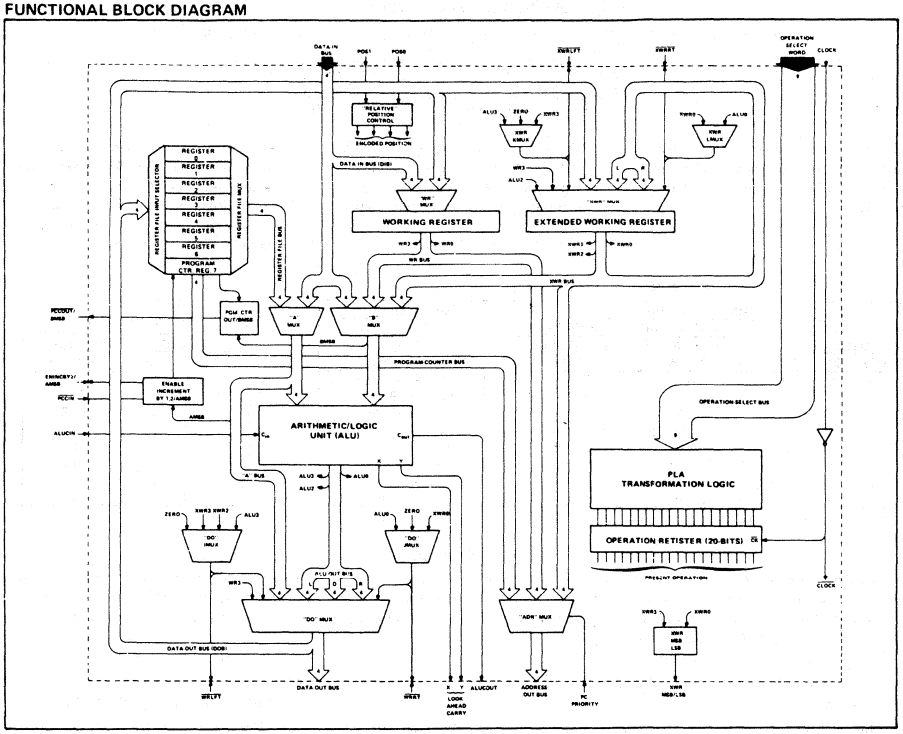
The SBP0400 utilizes non-isolated I^2L technology with the following results:

- **Operation propagation times . . . 110-530 ns at 128 mW nominal power**
- **Operates from a single power source capable of +0.85 V minimum at desired injector current**
- **Static, D. C. edge-triggered operation**
- **Fully TTL compatible at nominal injector current**
- **SBP0400M operates over full –55°C to 125°C military temperature range**
- **SBP0400C operates over industrial temperature range of 0°C to 70°C**
- **Speed/power performance selectable over a wide range.**

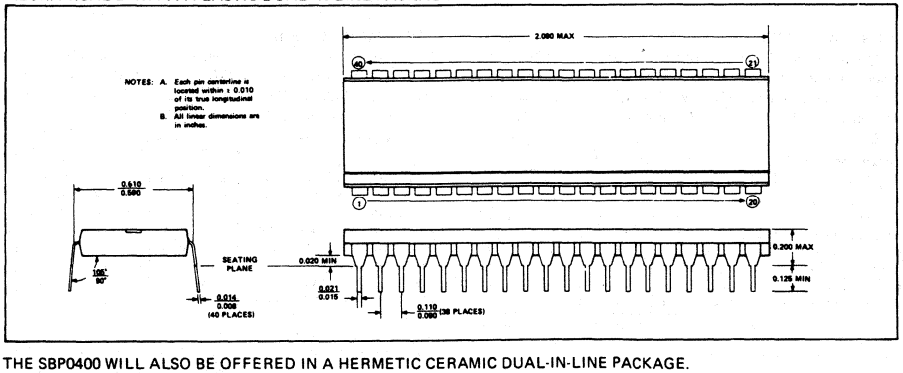
SBP0400
NORMALIZED PROPAGATION DELAY TIME
vs
INJECTOR CURRENT



FUNCTIONAL BLOCK DIAGRAM



MECHANICAL DATA . . . PLASTIC DUAL-IN-LINE PACKAGE



THE SBP0400 WILL ALSO BE OFFERED IN A HERMETIC CERAMIC DUAL-IN-LINE PACKAGE.

OPERATION-SELECT WORD

The 9-bit operation-select word consists of the 4 bit OP, 2-bit D, and 3 bit S fields as illustrated:

OP-FIELD				D-FIELD		S-FIELD		
X	X	X	X	X	X	X	X	X
OP3	OP2	OP1	OP0	D1	D0	S2	S1	S0

OP-FIELD . . . Primarily defines the 8 arithmetic and 8 logical operations associated with ALU functions defined below.

D-FIELD . . . In addition to stipulating the single- or double-precision word length, this field assimilates and extends the interactivity of the operation-select word.

S-FIELD . . . Primarily defines operation source (DIB, RF, WR, XWR) and destinations (DOB, RF, WR, XWR, AOB). Register file selections for operations form I through IV are shown below.

ALU FUNCTION-SELECT TABLE

ARITHMETIC OPERATIONS				LOGIC OPERATIONS
ALU SELECTION			ACTIVE-HIGH DATA (OP3 = L)	ACTIVE-HIGH DATA
OP2	OP1	OP0	ALUCIN = H (WITH CARRY)	ALUCIN = L (NO CARRY)	OP3 = H, ALUCIN = X
0	0	0	Fn = Low	Fn = High	Fn = AnBn
0	0	1	Fn = B − A	Fn = B − A − 1	Fn = An ⊕ Bn
0	1	0	Fn = A − B	Fn = A − B − 1	Fn = $\overline{An}$ ⊕ $\overline{Bn}$
0	1	1	Fn = A plus B plus 1	Fn = A plus B	Fn = $\overline{AnBn}$
1	0	0	Fn = B plus 1	Fn = B	Fn = $\overline{AnBn}$
1	0	1	Fn = $\overline{B}$ plus 1	Fn = $\overline{B}$	Fn = An + $\overline{Bn}$
1	1	0	Fn = A plus 1	Fn = A	Fn = $\overline{An}$ + Bn
1	1	1	Fn = $\overline{A}$ plus 1	Fn = $\overline{A}$	Fn = An + Bn

NOTE: Positive logic is used throughout: 1 = high, 0 = low.

REGISTER-FILE SELECTION TABLE

S-FIELD			REGISTER
S2	S1	S0	SELECT
0	0	0	RF0
0	0	1	RF1
0	1	0	RF2
0	1	1	RF3
1	0	0	RF4
1	0	1	RF5
1	1	0	RF6
1	1	1	PC

OPERATION SETS

In order to maximize the efficiency of available transformation logic, interactivity between the three fields is best categorized by six operation forms. These six powerful operations, forms I → VI, represent 45 flexible operation types. Combining the operation types with the ALU functions and eight RF combinations results in 459 unique, one-clock, operations. The remaining 53 are redundant operations. The six operation forms are:

I. A (ALU) B → A or B or C

II. A plus B plus ALUCIN → A or B or C

III. A → B

IV. (WR +/− A plus ALUCIN) SHIFTED · WR

V. (WR plus ALUCIN) SHIFTED → WR

VI. (WR plus ALUCIN, XWR) SHIFTED → (WR, XWR)

When a form I through form IV operation type specifies the RF as an operand source and/or destination, the operation-select word S-field selects a particular RF register to be utilized in execution of the operation as shown above.

OPERATION FORM I

Operation form I can be utilized to perform 1 of 16 ALU functions, selected by the Operation-Select Word OP-field, on 2 of 4 operand sources, (RF, WR, XWR, DIB). The result is transferred to 1 of 4 operand destinations (RF, WR, XWR, DOB).

OPERATION TYPE	OPERATION FORM I							
RF ALU WR → RF	ALU: 0000 → 1111	0	0	RF: 000 → 111				
RF ALU WR → WR	ALU: 0000 → 1111	0	1	RF: 000 → 111				
*DIB ALU WR → DOB	ALU: 0000 → 1111	1	1	0	0	0		
*DIB ALU WR → WR	ALU: 0000 → 1111	1	1	0	0	1		
DIB ALU XWR → WR	ALU: 0000 → 1111	1	1	0	1	1		
DIB ALU WR → XWR	ALU: 0000 → 1111	1	1	1	0	0		
DIB ALU XWR → XWR	ALU: 0000 → 1111	1	1	1	1	0		
DIB ALU XWR → DOB	ALU: 0000 → 1111	1	1	1	1	1		
	OP3 → OP0	D1	D0	S2	S1	S0		

NOTE: When PC PRIORITY is low WR → AOB.
*XWR → AOB.

OPERATION FORM II

Operation form II can be utilized to arithmetically sum 1 or 2 operand sources (RF, WR, XWR, DIB) and a ripple-carry-in (ALUCIN). The result is transferred to 1 of 4 operand destinations (RF, WR, XWR, DOB).

OPERATION TYPE	OPERATION FORM II									
RF plus WR plus ALUCIN *XWR	0	0	1	1	1	0	RF: 000 → 111			
RF plus DIB plus ALUCIN →WR	0	1	0	0	1	0	RF: 000 → 111			
RF plus DIB plus ALUCIN *XWR	0	1	0	1	1	0	RF: 000 → 111			
RF plus DIB plus ALUCIN →RF	0	1	1	1	1	0	RF: 000 → 111			
RF plus XWR plus ALUCIN *WR	1	1	0	0	1	0	RF: 000 → 111			
RF plus XWR plus ALUCIN *XWR	1	1	0	1	1	0	RF: 000 → 111			
XWR plus ALUCIN →RF	1	1	1	0	1	0	RF: 000 → 111			
DIB plus WR plus ALUCIN *XWR	0	0	1	1	1	1	0	1	0	
DIB plus WR plus ALUCIN *DOB	0	1	1	1	1	1	0	1	0	
DIB plus XWR plus ALUCIN *WR	1	1	0	0	1	1	0	1	0	
DIB plus XWR plus ALUCIN *XWR	1	1	0	1	1	1	0	1	0	
XWR plus ALUCIN *DOB	1	1	1	0	1	1	0	1	0	
	OP3 → OP0			D1	D0		S2	S1	S0	

OPERATION FORM III

Operation form III can be utilized to transfer 1 of 2 operand sources (RF, DIB) to 1 of 4 operand destinations (RF, WR, XWR, DOB).

OPERATION TYPE	OPERATION FORM III										
DIB → RF	1	1	1	1	1	0	RF: 000 → 111				
RF → DOB	0	0	0	0	1	0	RF: 000 → 111				
RF → XWR	0	0	0	1	1	0	RF: 000 → 111				
DIB → WR	0	1	1	0	1	0	X	X	X		
	0	1	1	0	1	1	0	1	0		
DIB → XWR	0	0	0	1	1	1	0	1	0		
DIB → DOB	1	1	1	1	1	1	0	1	0		
	0	0	0	0	1	1	0	1	0		
	OP3	→	OP0		D1	D0	S2	S1	S0		

OPERATION FORM IV

Operation form IV can be utilized to either:

- arithmetically sum the WR and the ripple carry-in (ALUCIN) with 1 of 2 operand sources (RF, DIB), arithmetically double-precision shift the result to the right, and transfer the shifted result to the WR and XWR;
- arithmetically sum the WR and the ripple carry-in (ALUCIN) with 1 of 2 operand sources (RF, DIB), double-precision circulate the result to the left, and transfer the circulated result to the WR and XWR;
- arithmetically subtract 1 of 2 operand sources (RF, DIB) and −1 from the WR, arithmetically add the ripple carry-in (ALUCIN), double-precision circulate the result to the left, and transfer the circulated result to the WR and XWR.

OPERATION TYPE	OPERATION FORM IV										
(WR − DIB − 1 plus ALUCIN) LCIR → WR, XWR	1	0	0	0	1	1	0	1	0		
(WR plus DIB plus ALUCIN) LCIR → WR, XWR	1	0	0	1	1	1	0	1	0		
(WR − RF − 1 plus ALUCIN) LCIR → WR, XWR	1	0	0	0	1	0	RF: 000 → 111				
(WR plus RF plus ALUCIN) LCIR → WR, XWR	1	0	0	1	1	0	RF: 000 → 111				
(WR plus ALUCIN) RSA → WR, XWR	1	0	1	0	1	0	X	X	X		
	1	0	1	0	1	1	0	1	0		
(WR − DIB − 1 plus ALUCIN) RSA → WR, XWR	0	0	1	0	1	1	0	1	0		
(WR plus DIB plus ALUCIN) RSA → WR, XWR	1	0	1	1	1	1	0	1	0		
(WR − RF − 1 plus ALUCIN) RSA → WR, XWR	0	0	1	0	1	0	RF: 000 → 111				
(WR plus RF plus ALUCIN) RSA → WR, XWR	1	0	1	1	1	0	RF: 000 → 111				
	OP3	OP0		D1	D0		S2	S1	S0		

OPERATION FORM V

Operation form V can be utilized to perform single-precision shifts on the contents of the WR, placing the result in the WR. The WR may be logically shifted left or right (LSL, RSL), arithmetically shifted left or right (LSA, RSA), or circulated left or right (LCIR, RCIR). In operation form V shifts, the MSB of the ALU is utilized as the sign-bit.

As the WR is passed through the ALU during form V and VI the ALUCIN is active and should be held at a low logic level for true shifts.

OPERATION TYPE	OPERATION FORM V										
(WR plus ALUCIN) RSA → WR	0	0	0	0	1	1	1	0	1		
(WR plus ALUCIN) RCIR → WR	0	0	0	1	1	1	1	0	1		
	1	0	0	1	1	1	1	0	1		
(WR plus ALUCIN) LSA → WR	0	0	1	0	1	1	1	0	1		
(WR plus ALUCIN) LCIR → WR	0	0	1	1	1	1	1	0	1		
	1	0	1	1	1	1	1	0	1		
(WR plus ALUCIN) RSL → WR	1	0	0	0	1	1	1	0	1		
(WR plus ALUCIN) LSL → WR	1	0	1	0	1	1	1	0	1		
	OP3	→	OP0		D1	D0	S2	S1	S0		

OPERATION FORM VI

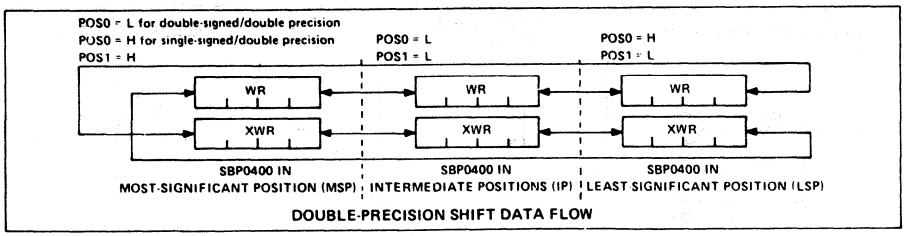
Operation form VI can be utilized to perform double-precision shifts on the contents of WR in conjunction with XWR. The WR in conjunction with the XWR may be:

- logically shifted left or right (LSL, RSL);
- arithmetically shifted left or right (LSA, RSA) single- or double-signed;
- circulated left or right (LCIR, RCIR).

In OPERATION FORM VI arithmetic shifts, the MSB of the ALU is utilized as the sign bit. For single signed arithmetic shifts the MSB of the ALU is placed in the MSB of the WR. For double signed arithmetic shifts, the MSB of the ALU is placed in the MSBs of both the WR and XWR.

OPERATION TYPE	OPERATION FORM VI										
(WR plus ALUCIN, XWR) RSA → (WR, XWR)	0	1	0	0	1	1	1	0	1		
(WR plus ALUCIN, XWR) RICR → (WR, XWR)	0	1	0	1	1	1	1	0	1		
	1	1	0	1	1	1	1	0	1		
(WR plus ALUCIN, XWR) LSA → (WR, XWR)	0	1	1	0	1	1	1	0	1		
(WR plus ALUCIN, XWR) LCIR → (WR, XWR)	0	1	1	1	1	1	1	0	1		
	1	1	1	1	1	1	1	0	1		
(WR plus ALUCIN, XWR) RSL → (WR, XWR)	1	1	0	0	1	1	1	0	1		
(WR plus ALUCIN, XWR) LSL → (WR, XWR)	1	1	1	0	1	1	1	0	1		
	OP3	OP0		D1	D0		R2	R1	R0		

In an expanded system, double-precision shift data flows as shown below.



DOUBLE-PRECISION SHIFT DATA FLOW

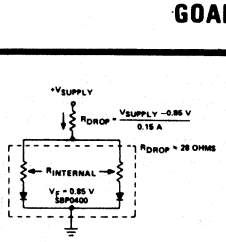
absolute maximum ratings (over operating free-air temperature range, unless otherwise noted)

Injector current, I_{CC} . . . . . 170 mA
Input voltage (see Note 1) . . . . . 4 V
Off-state output voltage . . . . . 4 V
Operating free-air temperature range:
SBP0400M . . . . . −55°C to 125°C
SBP0400C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SBP0400 power source

The SBP0400 can be operated from any d-c power source, voltage or current, capable of supplying the desired operating current at a minimum of +0.85 volts. A simple current source is shown in the adjacent diagram. In this example a 5-volt power supply and 150 mA nominal injector current have been selected for high-speed performance with full TTL compatibility. This ohm's law solution applies for calculating the dropping resistor value for any combination of supply voltage and injector current.



recommended operating conditions

		SBP0400M			SBP0400C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply current, I_{CC}		135	150	165	140	150	160	mA
High-level output voltage, V_{OH}				3.3			3.3	V
Low level output current, I_{OL}	Any AOB, X, Y, or ALUCOUT			20			20	mA
	Any DOB, or XWR MSB/LSB			10			10	
	$\overline{XWRLFT}$, $\overline{XWRRT}$, $\overline{WRRT}$, $\overline{WRLFT}$, $\overline{PCCOUT}$/BMSB, ENINCBY 2/AMSB			5			5	
Width of clock pulse, $t_{w(clock)}$	High	750			750			ns
	Low	250			250			
Setup time, t_{setup} (any input)		200†			200†			ns
Hold time, t_{hold} (any input)		0†			0†			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

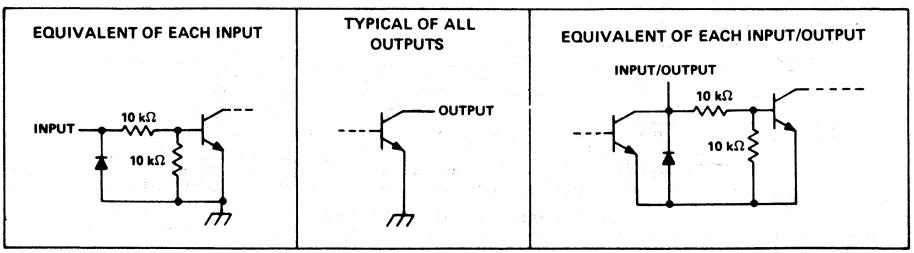
†Rising edge of clock pulse is reference.

electrical characteristics (over recommended operating free-air temperature range, unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SBP0400M			SBP0400C			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		I_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High-level output current		I_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 3.3 V			400			250	μA
V_{OL}	Low-level output voltage		I_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX		0.2	0.4		0.2	0.4	V
I_I	Input current	Clock, $\overline{PCCIN}$	I_{CC} = MAX,	V_I = 3.3		500	750		500	750	μA
		All other inputs				250	375		250	375	

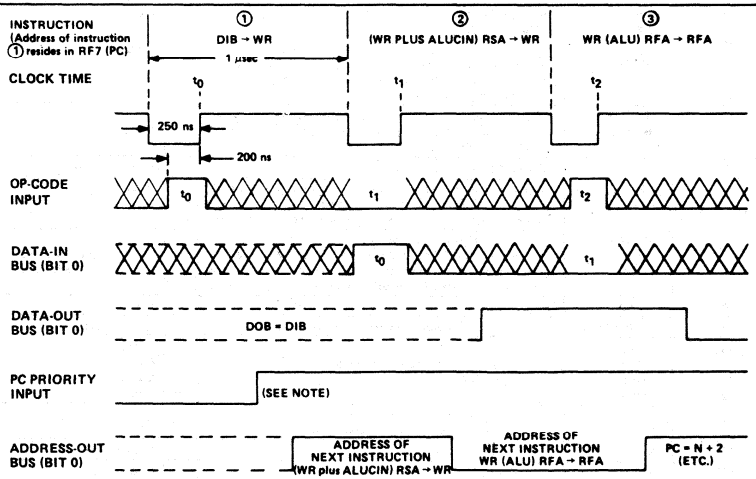
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at I_{CC} = 150 mA, T_A = 25°C.

SCHEMATICS OF EQUIVALENT INPUTS, OUTPUTS, INPUTS/OUTPUTS



switching characteristics (I_{CC} = 150 mA, T_A = 25°C)

PARAMETER	FROM	TO	TEST CONDITIONS	TYPICAL	UNIT
t_{PLH} or t_{PHL}	DIB	DOB	VIA A BUS, BYPASS ALU	250	ns
t_{PLH} or t_{PHL}	DIB	DOB	VIA A BUS, THRU ALU	380	ns
t_{PLH} or t_{PHL}	DIB	DOB	VIA B BUS, THRU ALU	500	ns
t_{PLH} or t_{PHL}	PC PRIORITY	AOB		180	ns
t_{PLH} or t_{PHL}	ALUCIN	ALUCOUT		180	ns
t_{PLH} or t_{PHL}	DIB	ENINCBY2/AMSB	POS0 = X, POS1 = H	180	ns
t_{PLH} or t_{PHL}	DIB	$\overline{\text{PCCOUT}}$/BMSB	POS0 = X, POS1 = H	250	ns
t_{PLH} or t_{PHL}	POS0, or POS1	ENINCBY2/AMSB or $\overline{\text{PCCOUT}}$/BMSB		180	ns
t_{PLH} or t_{PHL}	$\overline{\text{PCCIN}}$	$\overline{\text{PCCOUT}}$		110	ns
t_{PLH} or t_{PHL}	ALUCIN	DOB		310	ns
t_{PLH} or t_{PHL}	CLOCK	$\overline{\text{PCCOUT}}$/BMSB	POS0 = X, POS1 = H	350	ns
t_{PLH} or t_{PHL}	CLOCK	DOB	VIA A BUS, BYPASS ALU	350	ns
t_{PLH} or t_{PHL}	CLOCK	DOB	VIA A BUS, THRU ALU	500	ns
t_{PLH} or t_{PHL}	CLOCK	ENINCBY2/AMSB	POS0 = X, POS1 = H	280	ns
t_{PLH} or t_{PHL}	CLOCK	DOB	VIA B BUS, THRU ALU	530	ns
t_{PLH} or t_{PHL}	CLOCK	X, Y, or ALUCOUT	VIA A OR B BUS, THRU ALU	440	ns
t_{PLH} or t_{PHL}	CLOCK	AOB		350	ns
t_{PLH} or t_{PHL}	CLOCK	$\overline{\text{WRLFT}}$, $\overline{\text{WRRT}}$, $\overline{\text{XWRLFT}}$, or $\overline{\text{XWRRT}}$		500	ns
t_{PLH} or t_{PHL}	CLOCK	XWR MSB	POS0 = H, POS1 = H	350	ns
t_{PLH} or t_{PHL}	CLOCK	XWR LSB	POS0 = H, POS1 = L	350	ns



A typical sequence of operations shows:

1. Op-code instruction (DIB → WR) is setup and clocked into operation register (OR) at t_0 transition. Advance program counter (PC by 1 for next address.
2. At t_1 execute DIB → WR and fetch address of next instruction.
3. At t_2 execute (WR plus ALUCIN) RSA → WR and fetch address of next instruction.

NOTE: When taken high the PC priority input overrides any OR instruction and routes program-counter (PC) contents to AOB. PC can be incremented by the clock to generate next address at the AOB.

TYPICAL SEQUENCE FOR SBP0400

6

FUNCTIONAL DESCRIPTION

PIN NUMBER	PIN NAME	PIN FUNCTION	INPUT, OUTPUT, OR INPUT/OUTPUT
1	D1	2-bit, "D" field of the Operation-Select Word.	Input
2	D0		Input
3	S2	3-bit, "S" field of the Operation-Select Word designates, in general, a particular RF as an operand source/destination.	Input
4	S1		Input
5	S0		Input
6	$\overline{\text{XWRLFT}}$	Bidirectional I/O, low active, shift accommodation for the XWR. Receives double-precision right-shift data; outputs double-precision left-shift data. Becomes XWRLFT (high active) internally.	Bidirectional Input/output
7	$\overline{\text{XWRRT}}$	Bidirectional I/O, low active, shift accommodation. Receives double-precision left-shift data; outputs double precision right-shift data. Becomes XWRRT (high active) internally.	Bidirectional Input/output
8	XWR MSB/LSB	MSB of the XWR if in the most-significant 4-bit-slice position (MSP) and LSB if in the least-significant 4-bit slice position (LSP)	Output
9	$\overline{\text{WRRT}}$	Bidirectional I/O, low active, shift accommodation for ALU output data. Receives left-shift data. Outputs right-shift data. Becomes WRRT (high active) internally.	Bidirectional Input/output
10	$\overline{\text{WRLFT}}$	Bidirectional I/O, low active, shift accommodation for ALU output data. Receives right-shift data; outputs left-shift data. Becomes WRLFT (high active) internally.	Bidirectional Input/output
11	ALUCIN	Receives, high active, ALU ripple carry-in data.	Input
12	DOB0	4-bit, parallel, high active, data-out bus. (DOB3 → DOB0)	Output
13	DOB1		Output
14	DOB2		Output
15	DOB3		Output
16	DIB3	4-bit, parallel, high active, data-in bus. (DIB3 → DIB0)	Input
17	DIB2		Input
24	DIB1		Input
25	DIB0		Input
18	$\overline{\text{PCCIN}}$	In all position, directs the program counter to increment by 1 or 2, depending on the level applied to ENINCBY2, on the next low-to-high clock transition.	Input
19	$\overline{\text{PCCOUT}}$/ BMSB	In any position but MSP, $\overline{\text{PCCOUT}}$ is the program counter output applied to the next more significant package $\overline{\text{PCCIN}}$. In the MSP, outputs the MSB of the "B" bus.	Output
20	GND	Common or ground terminal	Supply common
21	POS0	Directs internal and input/output end-conditions required to define the relative position of each SBP0400 when a number is cascaded to implement > 4-bit word lengths. See double-precision shift data flow.	Input
22	POS1		Input
23	ENINCBY2/ AMSB	In the least-significant 4-bit slice position (LSP), ENINCBY2 = H in conjunction with $\overline{\text{PCCIN}}$ = L directs the PROGRAM COUNTER to increment by a displacement of 2 on the next clock. In the most-significant 4-bit slice position (MSP), outputs the MSB of the "A" BUS.	Bidirectional Input/output (LSP) (MSP)
26	CLOCK	Clock	Input
27	INJECTOR 1	One of two supply current sources. Connect to pin 40.	Supply input
28	AOB3	4-bit, parallel, high active, address-out bus (AOB3 → AOB0)	Output
29	AOB2		Output
31	AOB1		Output
32	AOB0		Output
30	PC PRIORITY	Selects program counter to the address-out bus (high active). Overrides internal direction of address-out bus.	Input
33	X	ALU carry-propagate	Output
34	Y	ALU carry-generate	Output
35	ALUCOUT	Outputs, high active, ALU ripple carry-out data	Output
36	OP3	This 4-bit, "OP" field of the Operation-Select Word designates in general, 1 of 16 ALU functions.	Input
37	OP2		Input
38	OP1		Input
39	OP0		Input
40	INJECTOR 2	One of two supply current sources. Connect to pin 27.	Supply input

TMS1000 Series

MOS/LSI
One-Chip Microcomputers

1. THE ONE-CHIP MICROCOMPUTERS FROM TEXAS INSTRUMENTS

1.1 DESCRIPTION

The TMS 1000 series is a family of P-channel MOS four-bit microcomputers with a ROM, a RAM, and an arithmetic logic unit on a single semiconductor chip. The TMS 1000 family is unique in the field of microprocessors because this device is a single-chip binary computer. A customer's specification determines the software that is reproduced during wafer processing by a single-level mask technique that defines a fixed ROM pattern. As summarized in Table 1, the TMS 1000 and TMS 1200 are the basic 1024-instruction ROM microcomputers. The TMS 1070 and TMS 1270 interface directly to high-voltage displays and use instructions identical to the TMS 1000/1200 devices. To increase the software capacity in one chip, the TMS 1100 and TMS 1300 provide twice the ROM and RAM size of the TMS 1000/1200.

The design support for the entire series includes software assembler and simulator, hardware simulator with debug control, and system evaluator devices for prototype fabrication.

TABLE 1
4-BIT MICROCOMPUTER FEATURES

	TMS 1000	TMS 1200	TMS 1070	TMS 1270	TMS 1100	TMS 1300
Package Pin Count	28 Pins	40 Pins	28 Pins	40 Pins	28 Pins	40 Pins
Instruction Read Only Memory	1024 X 8 Bits (8,192 Bits)		1024 X 8 Bits (8,192 Bits)		*2048 X 8 Bits (16,384 Bits)*	
Data Random Access Memory	64 X 4 Bits (256 Bits)		64 X 4 Bits (256 Bits)		*128 X 4 Bits (512 Bits)*	
"R" Individually Addressed Output Latches	11	13	11	13	11	*16*
"O" Parallel Latched Data Outputs	8 Bits		8 Bits	*10 Bits	8 Bits	
Maximum-Rated Voltage (O, R, and K)	20 V		*35 V*		20 V	
Working Registers	2-4 Bits Each		2-4 Bits Each		2-4 Bits Each	
Instruction Set	See Table 2, Page 9		See Table 2, Page 9		See Table 3, Page 15	
Programmable Instruction Decoder	Yes		Yes		Yes	
On-Chip Oscillator	Yes		Yes		Yes	
Power Supply/Typical Dissipation	15 V/90 mW		15 V/90 mW		15 V/105 mW	
Time-Share Assembler Support	Yes		Yes		Yes	
Time-Share Simulator Support	Yes		Yes		Yes	
Hardware Evaluator and Debugging Unit	HE-2		HE-2		HE-2	
System Evaluator Device with External Instruction Memory	SE-1 (TMS 1099 JL)		SE-1 (TMS 1099 JL)		SE-2 (TMS 1098 JL)	

*The HE 2 does not have a decoder for the extra O outputs.

1.2 DESIGN SUPPORT

Through a staff of experienced application programmers, Texas Instruments will, upon request, assist customers in evaluating applications, in training designers to program the TMS 1000 series, and in simulating programs. TI will also contract to write programs to customer's specifications.

TI developed assemblers and simulators for aiding software designs. These assembler and simulator programs are available on nationwide time-sharing systems and at TI computer facilities.

A TMS 1000 series program (see flowchart, Figure 1) is written in assembly language using standard mnemonics. The assembler converts the source code (assembly language program) into machine code, which is transferred to a software simulation program. Also, the assembler produces a machine code object deck. The object deck is used to produce a tape for hardware simulation or a tape for generating prototype tooling.

The TMS 1000 series programs are checked by software and hardware simulation. The software simulation offers the advantages of printed outputs for instruction traces or periodic outputs. The hardware simulation offers the designer the advantages of real-time simulation and testing asynchronous inputs.

After the algorithms have been checked and approved by the customer, the final object code and machine option statements are supplied to TI. A gate mask is generated and slices produced. After assembly and testing, the prototypes are shipped to the customer for approval. Upon receiving final approval, the part is released for volume production at the required rate as one unique version of the TMS 1000 family.

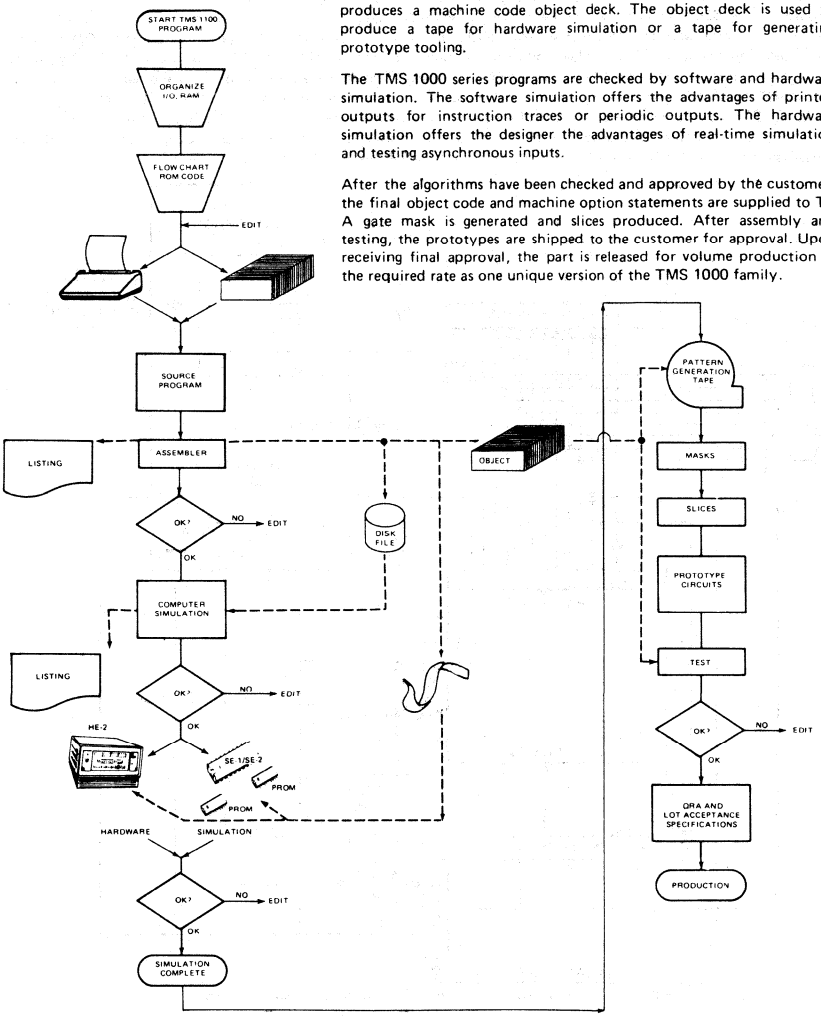
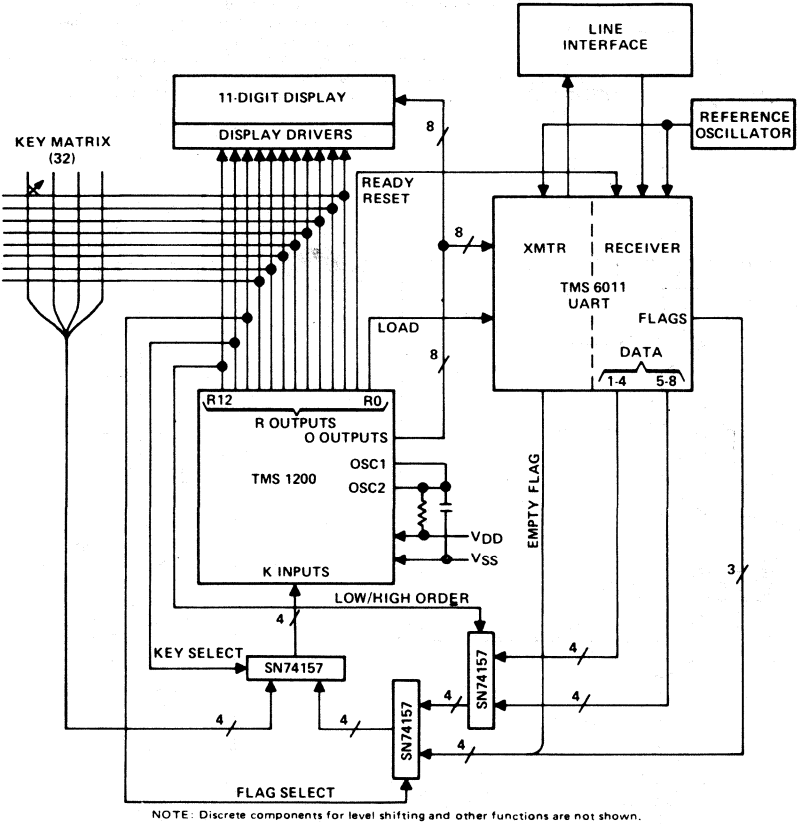


FIGURE 1 – TMS 1000 SERIES ALGORITHM DEVELOPMENT

1.3 APPLICATIONS

One major advantage of the TMS 1000 series is flexibility. The TMS 1000 series is effective in applications such as printer controllers, data terminals, remote sensing systems, cash registers, appliance controls, and automotive applications. A data terminal is a useful example. In Figure 2, a sample interconnect diagram shows how the R outputs control a universal asynchronous receiver/transmitter (UART), display scan, and keyboard scan. The ROM controls data output to the appropriate display digit or to the transmitter section of the UART. A routine in the ROM program controls selection of incoming data through the K-input ports. Two dedicated R outputs (load and ready reset) control the UART's transmit and receive modes. The remaining R outputs both scan the display and select inputs. The SN74157 TTL devices multiplex eight bits of the incoming data word, four bits of UART status, and the four key input lines. Through the TMS 1000 series' versatility, a wide range of systems realize reduced costs, fewer parts, and high reliability.



NOTE: Discrete components for level shifting and other functions are not shown.

FIGURE 2 – BLOCK DIAGRAM OF TYPICAL APPLICATION–TERMINAL CONTROLLER

2. TMS 1000/1200 AND TMS 1070/1270 MICROCOMPUTERS

2.1 INTRODUCTION

The TMS 1000/1200 and TMS 1070/1270 are identical except for maximum voltage ratings for the K inputs and the O and R outputs, and the TMS 1270 has a total of ten O outputs. See Section 5 for a TMS 1070/1270 description.

The microcomputer's ROM program controls data input, storage, processing, and output. Data processing takes place in the arithmetic logic unit. K input data goes into the ALU, as shown in Figure 3, and is stored in the four-bit accumulator. The accumulator output accesses the output latches, the RAM storage cells, and the adder input. Data storage in the 256-bit RAM is organized into 64 words, four bits per word. The four-bit words are conveniently grouped into four 16-word files addressed by a two-bit register. A four-bit register addresses one of the 16 words in a file by ROM control.

The O outputs and the R outputs are the output channels. The eight parallel O outputs are decoded from five data latches. The O outputs serve many applications because the decoder is a programmable logic array (PLA) that is modified by changing the gate-level mask tooling. Each of the thirteen R outputs of the TMS 1200 and the eleven R outputs on the TMS 1000 has an individual storage element that can be set or reset by program control. The R outputs send status or enable signals to external devices. The R outputs strobe the O outputs to displays, to other TMS 1000 series chips, or to TTL and other interface circuits. The same R outputs multiplex data into the K inputs whenever necessary.

There are 43 basic instructions that handle I/O, constant data from the ROM, bit control, internal data transfer, arithmetic processing, branching, looping, and subroutines. The eight-bit instruction word performs 256 unique operations for maximum efficiency. Section 2.9 defines the standard instruction set, which is optimized for most programs. Microprogramming for special applications is possible, and the operations of the instruction set can be modified by the same mask-tooling step that programs the ROM and the O output PLA.

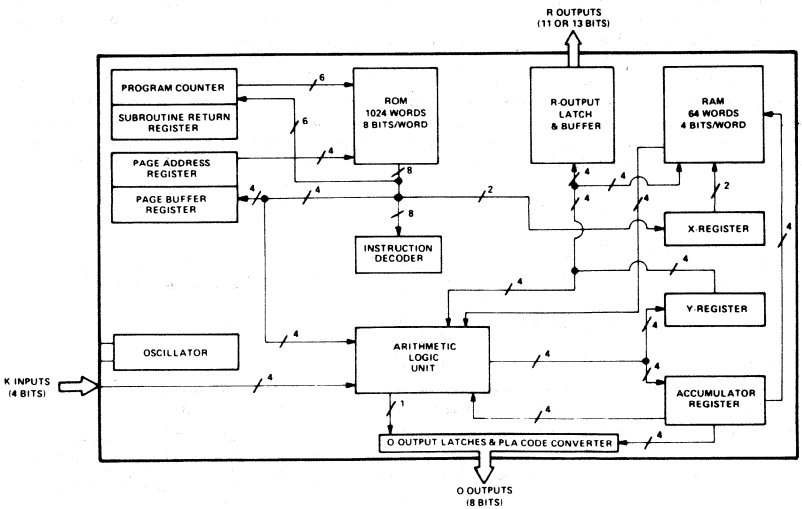


FIGURE 3 – TMS 1000/1200 LOGIC BLOCKS

2.2 ROM OPERATION

The sequence of the 1024 eight-bit ROM instructions determines the device operation. There are 16 pages of instructions with 64 instructions on each page. After power-up the program execution starts at a fixed instruction address. Then a shift-register program counter sequentially addresses each ROM instruction on a page. A conditional branch or call subroutine instruction may alter the six-bit program-counter address to transfer software control. One level of subroutine return address is stored in the subroutine return register. The page address register (four bits) holds the current address for one of the 16 ROM pages. To change pages, a constant from the ROM loads into the page buffer register (four bits), and upon a successful branch or call, the page buffer loads into the page address register. The page buffer register also holds the return page address in the call subroutine mode.

2.3 RAM OPERATION

There are 256 addressable bits of RAM storage available. The RAM is comprised of four files, each file containing 16 four-bit words. The RAM is addressed by the Y register and the X register. The Y register selects one of the 16 words in a file and is completely controllable by the arithmetic unit. The TMS 1000 series has instructions that: Compare Y to a constant, set Y to a constant, increment or decrement Y, and/or perform data transfer to or from Y. Two bits in the X register select one of the four 16-word files. The X register is set to a constant or is complemented. A four-bit data word goes to the RAM location addressed by X and Y from the accumulator or from the constants in the ROM. The RAM output words go to the arithmetic unit and can be operated on and loaded into Y or the accumulator in one instruction interval. Any selected bit in the RAM can be set, reset, or tested.

2.4 ARITHMETIC LOGIC UNIT OPERATION

Arithmetic and logic operations are performed by the four-bit adder and associated logic. The arithmetic unit performs logical comparison, arithmetic comparison, add, and subtract functions. The arithmetic unit and interconnects are shown in Figure 4. The operations are performed on two sets of inputs, P and N. The two four-bit parallel inputs may be added together or logically compared. The accumulator has an inverted output to the N selector for subtraction by two's complement arithmetic. The other N inputs are from the true output of the accumulator, the RAM, constants, and the K inputs. The P inputs come from the Y register, the RAM, the constants, and the K inputs.

Addition and subtraction results are stored in either the Y register or the accumulator. An arithmetic function may cause a carry output to the status logic. Logical comparison may generate an output to status. If the comparison functions are used, only the status bit affects the program control, and neither the Y register's nor the accumulator register's contents are affected. If the status feedback is a logic one, which is the normal state, then the conditional branch or call is executed successfully. If an instruction calls for a carry output to status and the carry does not occur,

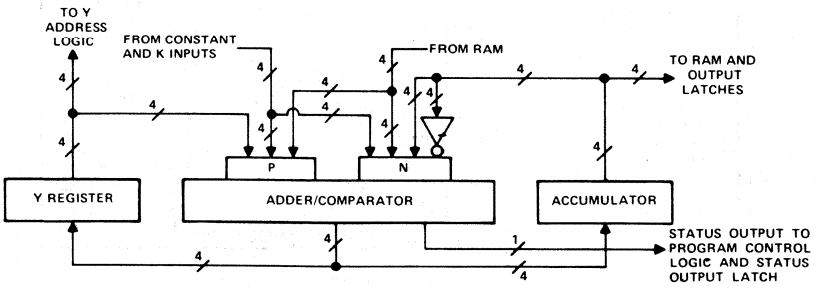


FIGURE 4 – ALU AND ASSOCIATED DATA PATHS

then status will go to a zero state for one instruction cycle. Likewise, if an instruction calls for the logical-comparison function and the bits compared are all equal, then status will go to a zero state for one instruction cycle. If status is a logic zero, then branches and calls are not performed successfully.

2.5 INPUT

There are four data inputs to the TMS 1000-series circuit, K1, K2, K4, and K8. Each time an input word is requested, the data path from the K inputs is enabled to the adder. The inputs are either tested for a high level ($\approx V_{SS}$), or the input data are stored in the accumulator for further use. The R outputs usually multiplex inputs such as keys and other data. Other input interfaces are possible. An external device that sends data out to the K-input bus at a fixed rate may be used with the TMS 1000 series when an initiating "handshake" signal is given from an R output. Data from the K inputs is stored periodically in synchronization with the predetermined data rate of the external device. Thus, multiple four-bit words can be requested and stored with only one R output supplying the control signal.

2.6 OUTPUT

There are two output channels with multiple purposes, the R outputs and the O outputs. Thirteen latches store the R output data. The eight parallel O outputs come from a five-bit-to-eight-bit code converter, which is the O-output PLA. The R outputs are individually addressed by the Y register. Each addressed bit can be set or reset.

The R outputs are normally used to multiplex inputs and strobe O output data to displays, external memories, and other devices. Also, one R output can strobe other R outputs that represent variable data, because every R output may be set or reset individually. For example, the Y register addresses each latch in turn; the variable data R outputs are set or reset; and finally, the data strobe R latch is set.

The eight O outputs usually send out display or binary data that are encoded from the O output latches. The O latches contain five bits. Four bits load from the accumulator in parallel. The fifth bit comes from the status latch, which is selectively loaded from the adder output (see Figure 4). The load output command sends the status latch and accumulator information into the five output latches. The five bits are available in true or complementary form to 20 programmable-input NAND gates in the O output PLA. Each NAND gate can simultaneously select any combination of O0 through O7 as an output. The user defines this PLA's decoding to suit an optimum output configuration. As an illustration, the O output PLA can encode any 16 characters of eight-segment display information and additionally can transfer out a four-bit word of binary data.

2.7 THE INSTRUCTION PROGRAMMABLE LOGIC ARRAY

The programmable instruction decode is defined by the instruction PLA. Thirty programmable-input NAND gates decode the eight bits of instruction word. Each NAND gate output selects a combination of 16 microinstructions. The 16 microinstructions control the arithmetic unit, status logic, status latch, and write inputs to the RAM.

As an example, the "add eight to the accumulator, results to accumulator" instruction can be modified to perform a "add eight to the Y register, result to Y" instruction. Modifications that take away an instruction that is not used very often are desirable if the modified instructions save ROM words by increasing the efficiency of the instruction repertoire. A programmer's reference manual is available to explain PLA programming and the TMS 1000-series operation in detail.

2.8 TIMING RELATIONSHIPS

Six oscillator pulses constitute one instruction cycle. All instructions are executed in one instruction cycle. The actual machine cycle period is determined by either a fixed external resistor and capacitor connected to the OSC1 and OSC2 pins (refer to Section 4), or an external clock input frequency.

2.9 SOFTWARE SUMMARY

Table 2 defines the TMS 1000/1200 and TMS 1070/1270 standard instruction set with a description, mnemonic, and status effect. The mnemonics were defined for easy reference to the functional description. Eighteen mnemonics use an identifier to indicate the condition that satisfies the status requirement for a successful branch or call if the instruction is followed immediately by a branch or call command. "C" means that if the instruction generates a carry (status = one), then a following branch or call is executed. If a branch instruction does not follow or if there is no carry (status = zero), then the program counter proceeds to the next address without changing the normal counting sequence. "N" means that if no borrow (equal to a carry in two's complement arithmetic) is generated, an ensuing branch or call is taken. "Z" indicates that if the two's complement of zero in the accumulator (instruction CPAIZ) is attempted with a branch or call following, then the branch or call is taken. "1", "LE", "NE", and "NEZ" are used to indicate conditions for branch and call for seven test instructions. The test instructions do not modify data at all; tests are used solely in conjunction with subsequent branches or calls.

If an instruction that does not affect status is placed between an instruction that does affect status and a branch or call instruction, then the branch or call is always successful. This is true because status always returns to its normal state (status = one) after one instruction cycle, and branches and calls are taken if status equals one.

TABLE 2
TMS 1000/1200 AND TMS 1070/1270 STANDARD INSTRUCTION SET

FUNCTION	MNEMONIC	STATUS EFFECTS		DESCRIPTION
		C	N	
Register to Register	TAY			Transfer accumulator to Y register.
	TYA			Transfer Y register to accumulator.
	CLA			Clear accumulator.
Transfer Register to Memory	TAM			Transfer accumulator to memory.
	TAMIY			Transfer accumulator to memory and increment Y register.
	TAMZA			Transfer accumulator to memory and zero accumulator.
Memory to Register	TMY			Transfer memory to Y register.
	TMA			Transfer memory to accumulator.
	XMA			Exchange memory and accumulator.
Arithmetic	AMAAC	Y		Add memory to accumulator, results to accumulator. If carry, one to status.
	SAMAN	Y		Subtract accumulator from memory, results to accumulator. If no borrow, one to status.
	IMAC	Y		Increment memory and load into accumulator. If carry, one to status.
	DMAN	Y		Decrement memory and load into accumulator. If no borrow, one to status.
	IA			Increment accumulator, no status effect.
	IYC	Y		Increment Y register. If carry, one to status.
	DAN	Y		Decrement accumulator. If no borrow, one to status.
	DYN	Y		Decrement Y register. If no borrow, one to status.
	A8AAC	Y		Add 8 to accumulator, results to accumulator. If carry, one to status.
	A10AAC	Y		Add 10 to accumulator, results to accumulator. If carry, one to status.
	A6AAC	Y		Add 6 to accumulator, results to accumulator. If carry, one to status.
	CPAIZ	Y		Complement accumulator and increment. If then zero, one to status.
Arithmetic Compare	ALEM	Y		If accumulator less than or equal to memory, one to status.
	ALEC	Y		If accumulator less than or equal to a constant, one to status.
Logical Compare	MNEZ		Y	If memory not equal to zero, one to status.
	YNEA		Y	If Y register not equal to accumulator, one to status and status latch.
	YNEC		Y	If Y register not equal to a constant, one to status.

– CONTINUED –

TABLE 2
TMS 1000/1200 AND TMS 1070/1270 STANDARD INSTRUCTION SET (Continued)

FUNCTION	MNEMONIC	STATUS EFFECTS C	STATUS EFFECTS N	DESCRIPTION
Bits in Memory	SBIT			Set memory bit.
	RBIT			Reset memory bit.
	TBIT1		Y	Test memory bit. If equal to one, one to status.
Constants	TCY			Transfer constant to Y register.
	TCMIY			Transfer constant to memory and increment Y.
Input	KNEZ		Y	If K inputs not equal to zero, one to status.
	TKA			Transfer K inputs to accumulator.
Output	SETR			Set R output addressed by Y.
	RSTR			Reset R output addressed by Y.
	TDO			Transfer data from accumulator and status latch to O outputs.
	CLO			Clear O-output register.
RAM 'X' Addressing	LDX			Load 'X' with a constant.
	COMX			Complement 'X'.
ROM Addressing	BR			Branch on status = one.
	CALL			Call subroutine on status = one.
	RETN			Return from subroutine.
	LDP			Load page buffer with constant.

NOTES: C-Y (Yes) means that if there is a carry out of the MSB, status output goes to the one state. If no carry is generated, status output goes to the zero state.

N-Y (Yes) means that if the bits compared are not equal, status output goes to the one state. If the bits are equal, status output goes to the zero state.

A zero in status remains through the next instruction cycle only. If the next instruction is a branch or call and status is a zero, then the branch or call is not executed successfully.

2.10 SAMPLE PROGRAM

The following example shows register addition of up to fifteen BCD digits. The add routine (flow charted in Figure 5) can use the entire RAM, which is divided into two pairs of registers. The definition of registers, for the purpose of illustration, is expanded to include the concept of a variable-length word that is a subset of a 16-digit file. Addition proceeds from the least-significant digit (LSD) to the most-significant digit (MSD), and carry ripples through the accumulator. The decrement-Y instruction is used to index the numbers in a register. The initial Y value sets the address for the LSD's of two numbers to be added. Thus, if Y equals eight at the start, the LSD is defined to be stored in M(X,8), [M(X, Y) ≡ contents of RAM word location X equals 0, 1, 2, or 3, and Y equals 0 to 15]. If Y is eight initially, M(X,7) is the next-most-significant digit.

RAM DATA MAP BEFORE EXECUTING SAMPLE ROUTINE

FILE ADDRESS	REGISTER	Y-REGISTER ADDRESS 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X = 00	D	OV 0	MSD 9	8	7	6	5	4	3	LSD 2							
X = 01	E	OV 0	MSD 1	2	3	4	5	6	7	8	9	0	1	2	3	4	LSD 5
X = 10	F	OV 0	MSD 5	4	3	2	1	0	9	8	7	6	5	4	3	2	LSD 1
X = 11	G	OV 0	MSD 8	7	6	5	4	3	2	LSD 1							

OV ≡ overflow, MSD ≡ most-significant digit, and LSD ≡ least-significant digit

In the preceeding RAM register assignment map, registers D and G are nine digits long, and registers E and F are 16 digits long. The sample routine calls the D plus G → D subroutine and the E plus F → E subroutine. After executing the two subroutines, the RAM contents are the following:

RAM DATA MAP AFTER EXECUTING SAMPLE ROUTINE

FILE ADDRESS	REGISTER	Y-REGISTER ADDRESS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X = 00	D	OV 1	MSD 8	6	4	1	9	7	5	LSD 3							
X = 01	E	OV 0	MSD 6	6	6	6	6	7	7	7	6	6	6	6	6	6	LSD 6
X = 10	F	OV 0	MSD 5	4	3	2	1	0	9	8	7	6	5	4	3	2	LSD 1
X = 11	G	OV 0	MSD 8	7	6	5	4	3	2	LSD 1							

NOTE: Shaded areas indicate locations in the RAM that are unaffected by executing the example routine.

```
                  LABEL    OPCODE   OPERAND   COMMENT
MAIN PROGRAM
PRESETS Y,                 TCY      8         Transfer 8 → Y
AND CALL                   CALL     ADGD      Add: D + G → D
SUBROUTINES                TCY      15        Transfer 15 → Y
                           CALL     AEFE      Add: E + F → E

                  ADGG     LDX      3         3 → X; Set up for D + G → G.
                           BR       BCDADD    Branch to BCD add.
MULTIPLE ENTRY    AEFF     LDX      2         2 → X; Set up for E + F → F.
POINTS FOR                 BR       BCDADD    Branch to BCD add.
SUBROUTINES       AEFE     LDX      1         1 → X; Set up for E + F → E.
                           BR       BCDADD    Branch to BCD add.
                  ADGD     LDX      0         0 → X; Add D + G → D.
                  BCDADD   CLA                Clear accumulator (A).
                  LOOP     COMX               X̄ → X.
                           AMAAC              M(X,Y) + A → A; A contains
                                              possible carry if in loop.
                           COMX               X̄ → X.
                           AMAAC              Add digits:
                                              M(X; Y) + [M(X̄,Y) + Carry] → A.
BASE                       BR       GT9       Branch if sum >15.
SUBROUTINE                 ALEC     9         If A ≤ 9, one to status.
CONTAINS                   BR       LT10      Branch if sum < 10.
LOOPING           GT9      A6AAC              Sum > 9, A + 6 → A;
AND                                           BCD Correction.
BCD                        TAMZA              Transfer corrected sum
CORRECTION                                    to memory, 0 → A.
                           IA                 1 → A; to propagate carry
                  DECY     DYN                Y − 1 → Y; index next digit.
                           BR       LOOP      If no borrow, continue.
                           RETN               If borrow, return to
                                              instruction after call.
                  LT10     TAMZA              Sum < 9, A → M(X,Y); 0 → A;
                                              No carry propagated.
                           BR       DECY
```

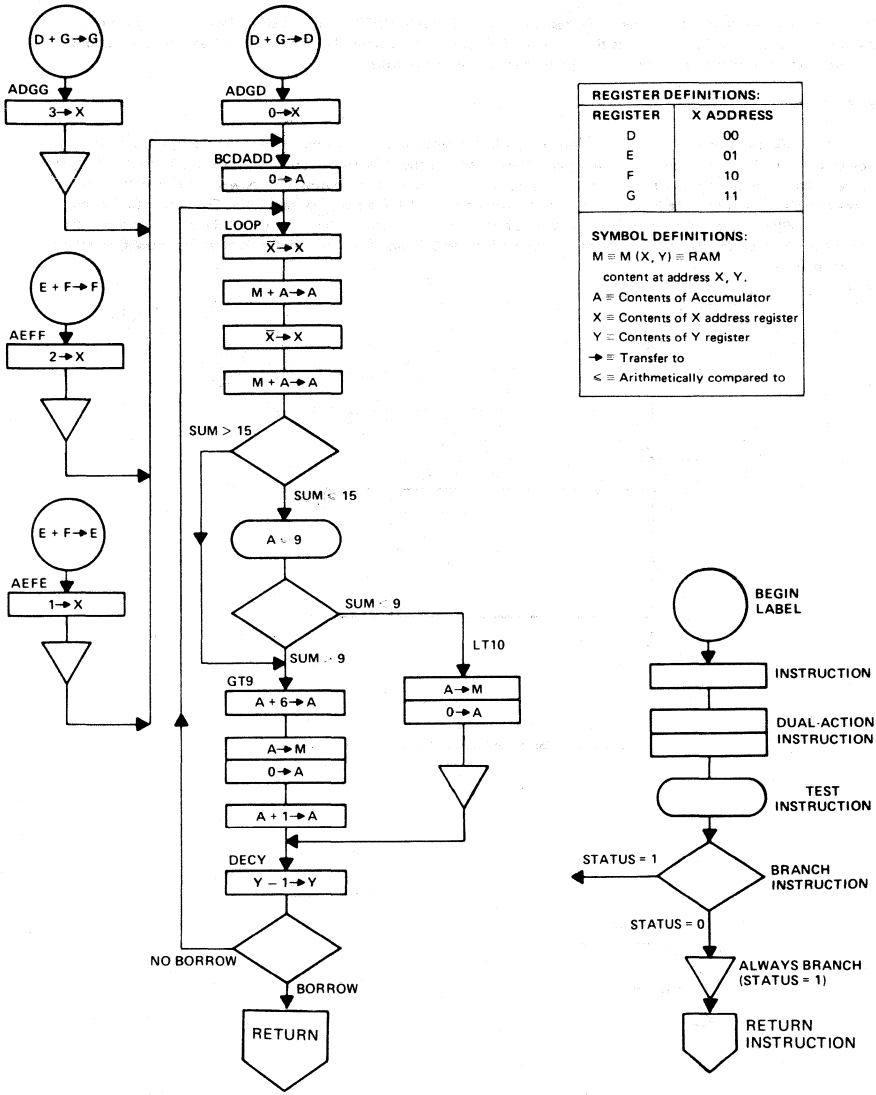
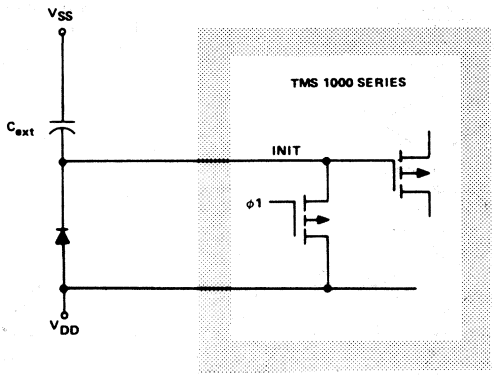


FIGURE 5 – MACHINE INSTRUCTION FLOWCHART–BCD-ADDITION SUBROUTINE

Note that there are four entry points to the base subroutine (ADGG, ADGD, AEFF, AEFE). The main program can call two of the other possible subroutines that store the addition results differently. These subroutines have applications in floating-point arithmetic, multiplication, division, and subtraction routines.

2.11 POWER-ON

The TMS 1000 series has a built-in power-on latch, which resets the program counter upon the proper application of power (with INIT input open or tied to V_{DD}). After power-up the chip resets and begins execution at a fixed ROM address. The system reset depends on the ROM program after the starting address. For power supplies with slow rise times or noisy conditions, the following network connected to the INIT pin may be necessary. To assist initialization of the TMS 1000 series devices, a capacitor maintains a high-level voltage on the INIT input after the power supply settles. The diode connecting V_{DD} to INIT is used to fully discharge C_{ext} and allow a proper reset when fast power-on-off-on cycles are expected.



$C_{ext}(\mu F)$ = 0.06 Power Supply Rise Time (ms)

3. TMS 1100 AND TMS 1300 MICROCOMPUTERS

3.1 INTRODUCTION

Texas Instruments increased the four-bit microprocessor capability with an expanded one-chip microcomputer containing all of the TMS 1000 features plus twice the ROM and RAM capacity. (See Figure 6.) Two versions of the expanded memory device are available:

TMS 1100

- Pin-for-pin interchangeable with the TMS 1000
- 16,384-bit ROM, 2048 eight-bit instruction words
- 512-bit RAM, 128 four-bit data words
- 11 individually latched R outputs, 28-pin package

TMS 1300

- 16,384-bit ROM
- 512-bit RAM
- 16 individually latched R outputs, 40-pin package

Many industrial, consumer, and business applications can be implemented with a microcomputer having the capabilities of two TMS 1000 devices. With considerably lower system cost, the TMS 1100/1300 single-device microcomputers enable a number of applications that previously required two TMS 1000's or external read/write memory. In the 40-pin version, the TMS 1300, the maximum number of R outputs is increased to 16. Displays 16 characters long as well as a 64-position keyboard or switch matrix (16 X 4) are scanned directly by the TMS 1300.

The TMS 1100/1300 operation is identical to that of the TMS 1000/1200 except where noted otherwise in the following paragraphs.

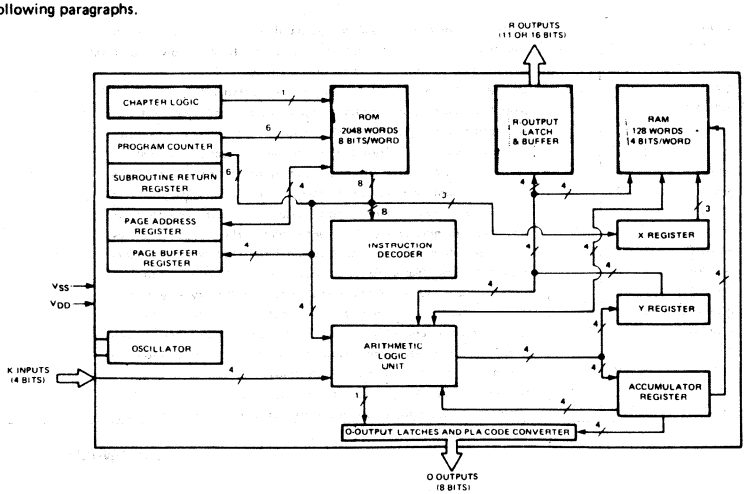


FIGURE 6 – TMS 1100/1300 LOGIC BLOCKS

3.2 ROM OPERATION

The TMS 1100/1300 instruction ROM contains two chapters of 16 pages each. A page contains 64 eight-bit words. The chapter logic consists of three control bits, chapter address, chapter buffer, and chapter subroutine. The chapter buffer bit is controlled by a complement chapter buffer instruction (see COMC in Table 3). The chapter buffer bit transfers into the current chapter address if a branch or call executes successfully. If a call is successful, the return chapter is saved in a chapter subroutine latch. Since the buffer bit is changeable without affecting the chapter subroutine-return address, up to 128 words that are contained on two pages of alternate chapters are available in a single subroutine. The program counter and page addressing operation is identical to the TMS 1000/1200 explained in 2-2.

TABLE 3
TMS 1100/1300 STANDARD INSTRUCTION SET

FUNCTION	MNEMONIC	STATUS EFFECT		DESCRIPTION
		C	N	
Register-to-Register Transfer	TAY			Transfer accumulator to Y register
	TYA			Transfer Y register to accumulator
	CLA			Clear accumulator
Register to Memory	TAM			Transfer accumulator to memory
	TAMIYC	Y		Transfer accumulator to memory and increment Y register. If carry, one to status.
	TAMDYN	Y		Transfer accumulator to memory and decrement Y register. If no borrow, one to status.
	TAMZA			Transfer accumulator to memory and zero accumulator
Memory to Register	TMY			Transfer memory to Y register
	TMA			Transfer memory to accumulator
	XMA			Exchange memory and accumulator
Arithmetic	AMAAC	Y		Add memory to accumulator, results to accumulator. If carry, one to status.
	SAMAN	Y		Subtract accumulator from memory, results to accumulator. If no borrow, one to status.
	IMAC	Y		Increment memory and load into accumulator. If carry, one to status.
	DMAN	Y		Decrement memory and load into accumulator. If no borrow, one to status.
	IAC	Y		Increment accumulator. If carry, one to status.
	DAN	Y		Decrement accumulator. If no borrow, one to status.
	A2AAC	Y		Add 2 to accumulator. Results to accumulator. If carry, one to status.
	A3AAC	Y		Add 3 to accumulator. Results to accumulator. If carry, one to status.
	A4AAC	Y		Add 4 to accumulator. Results to accumulator. If carry, one to status.
	A5AAC	Y		Add 5 to accumulator. Results to accumulator. If carry, one to status.
	A6AAC	Y		Add 6 to accumulator. Results to accumulator. If carry, one to status.
	A7AAC	Y		Add 7 to accumulator. Results to accumulator. If carry, one to status.
	A8AAC	Y		Add 8 to accumulator. Results to accumulator. If carry, one to status.
	A9AAC	Y		Add 9 to accumulator. Results to accumulator. If carry, one to status.
	A10AAC	Y		Add 10 to accumulator. Results to accumulator. If carry, one to status.
	A11AAC	Y		Add 11 to accumulator. Results to accumulator. If carry, one to status.
	A12AAC	Y		Add 12 to accumulator. Results to accumulator. If carry, one to status.
	A13AAC	Y		Add 13 to accumulator. Results to accumulator. If carry, one to status.
	A14AAC	Y		Add 14 to accumulator. Results to accumulator. If carry, one to status.
	IYC	Y		Increment Y register. If carry, one to status.
	DYN	Y		Decrement Y register. If no borrow, one to status.
	CPAIZ	Y		Complement accumulator and increment. If then zero, one to status.

– CONTINUED –

TABLE 3
TMS 1100/1300 STANDARD INSTRUCTION SET (Continued)

FUNCTION	MNEMONIC	STATUS EFFECT		DESCRIPTION
		C	N	
Arithmetic Compare	ALEM	Y		If accumulator less than or equal to memory, one to status.
Logical Compare	MNEA		Y	If memory is not equal to accumulator, one to status.
	MNEZ		Y	If memory not equal to zero, one to status.
	YNEA		Y	If Y register not equal to accumulator, one to status and status latch.
	YNEC		Y	If Y register not equal to a constant, one to status.
Bits in Memory	SBIT			Set memory bit
	RBIT			Reset memory bit
	TBIT1		Y	Test memory bit. If equal to one, one to status.
Constants	TCY			Transfer constant to Y register
	TCMIY			Transfer constant to memory and increment Y
Input	KNEZ		Y	If K inputs not equal to zero, one to status.
	TKA			Transfer K inputs to accumulator
Output	SETR			Set R output addressed by Y
	RSTR			Reset R output addressed by Y
	TDO			Transfer data from accumulator and status latch to O-outputs
RAM X Addressing	LDX			Load X with file address
	COMX			Complement the MSB of X
ROM Addressing	BR			Branch on status = one
	CALL			Call subroutine on status = one
	RETN			Return from subroutine
	LDP			Load page buffer with constant
	COMC			Complement chapter

NOTES: C-Y (Yes) means that if there is a carry out of the MSB, status output goes to the one state. If no carry is generated, status output goes to the zero state.

N-Y (Yes) means that if the bits compared are not equal, status output goes to the one state. If the bits are equal status output goes to the zero state.

A zero in status remains through the next instruction cycle only. If the next instruction is a branch or call and status is a zero, then the branch or call is not executed successfully.

6

3.3 RAM OPERATION

The TMS 1100/1300 devices contain a 512-bit RAM for data storage. The matrix consists of eight files, each file containing 16 four-bit words. Similar to the TMS 1000/1200, the X and Y registers address the RAM. The Y register selects one of the 16 words in a file and the X register (three bits long) selects one of eight possible files. When using the set or reset R instructions, the X register must be less than four.

3.4 OUTPUT

The TMS 1100 is pin-for-pin interchangeable with the TMS 1000 and contains eleven R outputs and eight O outputs.

The R-output capability in the TMS 1300 is increased to 16 output latches. These extra latches perform control functions directly that would have required external decoding logic in the TMS 1100 device. These additional R outputs can be set to any combination. For example, Figure 2 shows an O-output data bus going into the transmitter section of the UART. If the O-output PLA is programmed to send out four bits of binary data (when directed to do so by the status latch), then three additional R outputs connected to the UART transmitter input provides the user with full seven-bit ASCII output capability.

4. TMS 1000/1200 AND TMS 1100/1300 ELECTRICAL AND MECHANICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

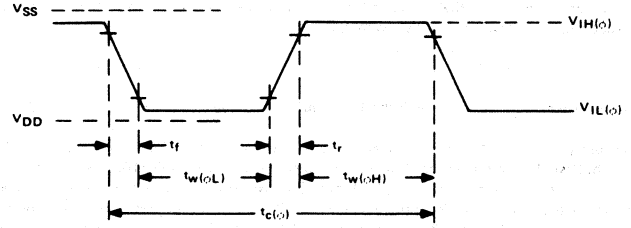
Voltage applied to any device terminal (see Note 1) . . . . . −20 V
Supply voltage, V_{DD} . . . . . −20 V to 0.3 V
Data input voltage . . . . . −20 V to 0.3 V
Clock input voltage . . . . . −20 V to 0.3 V
Average output current (see Note 2): O outputs . . . . . −24 mA
R outputs . . . . . −14 mA
Peak output current: O outputs . . . . . −48 mA
R outputs . . . . . −28 mA
Continuous power dissipation: TMS 1000/1100 NL . . . . . 400 mW
TMS 1200/1300 NL . . . . . 600 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 3)		−14	−15	−17.5	V
High-level input voltage, V_{IH} (see Note 4)	K	−1.3	−1	0.3	V
	INIT or Clock	−1.3	−1	0.3	
Low-level input voltage, V_{IL} (see Note 4)	K	V_{DD}		−4	V
	INIT or Clock	V_{DD}	−15	−8	
Clock cycle time, $t_{c(\phi)}$		2.5	3	10	μs
Instruction cycle time, t_c		15		60	μs
Pulse width, clock high, $t_{w(\phi H)}$		1			μs
Pulse width, clock low, $t_{w(\phi L)}$		1			μs
Sum of rise time and pulse width, clock high, $t_r + t_{w(\phi H)}$		1.25			μs
Sum of fall time and pulse width, clock low, $t_f + t_{w(\phi L)}$		1.25			μs
Oscillator frequency, f_{osc}		100		400	kHz
Operating free-air temperature, T_A		0		70	°C

NOTES: 1. Unless otherwise noted, all voltages are with respect to V_{SS}.
2. These average values apply for any 100-ms period.
3. Ripple must not exceed 0.2 volts peak-to-peak in the operating frequency range.
4. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this specification for logic voltage levels only.



NOTE: Timing points are 90% (high) and 10% (low).

FIGURE 7 – EXTERNALLY DRIVEN CLOCK INPUT WAVEFORM

4.3 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

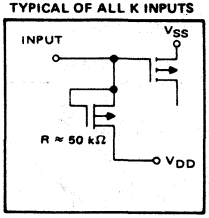
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_I	Input current, K inputs		V_I = 0 V		50	300	500	μA
V_{OH}	High-level output voltage (see Note 1)	O outputs	I_O = −10 mA		−1.1‡	−0.6‡		V
		R outputs	I_O = −2 mA		−0.75	−0.4		
I_{OL}	Low-level output current		V_{OL} = V_{DD}				−100	μA
$I_{DD(av)}$	Average supply current from V_{DD} TMS 1000/1200 (see Note 2)		All outputs open			−6	−10	mA
$I_{DD(av)}$	Average supply current from V_{DD} TMS1100/1300 (see Note 2)		All outputs open			−7	−11	mA
$P_{(AV)}$	Average power dissipation TMS 1000/1200 (see Note 2		All outputs open			90	175	mW
$P_{(AV)}$	Average power dissipation TMS1100/1300 (see Note 2)		All outputs open			105	193	mW
f_{osc}	Internal oscillator frequency		R_{ext} = 50 kΩ,	C_{ext} = 47 pF	250	300	350	kHz
C_i	Small-signal input capacitance, K inputs		V_I = 0,	f = 1 kHz		10		pF
$C_{i(\phi)}$	Input capacitance, clock input		V_I = 0,	f = 100 kHz		25		pF

†All typical values are at V_{DD} = −15 V, T_A = 25°C.
‡Parts with V_{OH} of −2 V minimum, −1.3 V typical, are available if requested.

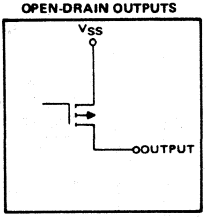
NOTES: 1. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this specification for logic voltage levels only.
2. Values are given for the open-drain O and R output configurations. Pull-down resistors are optionally available on all outputs and increase I_{DD} (see Section 4.4).

4.4 SCHEMATICS OF INPUTS AND OUTPUTS

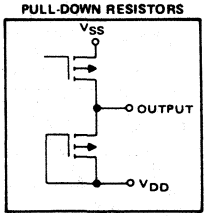
TYPICAL OF ALL K INPUTS



TYPICAL OF ALL O AND R OPEN-DRAIN OUTPUTS



TYPICAL OF ALL O AND R OUTPUTS WITH OPTIONAL PULL-DOWN RESISTORS



The O outputs have nominally 60 Ω on-state impedance; however, upon request a 130-Ω buffer can be mask programmed (see note [‡] section 4.3).

The value of the pull-down resistors is mask alterable and provides the following nominal short-circuit output currents (outputs shorted to V_{SS}):

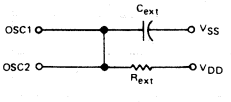
O outputs: 100, 200, 300, 500, or 900 μA

R outputs: 100, 150, or 200 μA

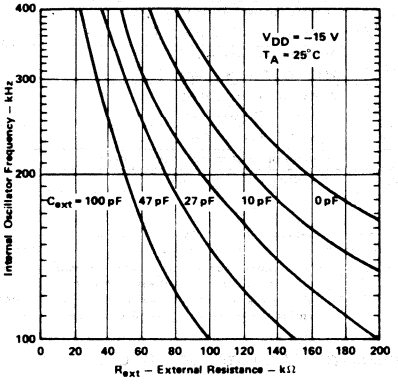
4.5 INTERNAL OR EXTERNAL CLOCK

If the internal oscillator is used, the OSC1 and OSC2 terminals are shorted together and tied to an external resistor to V_{DD} and a capacitor to V_{SS}. If an external clock is desired, the clock source may be connected to OSC1 and OSC2 shorted to V_{SS}.

CONNECTION FOR INTERNAL OSCILLATOR

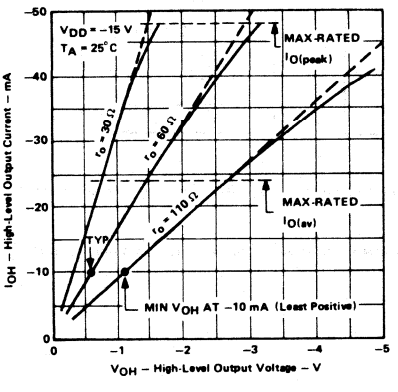


TYPICAL INTERNAL OSCILLATOR FREQUENCY
vs
EXTERNAL RESISTANCE

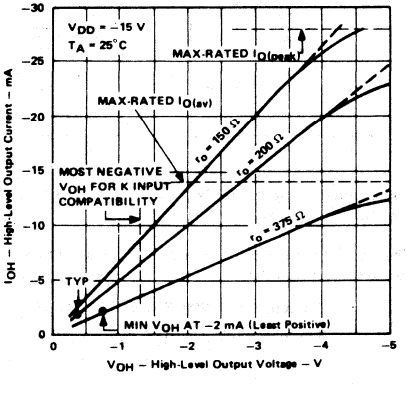


4.6 TYPICAL BUFFER CHARACTERISTICS

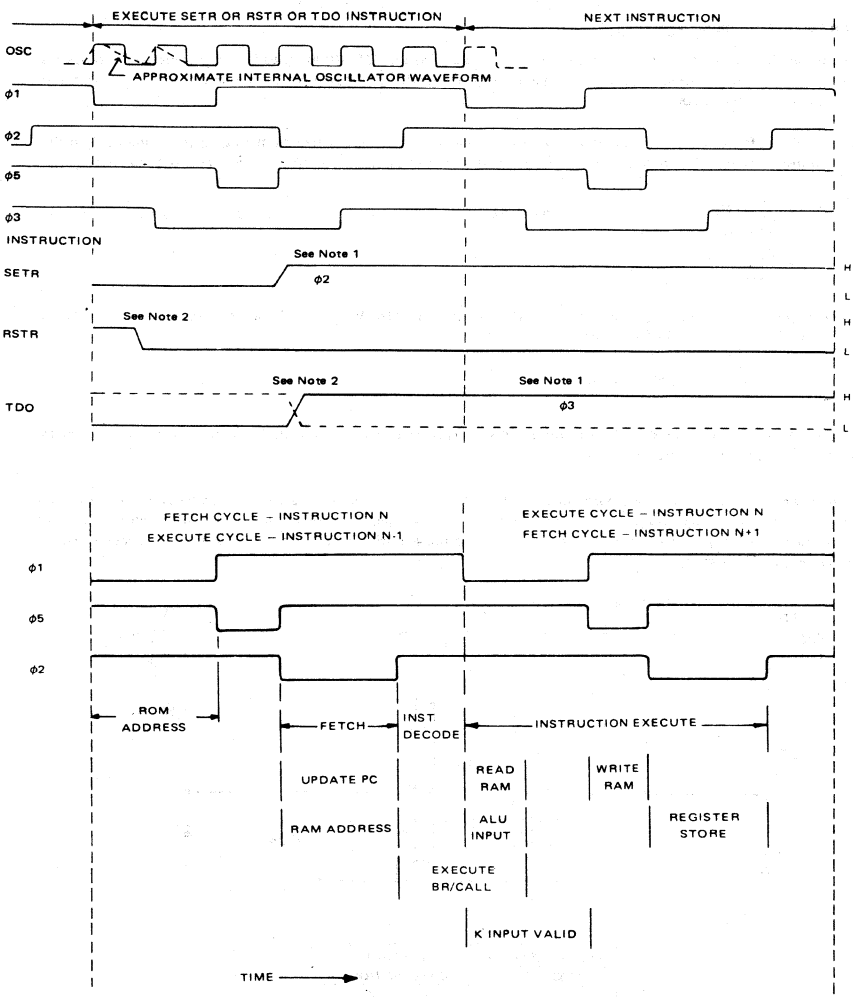
O OUTPUTS
HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE



R OUTPUTS
HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE



4.7 OUTPUT, INPUT, AND INSTRUCTION TIMING



NOTES: 1. Initial rise time is load dependent. The high-level output voltage, V_{OH}, is characterized following the indicated clock period. (See Section 4.6).
2. Rise and fall times are load dependent.

4.8 INTERFACE BETWEEN LOW-POWER SCHOTTKY AND TMS 1000

4.8.1 Push-Pull to MOS Input, $V_{SS} = V_{CC}$

Low-power Schottky series logic interfaces, as shown below, to the TMS 1000 series low-voltage devices and has the advantage of reduced power supply requirements. The level-shifting components are minimal if the V_{CC} supply is common to the V_{SS} supply.

To obtain a sufficient high-level input voltage, V_{IH}, a pull-up resistor R1 is tied from V_{SS} to the K input. With the upper transistor in the TTL push-pull output on and reverse biased by R1, the typical resistor value is calculated:

$$R1 = \frac{V_{IH}}{V_{DD}} \cdot (R2 + R1) \qquad R2 \gg R1$$

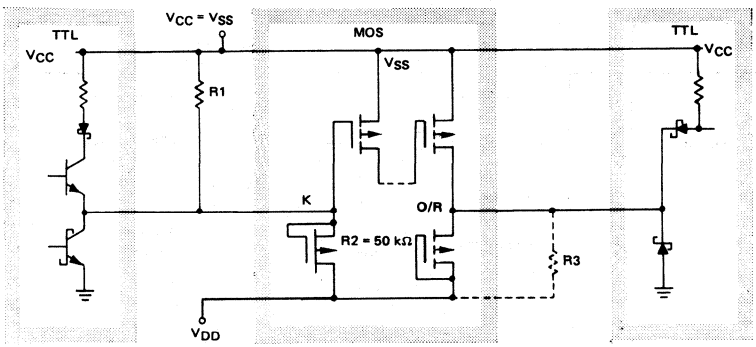
$$R1 \approx \frac{V_{IH}}{V_{DD}} \cdot R2$$

For example if a −0.5-volt noise margin is desired, the recommended V_{IH} is −1.3 volts plus 0.5 volts, which equals −0.8 volts. Since V_{DD} is −17.5 volts maximum, R1 is:

$$R1 = \frac{-0.8\ V}{-17.5\ V} \cdot 50\ k\Omega = 2.28\ k\Omega$$

To use ±10% resistors, R1 should be at most 2.0 kΩ. This procedure for calculating a pull-up resistor applies to standard TTL and open-collector interface as well.

If the lower transistor in the TTL push-pull output is on, the output current is 2 to 3 milliamperes and the low-level output voltage is typically 0.2 volts. Thus the low-level input voltage, V_{IL}, for the K inputs is obtained with 0.3-volt noise margin (at V_{CC} minimum of 4.5 volts). For high-noise environments, an open-collector interface device is shown in paragraph 4.11.



POWER SUPPLIES	VOLTAGE COMBINATIONS	
MOS	TTL	
$V_{SS} = V_{CC}$	5 V	0 V
GND	0 V	−5 V
V_{DD}	−10 V	−15 V

NOTE: TI cannot assume responsibility for any circuits shown or represent that they are free from patent infringement.

4.8.2 MOS to Low-Power Schottky, $V_{SS} = V_{CC}$

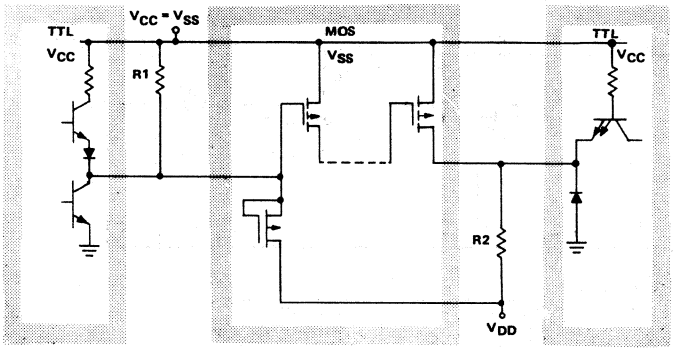
Due to the low current (−400 μA) required to bring a Schottky TTL input low, a single 22-kilohm pull-down resistor (R3) or the 900-microampere pull-down option (O outputs only) provides the necessary low-level input current. The high-level input voltage with the V_{CC} supply at 4.5 volts has 1-volt noise margin.

If a fan-out to more than one TTL circuit is used, the pull-down resistor value is divided by the fan-out number. In the increased fan-out situation, an O output requires an external resistor to assist the 900-microampere pull-down option.

4.9 INTERFACE BETWEEN STANDARD TTL AND TMS 1000

4.9.1 Push-Pull to MOS Input, $V_{SS} = V_{CC}$

Standard TTL logic interfaces as shown with the TMS 1000-series low-voltage devices. The input pull-up resistor R1 is calculated by the same procedure as found in paragraph 4.8.1. The lower push-pull device is stronger in standard TTL compared to Schottky versions. Thus a lower low-level input voltage, V_{IL}, is expected to provide a 0.1-volt increase in noise margin.



POWER SUPPLIES		VOLTAGE COMBINATIONS	
MOS	TTL		
$V_{SS} = V_{CC}$		5 V	0 V
	GND	0 V	−5 V
V_{DD}		−10 V	−15 V

4.9.2 MOS to Standard TTL, $V_{SS} = V_{CC}$

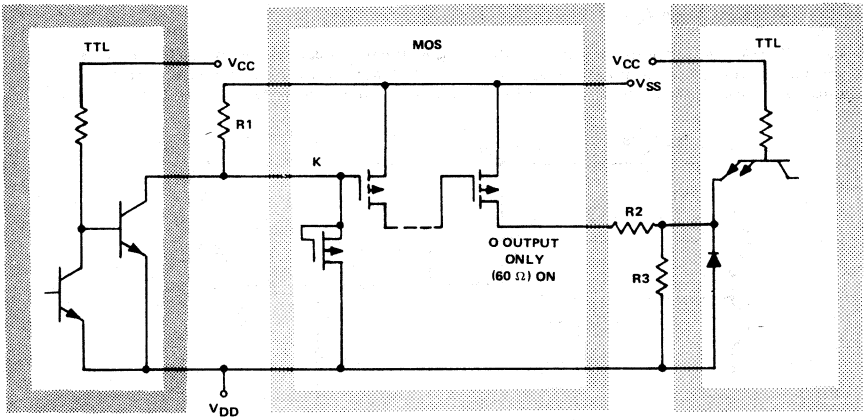
Since standard TTL requires −1.6 milliampere of low-level input current, a pull-down resistor R2 is used for both O and R outputs. With either of the outputs connected to a standard TTL input, a 6.2-kilohm resistor tied to V_{DD} provides slightly more low-level input current. To calculate the pull-down resistor's value, it is assumed that there is negligible current through the open-drain MOS output and that the short-circuit pull-down options are not programmed:

$$R2 \approx \frac{-10\ V}{-1.6\ mA \cdot \text{Fan-Out Number}}$$

4.10 INTERFACE BETWEEN OPEN-COLLECTOR TTL AND MOS

4.10.1 SN7406, SN7407 Open-Collector to MOS Input, V_{DD} = TTL Ground

The SN7406 and SN7407 provide superior noise margins for converting TTL logic levels to MOS inputs. A single pull-up resistor R1 is calculated by the same procedure as found in 4.8.1. The major difference in noise margin occurs with the output low and results from the open-collector being about 1 volt above TTL ground. Thus, the low-level noise margin is approximately 9 volts. More high-level noise margin is obtained by lowering the value of R1 at the cost of increased power dissipation.



POWER SUPPLIES		VOLTAGE COMBINATIONS	
MOS	TTL		
V_{SS}		15 V	10 V
	V_{CC}	5 V	0 V
V_{DD} = GND		0 V	−5 V

4.10.2 Interface Between MOS and Standard TTL, V_{DD} = TTL Ground

When the TTL ground and V_{DD} supplies are common, two resistors, R2 and R3, are required for level-shifting. This interface circuit applies to Schottky TTL also when V_{DD} = GND; only the values of R2 and R3 are changed.

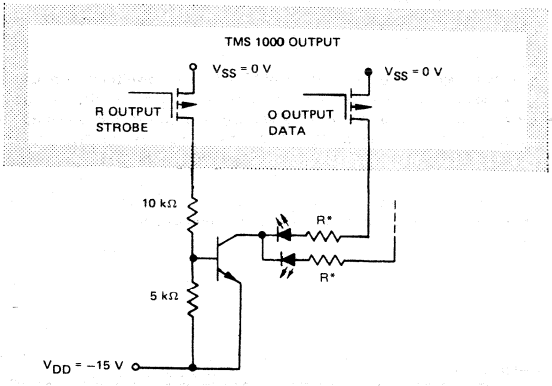
To supply −1.6 milliamperes of low-level input current at 0.4 V above ground requires a clamping resistor R3.

$$R3 = \frac{0.4\ V}{1.6\ mA} = 250\ \Omega$$

The series limiting resistor R2 is calculated to provide a high-level input voltage between 2.7 volts and 5 volts above TTL ground. For the O outputs ($r_{o(on)}$ = 60 Ω typically), R2 is between 1 kilohm and 500 ohms. The maximum current rating for the O output is not to be exceeded, and the fan-out is one TTL input maximum.

Note that when the low-level input current is reduced to 400 microamperes for low-power Schottky TTL, the same resistor network provides a fan-out of four using the O outputs. For an R output to Schottky input with V_{DD} = TTL ground, a fan-out of two is obtainable when R2 ≈ 1 kilohm and R3 ≈ 500 ohms.

4.11 TYPICAL SCANNED LED INTERFACE



*R value depends on duty cycle and brightness.

†The maximum number of LED's depends on the current required by each and the driver used.

SN75492 is recommended for the R-output interface for up to six display characters. The SN75491 quad driver is recommended for O-output interface to LED's requiring high current.

4.12 TERMINAL ASSIGNMENTS

TMS 1000/TMS 1100

R8	1	28	R7
R9	2	27	R6
R10	3	26	R5
V_{DD}	4	25	R4
K1	5	24	R3
K2	6	23	R2
K4	7	22	R1
K8	8	21	R0
INIT	9	20	V_{SS}
O7	10	19	OSC2
O6	11	18	OSC1
O5	12	17	O0
O4	13	16	O1
O3	14	15	O2

TMS 1200

R8	1	40	R7
R9	2	39	R6
R10	3	38	R5
R11	4	37	R4
R12	5	36	R3
V_{DD}	6	35	NC
K1	7	34	NC
K2	8	33	NC
K4	9	32	NC
K8	10	31	R2
INIT	11	30	R1
O7	12	29	R0
NC	13	28	V_{SS}
NC	14	27	OSC2
NC	15	26	OSC1
O6	16	25	O0
O5	17	24	O1
O4	18	23	O2
O3	19	22	NC
NC	20	21	NC

TMS 1300

R11	1	40	R10
R12	2	39	R9
R13	3	38	R8
R14	4	37	R7
R15	5	36	R6
V_{DD}	6	35	NC
K1	7	34	R5
K2	8	33	R4
K4	9	32	R3
K8	10	31	R2
INIT	11	30	R1
O7	12	29	R0
NC	13	28	V_{SS}
NC	14	27	OSC2
NC	15	26	OSC1
O6	16	25	O0
O5	17	24	O1
O4	18	23	O2
O3	19	22	NC
NC	20	21	NC

NC – NO INTERNAL CONNECTION

5. TMS 1070 AND TMS 1270 MICROCOMPUTERS

5.1 INTRODUCTION

The TMS 1000 series flexibility is augmented by two versions of high-voltage (35-volt) microcomputers, the TMS 1070 and the TMS 1270. The standard instruction set and operation is identical to that of the TMS 1000/1200. Architecturally, the devices are identical to the TMS 1000/1200 except that two additional O-output OR-matrix terms were added to provide a total of ten O outputs in the TMS 1270, a 40-pin package unit. The TMS 1070/1270 provides direct interface to low-voltage flourescent displays. The TMS 1070/1270 interfaces with all circuits requiring up to 35-volt levels.

The accompanying diagram, Figure 8, shows an interface to a 30-volt fluorescent display.

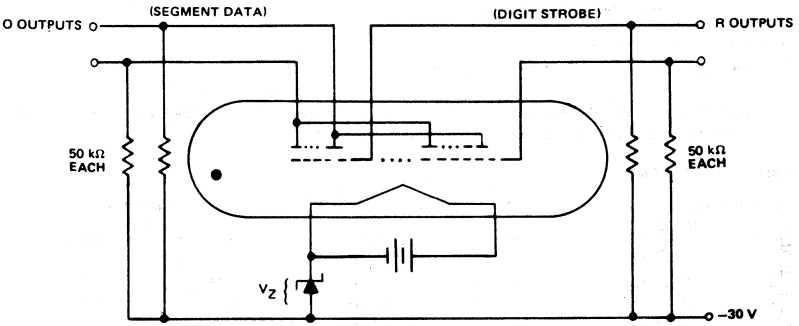


FIGURE 8 – STROBED FLUORESCENT DISPLAY INTERCONNECT

5.2 DESIGN SUPPORT

The TMS 1070/1270 simulation is provided by several time-sharing services. The assembler and simulator programs are accessed by specifying the appropriate device option in the assembler TITLE command.

Functional hardware simulation is accomplished by an SE-1 or an HE-2. To emulate more than eight O outputs in the TMS 1270 with an HE-2 requires an external decoder. Level-shifting buffers allow functional evaluation in the high-voltage prototyping systems.

5.3 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Voltage applied to any device terminal (see Note 1)	−20 V
Supply voltage, V_{DD}	−20 V to 0.3 V
Data input and output voltage with V_{DD} applied (see Note 2)	−35 V to 0.3 V
Clock input and INIT input voltage	−20 V to 0.3 V
Average output current (see Note 3): O outputs	−2.5 mA
R outputs	−12 mA
Peak output current: O outputs	−5 mA
R outputs	−24 mA
Continuous power dissipation: TMS 1070 NL	400 mW
TMS 1270 NL	600 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.4 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 4)		−14	−15	−17.5	V
High-level input voltage, V_{IH} (see Note 5)	K	−6		0.3	V
	INIT or Clock	−1.3	−1	0.3	
Low-level input voltage, V_{IL} (see Note 5)	K (See Note 2)	−35		−8	V
	INIT or Clock	V_{DD}	−15	−8	
Clock cycle time, $t_{c(\phi)}$		2.5	3	10	µs
Instruction cycle time, t_c		15		60	µs
Pulse width, clock high, $t_{w(\phi H)}$		1			µs
Pulse width, clock low, $t_{w(\phi L)}$		1			µs
Sum of rise time and pulse width, clock high, $t_r + t_{w(\phi H)}$		1.25			µs
Sum of fall time and pulse width, clock low, $t_f + t_{w(\phi L)}$		1.25			µs
Oscillator frequency, f_{osc}		100		400	kHz
Operating free-air temperature, T_A		0		70	°C

NOTES: 1. Unless otherwise noted, all voltages are with respect to V_{SS}.
2. V_{DD} must be within the recommended operating conditions specified in 5.4.
3. These average values apply for any 100-ms period.
4. Ripple must not exceed 0.2 volts peak-to-peak in the operating frequency range.
5. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this specification for logic voltage levels only.

5.5 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

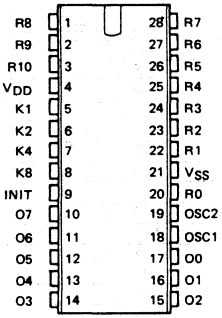
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current, K inputs		V_I = 0 V	40	100	300	μA
V_{OH}	High-level output voltage (see Note 1)	O outputs	I_O = −1 mA	−1	−0.5		V
		R outputs	I_O = −10 mA	−4.5	−2.25		
I_{OL}	Low-level output current		V_{OL} = V_{DD}			−100	μA
$I_{DD(av)}$	Average supply current from V_{DD}		All outputs open		−6	−10	mA
$P_{(AV)}$	Average power dissipation		All outputs open		90	175	mW
f_{osc}	Internal oscillator frequency		R_{ext} = 50 kΩ, C_{ext} = 47 pF	250	300	350	kHz
C_i	Small-signal input capacitance, K inputs		V_I = 0 V, f = 1 kHz		10		pF
$C_{i(\phi)}$	Input capacitance, clock input		V_I = 0 V, f = 100 kHz		25		pF

†All typical values are at V_{DD} = −15 V, T_A = 25°C.

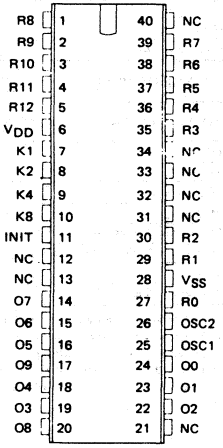
NOTE 1: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this specification for logic voltage levels only.

5.6 TERMINAL ASSIGNMENTS

TMS 1070



TMS 1270



NC – NO INTERNAL CONNECTION

6. MICROCOMPUTER SYSTEM EVALUATORS, SE-1 AND SE-2

6.1 INTRODUCTION

The SE-1 and SE-2 are functionally identical to the TMS 1000/1200 and TMS 1100/1300, respectively, when combined with external instruction memory. The system evaluators are ideally suited for prototype fabrication and field testing. The TMS 1000/1200 and TMS 1100/1300 standard instruction sets are used in the SE-1 and SE-2, respectively. Each unit sends out an instruction address to a PROM (or to other memory device), which feeds an eight-bit instruction word back into the system evaluator for execution. Table 4 summarizes the functions of both system evaluators. Costly errors in mask programming the TMS 1000 series can be eliminated by testing algorithms thoroughly before submitting the final code to Texas Instruments for manufacturing.

TABLE 4
SYSTEM EVALUATORS SE-1 AND SE-2

	SE-1	SE-2
TMS number	TMS 1099 JL	TMS 1098 JL
Simulates microcomputers (instruction set)	TMS 1000/1200 TMS 1070/1270	TMS 1100/1300
Maximum ROM addresses	1024 words X 8 bits/word	2048 words X 8 bits/word
O outputs	5	5
Maximum R outputs	13	16
Single power supply (15 V)	Yes	Yes
Internal or external oscillator	Yes	Yes

6.2 OPERATION

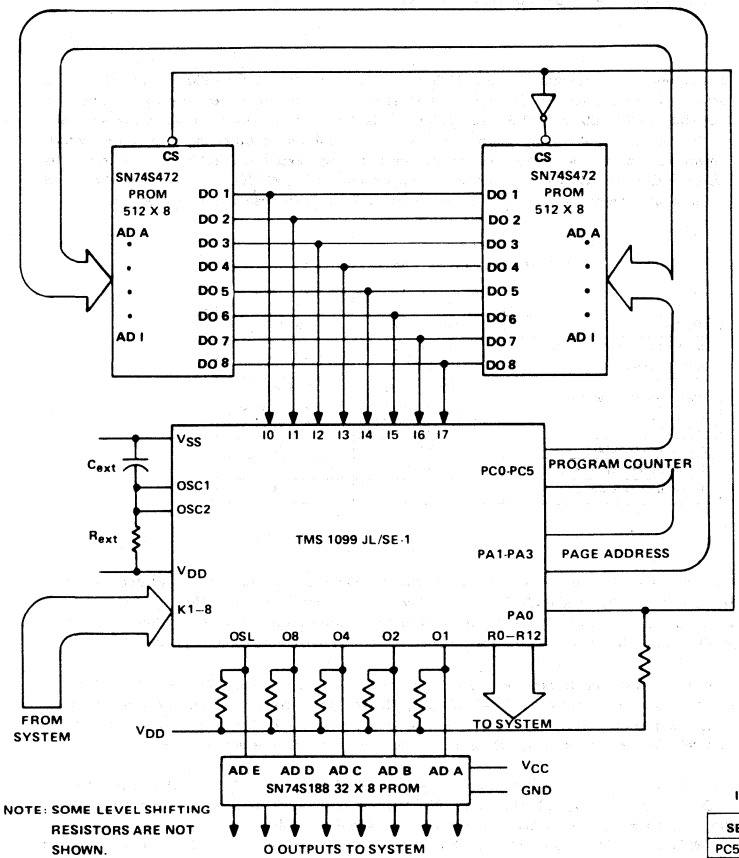
When the system evaluators are combined with external instruction memory, their operation is identical to their respective TMS 1000 series devices described in the *"TMS 1000 Series Programmer's Reference Manual"* (CM 122-1). A dedicated parallel-instruction address selects the instruction word that transfers into the system evaluator through a dedicated eight-bit-parallel input. Therefore, the user does not need external timing or multiplexing circuits.

To store the program, Texas Instruments provide a variety of memory products. The TTL PROM's, SN74S470, 'S471, 'S472, and 'S473, and TTL RAM's, SN74S209 and 'S309, store the instruction codes for program execution by the system evaluator. These TTL RAM's, as well as the MOS static RAM's such as the TMS 4033, are convenient when a teletype or paper-tape interface is available for entering an assembled program.

The system evaluators O-output Programmable Logic Array (PLA) transfers the five-bit O-register contents directly to the five O outputs, O1, O2, O4, O8, and OSL. Various devices are available that can emulate the O-output PLA coding. If seven-segment displays are used, an SN7448, SN7449, or equivalent, is ideal. For nonstandard codes, an SN74188 PROM (organized as 32 X 8) provides the code conversion (two required for users with TMS 1270 applications having ten O outputs).

If the system evaluators are used to emulate the TMS 1000 series devices, the user must remember that the O-output PLA has a maximum of 20 product terms. Refer to the O-output PLA description in the *TMS 1000 Series Programmer's Reference Manual* for details.

Figure 9 and 10 show typical configurations with the system evaluators in prototyping systems.

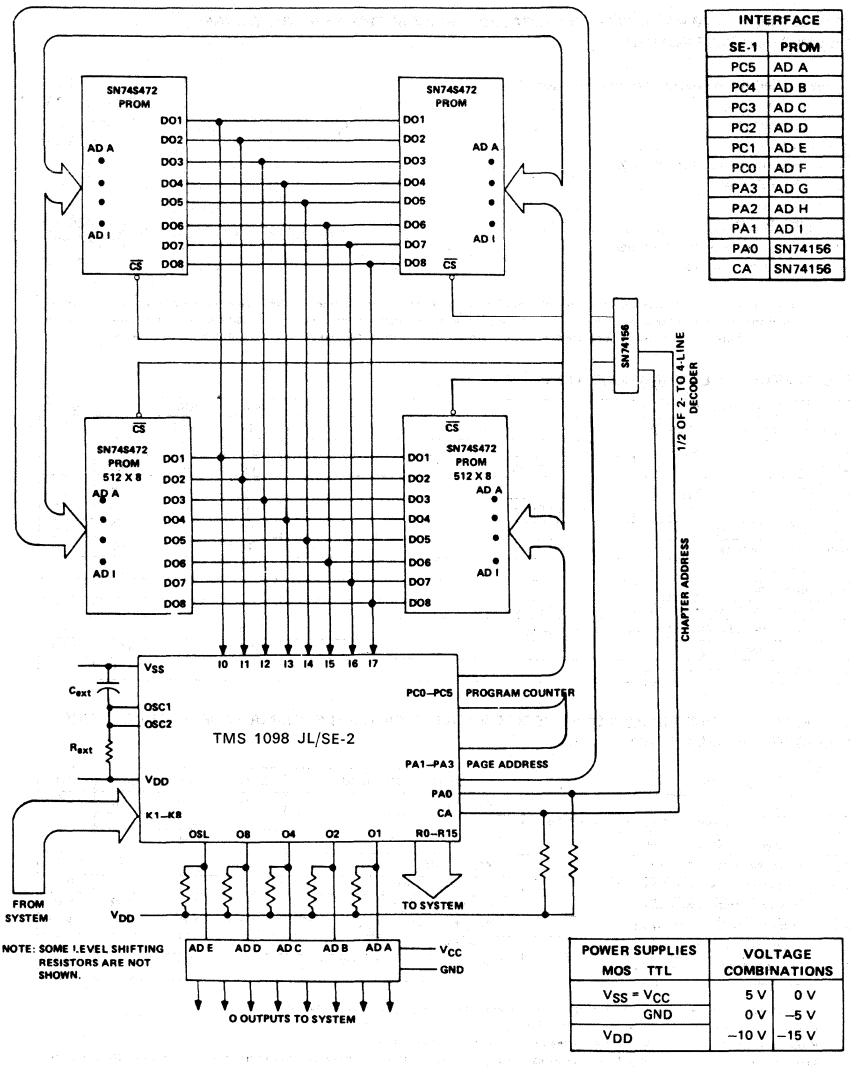


POWER SUPPLIES MOS	POWER SUPPLIES TTL	VOLTAGE COMBINATIONS	
V_{SS} = V_{CC}	GND	5 V	0 V
V_{DD}		−10 V	−15 V

INTERFACE

SE-1	PROM
PC5	AD A
PC4	AD B
PC3	AD C
PC2	AD D
PC1	AD E
PC0	AD F
PA3	AD G
PA2	AD H
PA1	AD I
PA0/$\overline{PA0}$	$\overline{CS}$

FIGURE 9 – BLOCK DIAGRAM OF TYPICAL APPLICATION – PROTOTYPING SYSTEM WITH SE-1



INTERFACE	
SE-1	PROM
PC5	AD A
PC4	AD B
PC3	AD C
PC2	AD D
PC1	AD E
PC0	AD F
PA3	AD G
PA2	AD H
PA1	AD I
PA0	SN74156
CA	SN74156

POWER SUPPLIES MOS	POWER SUPPLIES TTL	VOLTAGE COMBINATIONS	
$V_{SS} = V_{CC}$		5 V	0 V
GND		0 V	–5 V
V_{DD}		–10 V	–15 V

FIGURE 10 – BLOCK DIAGRAM OF TYPICAL APPLICATION – PROTOTYPING SYSTEM WITH SE-2

6.3 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Voltage applied to any device terminal (see Note 1) . . . . . −20 V
Supply voltage, V_{DD} . . . . . −20 V to 0.3 V
Data input voltage . . . . . −20 V to 0.3 V
Clock input voltage . . . . . −20 V to 0.3 V
Average output current (see Note 2)
O, R, PC, PA, CA . . . . . −14 mA
Peak output current
O, R, PC, PA, CA . . . . . −28 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

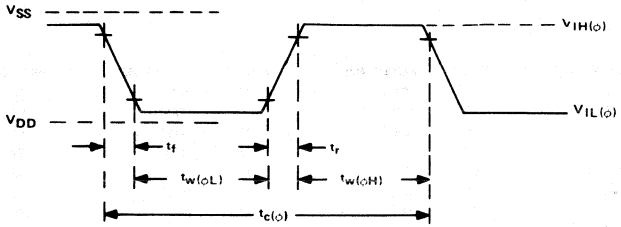
6.4 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 3)		−14	−15	−17.5	V
High-level input voltage, V_{IH} (see Note 4)	K	−1.3	−1	0.3	V
	INIT or Clock	−1.3	−1	0.3	
Low-level input voltage, V_{IL} (see Note 4)	K	V_{DD}		−4	V
	INIT or Clock	V_{DD}	−15	−8	
Clock cycle time, $t_{c(\phi)}$		2.5	3	10	µs
Instruction cycle time, t_c		15		60	µs
Pulse width, clock high, $t_{w(\phi H)}$		1			µs
Pulse width, clock low, $t_{w(\phi L)}$		1			µs
Sum of rise time and pulse width, clock high, $t_r + t_{w(\phi H)}$		1.25			µs
Sum of fall time and pulse width, clock low, $t_f + t_{w(\phi L)}$		1.25			µs
Oscillator frequency, f_{osc}		100		400	kHz
Operating free-air temperature, T_A		0		70	°C

6.5 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_I	Input current		$V_I = V_{SS}$		50	300	500	µA
V_{OH}	High-level output voltage (see Note 3)	O, PC, PA, and CA	$I_O = -2$ mA		−1	−0.5		V
		R			−0.75	−0.4		
I_{OL}	Low-level output current		$V_{OL} = V_{DD}$				−100	µA
$I_{DD(av)}$	Average supply current from V_{DD}		All outputs open			−7	−11	mA
$P_{(AV)}$	Average power dissipation		All outputs open			105	193	mW
f_{osc}	Internal oscillator frequency		R_{ext} = 50 kΩ,	C_{ext} = 47 pF	250	300	350	kHz
C_i	Input capacitance		$V_I = 0$ V,	f = 1 kHz		10		pF
$C_{i(\phi)}$	Input capacitance, clock input		$V_I = 0$ V,	f = 100 kHz		25		pF

NOTES: 1. Throughout this data sheet supply voltage values are with respect to V_{SS}, unless otherwise noted.
2. Average current is specified over any 100-ms period.
3. Ripple must not exceed 0.3 volts peak-to-peak in the operating frequency range.
4. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this specification for logic voltage levels only.

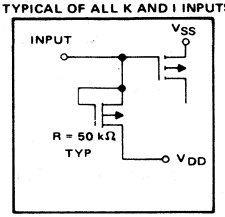


NOTE: Timing points are 90% (high) and 10% (low).

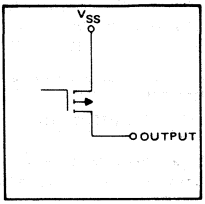
FIGURE 11 – EXTERNALLY DRIVEN CLOCK INPUT WAVEFORM

6.6 SCHEMATICS OF INPUTS AND OUTPUTS

TYPICAL OF ALL K AND I INPUTS



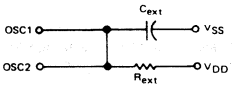
TYPICAL OF ALL O, R, PC, AND PA OPEN-DRAIN OUTPUTS



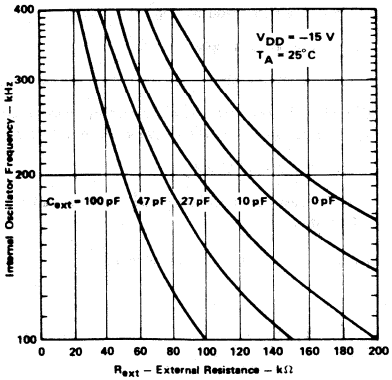
6.7 INTERNAL OR EXTERNAL CLOCK

If the internal oscillator is used, OSC1 and OSC2 terminals are shorted together and tied to an external resistor to V_{DD} and a capacitor to V_{SS}. If an external clock is desired, the clock source may be connected to OSC1 and OSC2 shorted to V_{SS}.

CONNECTION FOR INTERNAL OSCILLATOR



TYPICAL INTERNAL OSCILLATOR FREQUENCY
vs
EXTERNAL RESISTANCE



6.8 TERMINAL ASSIGNMENTS

PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	NC	17	PC4	33	NC	49	NC
2	NC	18	PC3	34	R11*	50	PA0
3	O4	19	PC2	35	R12*	51	NC
4	NC	20	PC1	36	R13*	52	I0
5	O2	21	NC	37	R14*	53	NC
6	NC	22	R3	38	R15*	54	I1
7	O1	23	R4	39	NC	55	NC
8	NC	24	R5	40	V_{DD}	56	I2
9	OSC1	25	NC	41	PA2	57	OSL
10	OSC2	26	NC	42	PA3	58	I3
11	V_{SS}	27	R6	43	K1	59	I4
12	R0	28	R7	44	K2	60	I5
13	R1	29	R8	45	K4	61	I6
14	R2	30	R9	46	K8	62	I7
15	CA, SE-2 (NC, SE-1)	31	R10	47	PA1	63	O8
16	PC5	32	PC0	48	INIT	64	NC

*The user determines which R outputs are appropriate for a specified device emulation. Note the device descriptions.
NC – NO INTERNAL CONNECTION

6.9 TERMINAL FUNCTION DESCRIPTION

1. PC0 → PC5 are the ROM program-counter outputs with PC0 being the most-significant bit and PC5 being the least-significant bit. The addresses change in a non-sequential binary manner.
2. PA0 → PA3 are the ROM page-address outputs with PA0 being the most-significant bit.
3. CA is the ROM chapter address output for the SE-2.
4. I0 → I7 are the external-memory-instruction inputs with I0 being the most-significant bit.
5. O1, O2, O4, O8, and OSL are the data outputs latched in the O register, with O1 being the least-significant bit and OSL being the output of the status latch.
6. K1, K2, K4, and K8 are the data input lines with K1 being the least-significant bit of those inputs.
7. R0 → R15 are the R-output register outputs.
8. V_{DD} is the power-supply input.
9. V_{SS} is the ground pin.
10. OSC1† is the oscillator input if driven by an external clock. OSC1 and OSC2 are shorted together to operate with the internal oscillator. The frequency is controlled by an external RC circuit.
11. OSC2 is the oscillator output.
12. INIT is used for power-on initialization or hardware reset (see the *Programmer's Reference Manual* for more information).

†If an external clock is used, OSC2 is tied to V_{SS}.

7. HE-2 HARDWARE EVALUATOR

7.1 INTRODUCTION

The HE-2 is a register-level emulator and debugging unit for TMS 1000 series microcomputers. The software simulation provided by time-sharing processing combined with the HE-2 having such features as single-step, repetitive step, breakpoint, RAM inspection, and manual load for instructions make significant improvements in design-cycle time possible. The unit is especially valuable when programs that control mechanical devices or several peripherals must be verified in real time. If problems are encountered in the laboratory, there is no need for immediate reassembly of the code since algorithm changes can be entered manually into the instruction RAM's. RAM's are used for the instruction memory, instruction decoder, and the output decoder. Thus, each programmable portion of the TMS 1000 series devices is modified by a paper-tape input, rather than programming a PROM every time a design change occurs.

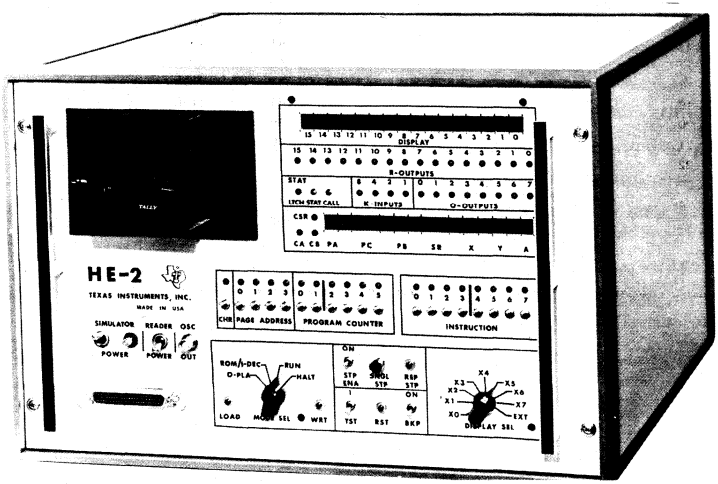
Since every day saved in new-product development can represent thousands of dollars, the hardware evaluator will usually pay for itself many times over in the first project.

The HE-2 emulates all microcomputers in the TMS 1000 series. By removing a small PC board, the HE-2 can emulate the TMS 1000, TMS 1200, TMS 1070, or the TMS 1270. Replacing the PC board enables emulation of the TMS 1100 and TMS 1300.

7.2 CONTROLS AND FRONT PANEL

All of the internal status bits, register and RAM contents, and instruction codes are displayed on the front panel. Address and instruction bit switches control the memory inspection and manual entry mode. In the halt mode or with breakpoint, a display select switch allows RAM inspection at any point in the program execution. The step enable allows the designer to cycle through single instructions or through multiple instructions at a 2-Hz to 3-Hz rate.

A complete operation guide is available upon request for review. A manual is shipped with each system purchased.



7.3 ELECTRICAL AND MECHANICAL FEATURES

Implementation: MOS and BiPolar

Space Requirements: 19 1/2" wide X 13" high X 25 1/4" deep

Paper Tape Reader: Front panel mounted (50 characters per second)

Power Requirements: 120 V ac, 2 amperes, 50 to 60 Hz

Cooling: Self contained, rear of chassis

Connector: Amphenol #57-20500 fernale

Self-Contained Oscillator: 100 kHz to 400 kHz, adjustable.

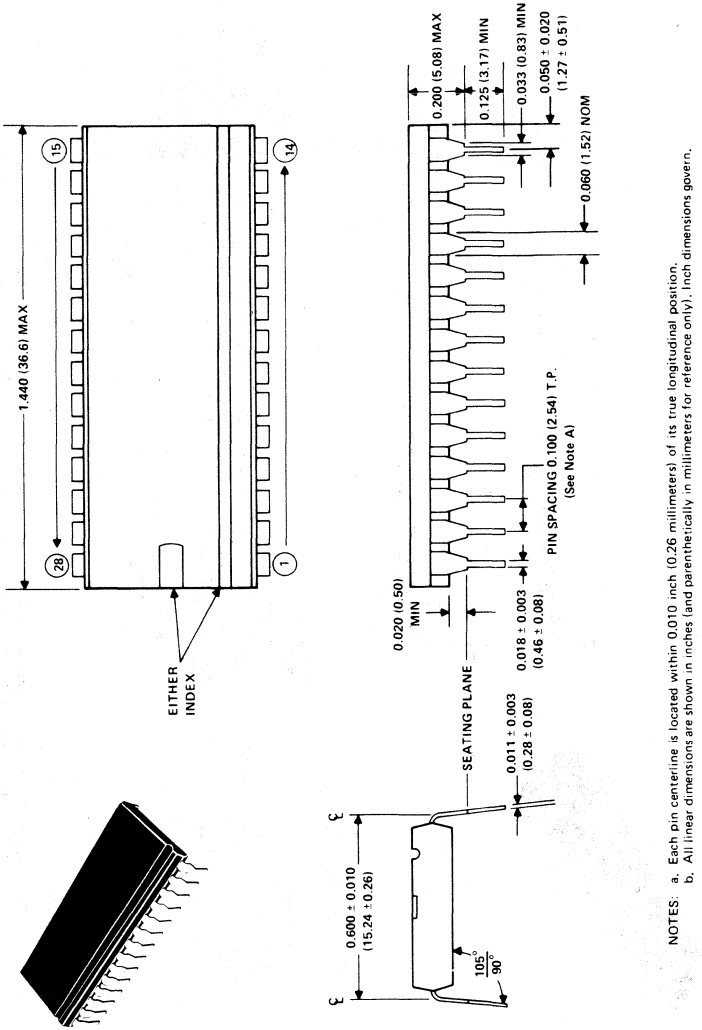
7.4 CONNECTOR PIN ASSIGNMENTS

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	R0	26	K2
2	R1	27	K4
3	R2	28	K8
4	R3	29	INIT
5	R4	30	NC
6	R5	31	NC
7	R6	32	NC
8	R7	33	NC
9	R8	34	NC
10	R9	35	NC
11	R10	36	NC
12	R11	37	NC
13	R12	38	NC
14	R13	39	NC
15	R14	40	NC
17	R15	41	NC
17	O0	42	NC
18	O1	43	NC
19	O2	44	GND
20	O3	45	GND
21	O4	46	GND
22	O5	47	NC
23	O6	48	+5 V }
24	O7	49	+5 V } 1A maximum
25	K1	50	+5 V }

NOTE: The R and O outputs have standard push-pull TTL outputs. Each K input uses an emitter-follower input buffer with a five-volt power supply.

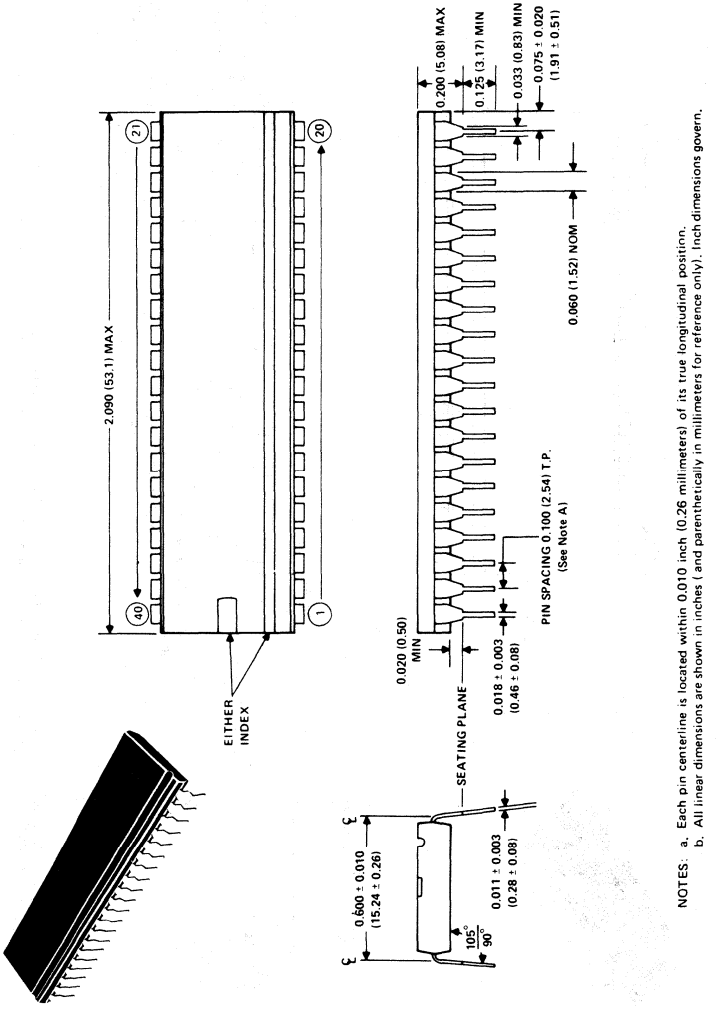
8. MECHANICAL DATA

8.1 TMS 1000 NL, TMS 1070 NL, TMS 1100 NL – 28-PIN PLASTIC PACKAGE



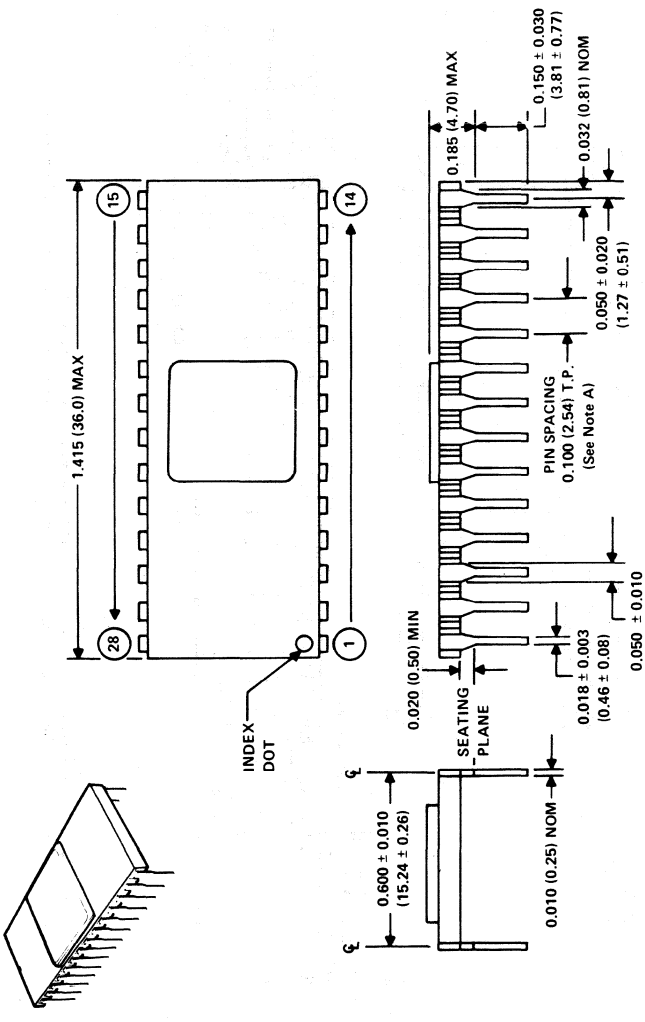
NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

8.2 TMS 1200 NL, TMS 1270 NL, TMS 1300 NL – 40-PIN PLASTIC PACKAGE



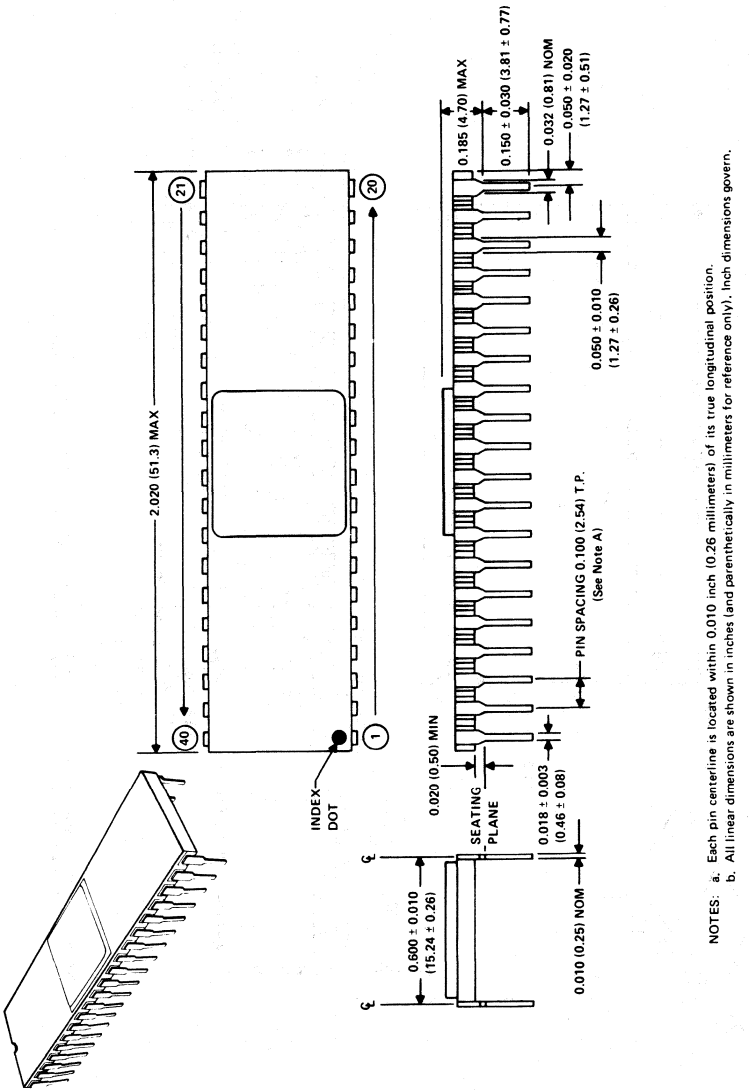
NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal positinn.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

8.3 TMS 1000 JL, TMS 1070 JL, TMS 1100 JL – 28-PIN CERAMIC PACKAGE



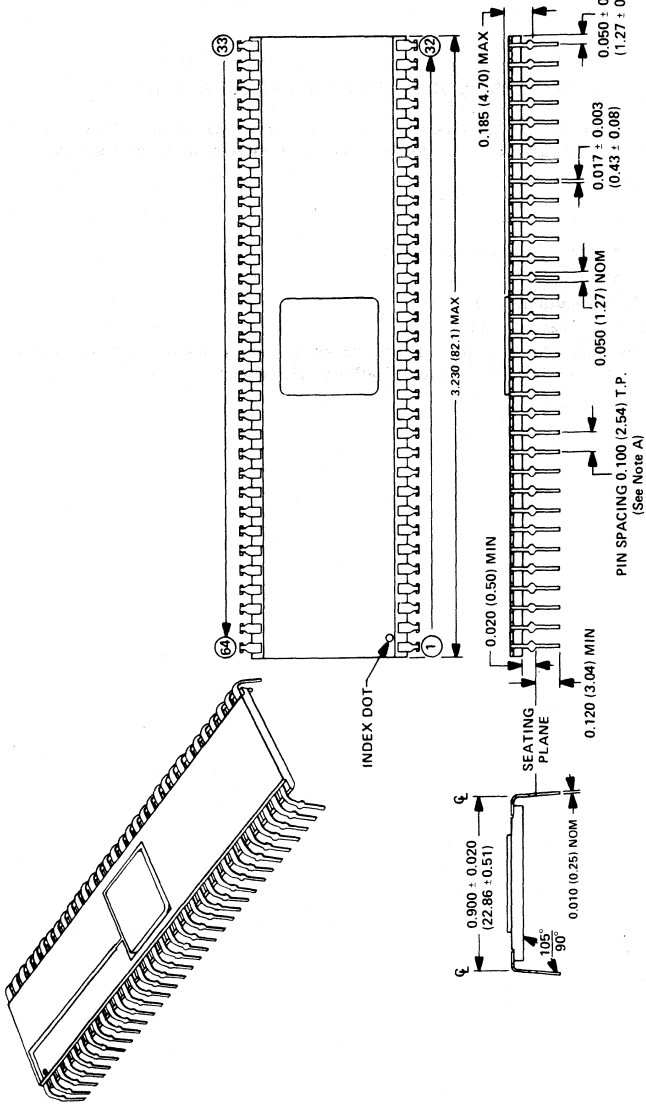
NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

8.4 TMS 1200 JL, TMS 1270 JL, TMS 1300 JL – 40-PIN CERAMIC PACKAGE



NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

8.5 TMS 1099 JL/SE-1, TMS 1098 JL/SE-2



NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

TMS 2000
ONE-CHIP MICROCOMPUTER

TMS 2000 SERIES OF LOW COST MICROCOMPUTERS

The TMS 2000 series of microcomputers are N-channel Silicon Gate implementations of the TMS 1000 series of one-chip microcomputers. The devices have been designed to be plug-in replacements for the TMS 1000 but with enhanced performance.

Features

- Full TMS1000 Instruction Set and Architecture
- 5 volt Single Power Supply
- 5μsec Instruction Execution Time
- TTL compatible inputs and outputs
- Ideally suited for high volume control applications which require low power supply voltages i.e. Automotive – existing TTL systems – battery operated systems

TMS 8080
Microprocessor

1. ARCHITECTURE

1.1 INTRODUCTION

The TMS 8080 is an 8-bit parallel central processing unit (CPU) fabricated on a single chip using a high-speed N-channel silicon-gate process. (See Figure 1). A complete microcomputer system with a 2-μs instruction cycle can be formed by interfacing this circuit with any appropriate memory. Separate 8-bit data and 16-bit address buses simplify the interface and allow direct addressing of 65,536 bytes of memory. Up to 256 input and 256 output ports are also provided with direct addressing. Control signals are brought directly out of the processor and all signals, excluding clocks, are TTL compatible.

1.2 THE STACK

The TMS 8080 incorporates a stack architecture in which a portion of external memory is used as a pushdown stack for storing data from working registers and internal machine status. A 16-bit stack pointer (SP) is provided to facilitate stack location in the memory and to allow almost unlimited interrupt handling capability. The CALL and RST (restart) instructions use the SP to store the program counter (PC) into the stack. The RET (return) instruction uses the SP to acquire the previous PC value. Additional instructions allow data from registers and flags to be saved in the stack.

1.3 REGISTERS

The TMS 8080 has three categories of registers: general registers, program control registers, and internal registers. The general registers and program control registers are listed in Table 1. The internal registers are not accessible by the programmer. They include the instruction register, which holds the present instruction, and several temporary storage registers to hold internal data or latch input and output addresses and data.

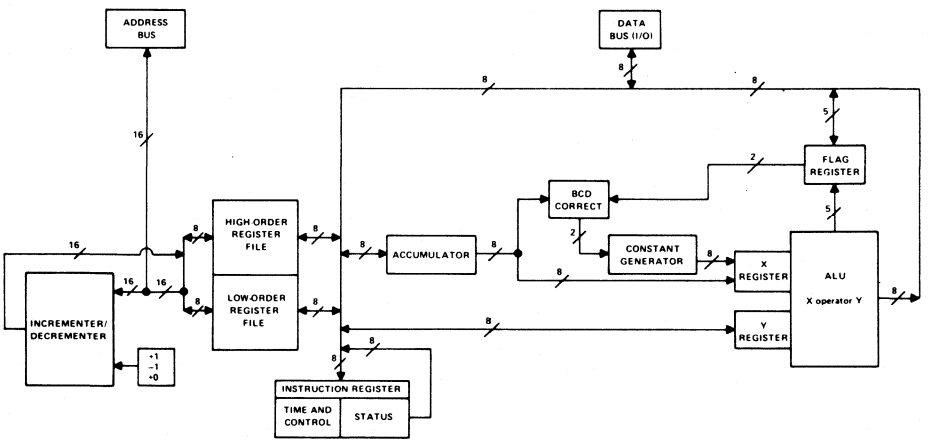


FIGURE 1–TMS 8080 FUNCTIONAL BLOCK DIAGRAM

1.4 THE ARITHMETIC UNIT

Arithmetic operations are performed in an 8-bit parallel arithmetic unit that has both binary and decimal capabilities. Four testable internal flag bits are provided to facilitate program control, and a fifth flag is used for decimal corrections. Table 2 defines these flags and their operation. Decimal corrections are performed with the DAA instruction. The DAA corrects the result of binary arithmetic operation on BCD data as shown in Table 3.

1.5 STATUS & CONTROL

Two types of status are provided by the TMS8080. Certain status is indicated by dedicated control lines. Additional status is transmitted on the data bus during the beginning of each instruction cycle (machine cycle). Table 3 indicates the pin functions of the TMS8080. Table 4 defines the status information that is presented during the beginning of each machine cycle (SYNC time) on the data bus.

1.6 I/O OPERATIONS

Input/output operations (I/O) are performed using the IN and OUT instructions. The second byte of these instructions indicates the device address (256 device addresses). When an IN instruction is executed, the input device address appears in duplicate on A7 through A0 and A15 through A8, along with $\overline{WO}$ and INP status on the data bus. The addressed input device then puts its input data on the data bus for entry into the accumulator. When an OUT instruction is executed, the same operation occurs except that the data bus has OUT status and then has output data.

Direct memory access channels (DMA) can be OR-tied directly with the data and address buses through the use of the HOLD and HLDA (hold acknowledge) controls. When a HOLD request is accepted by the CPU, HLDA goes high, the address and data lines are forced to a high-impedance or "floating" condition, and the CPU stops until the HOLD request is removed.

Interfacing with different speed memories is easily accomplished by use of the WAIT and READY pins. During each machine cycle, the CPU polls the READY input and enters a wait condition until the READY line becomes true. When the WAIT output pin is high, it indicates that the CPU has entered the wait state.

Designing interrupt driven systems is simplified through the use of vectored interrupts. At the end of each instruction, the CPU polls the INT input to determine if an interrupt request is being made. This action does not occur if the CPU is in the HOLD state or if interrupts are disabled. The INTE output indicates if the interrupt logic is enabled (INTE is high). When a request is honored, the INTA status bit becomes high, and an RST instruction may be inserted to force the CPU to jump to one of eight possible locations. Enabling or disabling interrupts is controlled by special instructions (EI or DI). The interrupt input is automatically disabled when an interrupt request is accepted or when a RESET signal is received.

1.7 INSTRUCTION TIMING

The execution time of the instructions varies depending on the operation required and the number of memory references needed. A machine cycle is defined to be a memory referencing operation and is either 3, 4, or 5 state times long. A state time (designated S) is a full cycle of clocks $\phi 1$ and $\phi 2$. (NOTE: The exception to this rule is the DAD instruction, which consists of 1 memory reference in 10 state times). The first machine cycle (designated M1) is either 4 or 5 state times long and is the "instruction fetch" cycle with the program counter appearing on the address bus. The CPU then continues with as many M cycles as necessary to complete the execution of the instruction (up to a maximum of 5). Thus the instruction execution time varies from 4 state times (several including ADDr) to 18 (XTHL). The WAIT or HOLD conditions may affect the execution time since they can be used to control the machine (for example to "single step") and the HALT instruction forces the CPU to stop until an interrupt is received. As the instruction execution is completed (or in the HALT state) the INT pin is polled for an interrupt. In the event of an interrupt, the PC will not be incremented during the next M1 and an RST instruction can be inserted.

TABLE 1
TMS 8080 REGISTERS

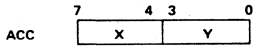
NAME	DESIGNATOR	LENGTH	PURPOSE
Accumulator	A	8	Used for arithmetic, logical, and I/O operations
B Register	B	8	General or most significant 8 bits of double register BC
C Register	C	8	General or least significant 8 bits of double register BC
D Register	D	8	General or most significant 8 bits of double register DE
E Register	E	8	General or least significant 8 bits of double register DE
H Register	H	8	General or most significant 8 bits of double register HL
L Register	L	8	General or least significant 8 bits of double register HL
Program Counter	PC	16	Contains address of next byte to be fetched
Stack Pointer	SP	16	Contains address of the last byte of data saved in the memory stack
Flag Register	F	5	Five flags (C, Z, S, P, C1)

NOTE: Registers B and C may be used together as a single 16-bit register, likewise, D and E, and H and L.

TABLE 2
FLAG DESCRIPTIONS

SYMBOL	TESTABLE	DESCRIPTION
C	YES	C is the carry/borrow out of the MSB (most significant bit) of the ALU (Arithment Logic Unit). A TRUE condition (C = 1) indicates overflow for addition or underflow for subtraction.
Z	YES	A TRUE condition (Z = 1) indicates that the output of the ALU is equal to zero.
S	YES	A TRUE condition (S = 1) indicates that the MSB of the ALU output is equal to a one (1).
P	YES	A TRUE condition (P = 1) indicates that the output of the ALU has even parity (the number of bits equal to one is even).
C1	NO	C1 is the carry out of the fourth bit of the ALU (TRUE condition). C1 is used only for BCD correction with the DAA instruction.

TABLE 3
FUNCTION OF THE DAA INSTRUCTION
Assume the accumulator (A) contains two BCD digits, X and Y



ACCUMULATOR BEFORE DAA				ACCUMULATOR AFTER DAA			
C	$A_7 \ldots A_4$	C1	$A_3 \ldots A_0$	C	$A_7 \ldots A_4$	C1	$A_3 \ldots A_0$
0	X < 10	0	Y < 10	0	X	0	Y
0	X < 10	1	Y < 10	0	X	0	Y + 6
0	X < 9	0	Y ⩾ 10	0	X + 1	1	Y + 6
1	X < 10	0	Y < 10	1	X + 6	0	Y
1	X < 10	1	Y < 10	1	X + 6	0	Y + 6
1	X < 10	0	Y ⩾ 10	1	X + 7	1	Y + 6
0	X ⩾ 10	0	Y < 10	1	X + 6	0	Y
0	X ⩾ 10	1	Y < 10	1	X + 6	0	Y + 6
0	X ⩾ 9	0	Y ⩾ 10	1	X + 7	1	Y + 6

NOTE: The corrections shown in Table 3 are sufficient for addition. For subtraction, the programmer must account for the borrow condition that occur and give erroneous results. The most straight forward method is to set A = 99_{16} and carry = 1. Then add the minuend to A after subtracting the subtrahend from A.

TABLE 4
TMS 8080 PIN DEFINITIONS

SIGNATURE	PIN	I/O	DESCRIPTION
A15 (MSB)	36	OUT	A15 through A0 comprise the address bus. True memory or I/O device addresses appear on this 3-state bus during the first state time of each instruction cycle.
A14	39	OUT	
A13	38	OUT	
A12	37	OUT	
A11	40	OUT	
A10	1	OUT	
A9	35	OUT	
A8	34	OUT	
A7	33	OUT	
A6	32	OUT	
A5	31	OUT	
A4	30	OUT	
A3	29	OUT	
A2	27	OUT	
A1	26	OUT	
A0 (LSB)	25	OUT	
D7 (MSB)	6	IN/OUT	D7 through D0 comprise the bidirectional 3-state data bus. Memory, status, or I/O data is transferred on this bus.
D6	5	IN/OUT	
D5	4	IN/OUT	
D4	3	IN/OUT	
D3	7	IN/OUT	
D2	8	IN/OUT	
D1	9	IN/OUT	
D0 (LSB)	10	IN/OUT	
V_{SS}	2		Ground reference
V_{BB}	11		Supply voltage (−5 V nominal)
V_{CC}	20		Supply voltage (5 V nominal)
V_{DD}	28		Supply voltage (12 V nominal)
$\phi 1$	22	IN	Phase 1 clock.
$\phi 2$	15	IN	Phase 2 clock. See page 15 for $\phi 1$ and $\phi 2$ timing.

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TABLE 4 (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
RESET	12	IN	Reset. When active (high) for a minimum of 3 clock cycles, the RESET input causes the TMS 8080 to be reset. PC is cleared, interrupts are disabled, and after RESET, instruction execution starts at memory location 0. To prevent a lockup condition, a HALT instruction must not be used in location 0.
HOLD	13	IN	Hold signal. When active (high) HOLD causes the TMS 8080 to enter a hold state and float (put the 3-state address and data bus in a high-impedance state). The chip acknowledges entering the hold state with the HLDA signal and will not accept interrupts until it leaves the hold state.
INT	14	IN	Interrupt request. When active (high) INT indicates to the TMS8080 that an interrupt is being requested. The TMS8080 polls INT during a HALT or at the end of an instruction. The request will be accepted except when INTE is low or the CPU is in the HOLD condition.
INTE	16	OUT	Interrupts enabled. INTE indicates that an interrupt will be accepted by the TMS 8080 unless it is in the hold state. INTE is set to a high logic level by the EI (Enable Interrupt) instruction and reset to a low logic level by the DI (Disable Interrupt) instruction. INTE is also reset when an interrupt is accepted and by the A high on RESET.
DBIN	17	OUT	Data bus in. DBIN indicates whether the data bus is in an input or output mode. (high = input, low = output).
WR	18	OUT	Write. When active (low) WR indicates a write operation on the data bus to memory or to an I/O port.
SYNC	19	OUT	Synchronizing control line. When active (high) SYNC indicates the beginning of each machine cycle of the TMS8080. Status information is also present on the data bus during SYNC for external latches.
HLDA	21	OUT	Hold acknowledge. When active (high) HLDA indicates that the TMS8080 is in a hold state.
READY	23	IN	Ready control line. An active (high) level indicates to the TMS 8080 that an external device has completed the transfer of data to or from the data bus. READY is used in conjunction with WAIT for different memory speeds.
WAIT	24	OUT	Wait status. When active (high) WAIT indicates that the TMS8080 has entered a wait state pending a READY signal from memory.

TABLE 5
TMS 8080 STATUS

SIGNATURE	DATA BUS BIT	DESCRIPTION
INTA	D0	Interrupt acknowledge.
$\overline{WO}$	D1	Indicates that current machine cycle will be a read (input) (high = read) or a write (output) (low = write) operation.
STACK	D2	Indicates that address is stack address from the SP.
HLTA	D3	HALT instruction acknowledge.
OUT	D4	Indicates that the address bus has an output device address and the data bus has output data.
M1	D5	Indicates instruction acquisition for first byte.
INP	D6	Indicates address bus has address of input device.
MEMR	D7	Indicates that data bus will be used for memory read data.

INSTRUCTION FORMATS

TMS 8080 instructions are either one, two, or three bytes long and are stored as binary integers in successive memory locations in the format shown below.

One-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE

Two-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE
D7 D8 D5 D4 D3 D2 D1 D0	OPERAND

Three-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE
D7 D6 D5 D4 D3 D2 D1 D0	LOW ADDRESS OR OPERAND 1
D7 D6 D5 D4 D3 D2 D1 D0	HIGH ADDRESS OR OPERAND 2

INSTRUCTION SET SUMMARY (alphabetically listed)

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
ACI	2	Add immediate to A with carry†		C	E	7
ADC M	1	Add memory to A with carry†		8	E	7
ADC r	1	Add register to A with carry†	B	8	8	4
			C	8	9	
			D	8	A	
			E	8	B	
			H	8	C	
			L	8	D	
			A	8	F	
ADD M	1	Add memory to A†		8	6	7
ADD r	1	Add register to A†	B	8	0	4
			C	8	1	
			D	8	2	
			E	8	3	
			H	8	4	
			L	8	5	
			A	8	7	
ADI	2	Add immediate to A†		C	6	7
ANA M	1	AND memory with A†		A	6	7
ANAr	1	AND register with A†	B	A	0	4
ANI	2	AND immediate with A†		E	6	7
CALL	3	Call unconditional		C	D	17
CC	3	Call on carry		D	C	11/17
CM	3	Call on minus		F	C	11/17
CMA	1	Complement A		2	F	4
CMC	1	Complement carry‡		3	F	4
CMP M	1	Compare memory with A†		B	E	7

*Two possible cycle times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.
‡Only carry flag affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
CMP r	1	Compare register with A				
			B	B	8	4
			C	B	9	
			D	B	A	
			E	B	B	
			H	B	C	
			L	B	D	
			A	B	F	
CNC	3	Call on no carry		D	4	11/17
CNZ	3	Call on no zero		C	4	11/17
CP	3	Call on positive		F	4	11/17
CPE	3	Call on parity even		E	C	11/17
CPI	2	Compare immediate with A†		F	E	7
CPO	3	Call on parity odd		E	4	11/17
CZ	3	Call on zero		C	C	11/17
DAA	1	Decimal adjust A†		2	7	4
DAD B	1	Add B&C to H&L‡		0	9	10
DAD D	1	Add D&E to H&L‡		1	9	10
DAD H	1	Add H&L to H&L‡		2	9	10
DAD SP	1	Add stack pointer to H&L‡		3	9	10
DCR M	1	Decrement Memory§		3	5	10
DCR r	1	Decrement Register§	B	0	5	5
			C	0	D	
			D	1	5	
			E	1	D	
			H	2	5	
			L	2	D	
			A	3	D	
DCX B	1	Decrement B&C		0	B	5
DCX D	1	Decrement D&E		1	B	5
DCX H	1	Decrement H&L		2	B	5
DCX SP	1	Decrement stack pointer		3	B	5
DI	1	Disable interrupts		F	3	4
EI	1	Enable interrupts		F	B	4
HLT	1	Halt		7	6	7
IN	2	Input		D	B	10
INR M	1	Increment memory§		3	4	10
INR r	1	Increment register§	B	0	4	5
			C	0	C	
			D	1	4	
			E	1	C	
			H	2	4	
			L	2	C	
			A	3	C	
INX B	1	Increment B&C register		0	3	5
INX D	1	Increment D&E register		1	3	5
INX H	1	Increment H&L register		2	3	5
INX SP	1	Increment stack pointer		3	3	5
JC	3	Jump on carry		D	A	10
JM	3	Jump on minus		F	A	10

* Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags.
† All flags (C, Z, S, P, C1) affected.
‡ Only carry flag affected.
§ All flags except carry affected

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	D3–D0	CLOCK CYCLES*
JMP	3	Jump unconditional		C	3	10
JNC	3	Jump on no carry		D	2	10
JNZ	3	Jump on no zero		C	2	10
JP	3	Jump on positive		F	2	10
JPE	3	Jump on parity even		E	A	10
JPO	3	Jump on parity odd		E	2	10
JZ	3	Jump on zero		C	A	10
LDA	1	Load A direct		3	A	13
LDAX B	1	Load A indirect		0	A	7
LDAX D	1	Load A indirect		1	A	7
LHLD	3	Load H&L direct		2	A	16
LXI B	3	Load immediate register pair B&C		0	1	10
LXI D	3	Load immediate register pair D&E		1	1	10
LXI H	3	Load immediate register		2	1	10
LXI SP	3	Load immediate stack pointer		3	1	10
MOV M,r	1	Move register to memory	B	7	0	7
			C	7	1	
			D	7	2	
			E	7	3	
			H	7	4	
			L	7	5	
			A	7	7	
MOV r,M	1	Move memory to register	B	4	6	7
			C	4	E	
			D	5	6	
			E	5	E	
			H	6	6	
			L	6	E	
			A	7	E	
MOV r_1, r_2	1	Move register to register	B,B	4	0	5
			B,C	4	1	
			B,D	4	2	
			B,E	4	3	
			B,H	4	4	
			B,L	4	5	
			B,A	4	7	
			C,B	4	8	
			C,C	4	9	
			C,D	4	A	
			C,E	4	B	
			C,H	4	C	
			C,L	4	D	
			C,A	4	F	
			D,B	5	0	
			D,C	5	1	
			D,D	5	2	
			D,E	5	3	
			D,H	5	4	
			H,L	5	5	
			D,A	5	7	
			E,B	5	8	

*Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	D3–D0	CLOCK CYCLES*
MOV r_1, r_2	1	Move register to register (continued)	E,C	5	9	
			E,D	5	A	
			E,E	5	B	
			E,H	5	C	
			E,L	5	D	
			E,A	5	F	
			H,B	6	0	
			H,C	6	1	
			H,D	6	2	
			H,E	6	3	
			H,H	6	4	
			H,L	6	5	
			H,A	6	7	
			L,B	6	8	
			L,C	6	9	
			L,D	6	A	
			L,E	6	B	
			L,H	6	C	
			L,L	6	D	
			L,A	6	F	
			A,B	7	8	
			A,C	7	9	
			A,D	7	A	
			A,E	7	B	
			A,H	7	C	
			A,L	7	D	
			A,A	7	F	
MVI M	2	Move immediate memory		3	6	10
MVI r	2	Move immediate register	B	0	6	7
			C	0	E	
			D	1	6	
			E	1	E	
			H	2	6	
			L	2	E	
			A	3	E	
NOP	1	No operation		0	0	4
ORA M	1	OR memory with A†		B	6	7
ORA r	1	OR register with A†	B	B	0	4
			C	B	1	
			D	B	2	
			E	B	3	
			H	B	4	
			L	B	5	
			A	B	7	
ORI	2	OR immediate with A†		F	6	7
OUT	2	Output		D	3	10
PCHL	1	H&L to program counter		E	9	5
POP B	1	Pop register pair B&C off stack		C	1	10
POP D	1	Pop register pair D&E off stack		D	1	10
POP H	1	Pop register pair H&L off stack		E	1	10
POP PSW	1	Pop A and flags off stack†		F	1	10

*Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	D3–D0	CLOCK CYCLES*
PUSH B	1	Push register pair B&C		C	5	11
PUSH D	1	Push register pair D&C		D	5	11
PUSH H	2	Push register pair H&L on stack		E	5	11
PUSH PSW	1	Push A and Flags on stack		F	5	11
RAL	1	Rotate A left through carry ‡		1	7	4
RAR	1	Rotate A right through carry‡		1	F	4
RC	1	Return on carry		D	8	5/11
RET	1	Return		C	9	10
RLC	1	Rotate A left‡		0	7	4
RM	1	Return on minus		F	8	5/11
RNC	1	Return on no carry		D	0	5/11
RNZ	1	Return on no zero		C	0	5/11
RP	1	Return on positive		F	0	5/11
RPE	1	Return on parity even		E	8	5/11
RPO	1	Return on parity odd		E	0	5/11
RRC	1	Rotate A right‡		0	F	4
RST	1	Restart				11
			$PC \leftarrow 0000_{16}$	C	7	
			$PC \leftarrow 0008_{16}$	C	F	
			$PC \leftarrow 0010_{16}$	D	7	
			$PC \leftarrow 0018_{16}$	D	F	
			$PC \leftarrow 0020_{16}$	E	7	
			$PC \leftarrow 0028_{16}$	E	F	
			$PC \leftarrow 0030_{16}$	F	7	
			$PC \leftarrow 0038_{16}$	F	F	
RZ	1	Return on Zero		C	8	5/11
SBB M	1	Subtract memory from A with borrow†		9	E	7
SBB r	1	Subtract register from A with borrow†	B	9	8	4
			C	9	9	
			D	9	A	
			E	9	B	
			H	9	C	
			L	9	D	
			A	9	F	
SBI	2	Subtract immediate from A with borrow†		D	E	7
SHLD	3	Store H&L direct		2	2	16
SPHL	1	H&L to stack pointer		F	9	5
STA	3	Store A direct		3	2	13
STAX B	1	Store A indirect		0	2	7
STAX D	1	Store A indirect		1	2	7
STC	1	Set carry‡		3	7	4
SUB M	1	Subtract memory from A†		9	6	7
SUB r	1	Subtract register from A†	B	9	0	4
			C	9	1	
			D	9	2	
			E	9	3	
			H	9	4	
			L	9	5	
			A	9	7	
SUI	2	Subtract immediate from A†		D	6	7

*Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.
‡Only carry flag affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
XCHG	1	Exchange D&E, H&L registers		E	B	4
XRA M	1	Exclusive OR memory with A†		A	E	7
XRA r	1	Exclusive OR register with A†	B	A	8	4
			C	A	9	
			D	A	A	
			E	A	B	
			H	A	C	
			L	A	D	
			A	A	F	
XRI	2	Exclusive OR immediate with A†		E	E	7
XTHL	1	Exchange top of stack H&L		E	3	18

*Two possible cycle times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.

2. TMS 8080 ELECTRICAL AND MECHANICAL SPECIFICATIONS

2.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1 . . . . . −0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1) . . . . . −0.3 V to 20 V
All input and output voltages (see Note 1) . . . . . −0.3 V to 20 V
Continuous power dissipation . . . . . 1.5 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{SS} unless otherwise noted.

2.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (all inputs except clocks) (see Note 2)	3.3		$V_{CC}+1$	V
High-level clock input voltage, $V_{IH(\phi)}$	$V_{DD}-1$		$V_{DD}+1$	V
Low-level input voltage, V_{IL} (all inputs except clocks) (see Note 3)	−1		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 3)	−1		0.6	V
Operating free-air temperature, T_A	0		70	°C

NOTES: 2. Active pull-up resistors of nominally 2 kΩ will be switched onto the data bus when DBIN is high and the data input voltage is more positive than V_{IH} min.
3. The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only.

2.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current (any input except clocks and data bus	V_I = 0 V to V_{CC}			±10	μA
$I_{I(\phi)}$	Clock input current	$V_{I(\phi)}$ = 0 V to V_{DD}			±10	μA
$I_{I(DB)}$	Input current, data bus	V_{IDB} = 0 V to V_{CC}			−100	μA
$I_{I(hold)}$	Address or data bus input current during hold	$V_{I(ad)}$ or $V_{I(DB)}$ = V_{CC}			10	μA
		$V_{I(ad)}$ or $V_{I(DB)}$ = 0 V			−100	
V_{OH}	High-level output voltage	I_{OH} = 100 μA	3.7			V
V_{OL}	Low-level output voltage	I_{OLDB} = 1.7 mA, I_{OL} = 0.75 mA (any output except DB)			0.45	V
$I_{BB(av)}$	Average supply current from V_{BB}	Operating at $t_{c(\phi)}$ = 480 ns,		−0.01	−1	mA
$I_{CC(av)}$	Average supply current from V_{CC}	T_A = 25°C,		60	75	
$I_{DD(av)}$	Average supply current from V_{DD}	See Note 4		40	67	
C_i	Capacitance, any input except clock	V_{BB} = V_{DD} = V_{SS} = 0 V,		10	20	pF
$C_{i(\phi)}$	Clock input capacitance	V_{SS} = −4.75 to −5.25 V, f = 1 MHz,		5	10	
C_o	Output capacitance	All other pins at 0 V		10	20	

†All typical values are at T_A = 25°C and nominal voltages.

NOTE 4: The supply currents vary inversely with temperature at the rate of 0.45%/°C.

2.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time (see Note 5)	480	2000	ns
$t_{r(\phi)}$	Clock rise time	5	50	ns
$t_{f(\phi)}$	Clock fall time	5	50	ns
$t_{w(\phi1)}$	Pulse width, clock 1 high	60		ns
$t_{w(\phi2)}$	Pulse width, clock 2 high	220		ns
$t_{d(\phi1L-\phi2)}$	Delay time, clock 1 low to clock 2	0		ns
$t_{d(\phi2-\phi1)}$	Delay time, clock 2 to clock 1	70		ns
$t_{d(\phi1H-\phi2)}$	Delay time, clock 1 high to clock 2 (time between leading edges)	130		ns
$t_{su(da-\phi1)}$	Data setup time with respect to clock 1	50		ns
$t_{su(da-\phi2)}$	Data setup time with respect to clock 2	150		ns
$t_{su(hold)}$	Hold input setup time	140		ns
$t_{su(int)}$	Interrupt input setup time	180		ns
$t_{su(rdy)}$	Ready input setup time	120		ns
$t_{h(da)}$	Data hold time (see Note 6)	$t_{PD(DBI)}$		ns
$t_{h(hold)}$	Hold input hold time	0		ns
$t_{h(int)}$	Interrupt input hold time	0		ns
$t_{h(rdy)}$	Ready input hold time	0		ns

NOTES: 5. $t_{c(\phi)} = t_{d(\phi1L-\phi2)} + t_{r(\phi2)} + t_{w(\phi2)} + t_{f(\phi2)} + t_{d(\phi2-\phi1)} + t_{r(\phi1)}$; 480 ns ≤ $t_{c(\phi)}$ ≤ 2000 ns.

6. The data input should be enabled using the DBIN status signal. No bus conflict can then occur and the data hold time requirement is thus assured.

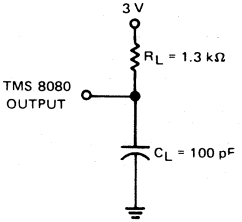
2.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURE)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{PD(ad)}$	Propagation delay time, clock 2 to address outputs	C_L = 100 pF, R_L = 1.3 kΩ		200	ns
$t_{PD(da)}$	Propagation delay time, clock 2 to data bus			220	ns
$t_{PD(cont)}$	Propagation delay time, clocks to control outputs			120	ns
$t_{PD(DBI)}$	Propagation delay time, clock 2 to DBIN output		25	140	ns
$t_{PD(int)}$	Propagation delay time, clock 2 to INTE output			200	ns
t_{DI}	Time for data bus to enter input mode			$t_{PD(DBI)}$	ns
t_{PXZ}	Disable time to high-impedance state during hold (address outputs and data bus)			120	ns

The time that the address outputs and output data will remain stable after $\overline{WR}$ goes high, t_{WA} and $t_{WD} \geq t_{d(\phi 1H\text{-}\phi 2)}$.
The time between address outputs becoming stable and $\overline{WR}$ going low, $t_{AW} \leq 2\ t_{c(\phi)} - t_{d(\phi 1L\text{-}\phi 2)} - t_{r(\phi)} - 120$ ns.
The time between output data becoming stable and $\overline{WR}$ going low, $t_{DW} \geq t_{c(\phi)} - t_{d(\phi 1L\text{-}\phi 2)} - t_{r(\phi)} - 150$ ns.
The following are relevant when interfacing to devices requiring V_{IH} min of 3.3 V:

a) Maximum output rise time (t_{TLH}) from 0.8 V to 3.3 V is 140 ns with C_L as specified for the propagation delay times above.

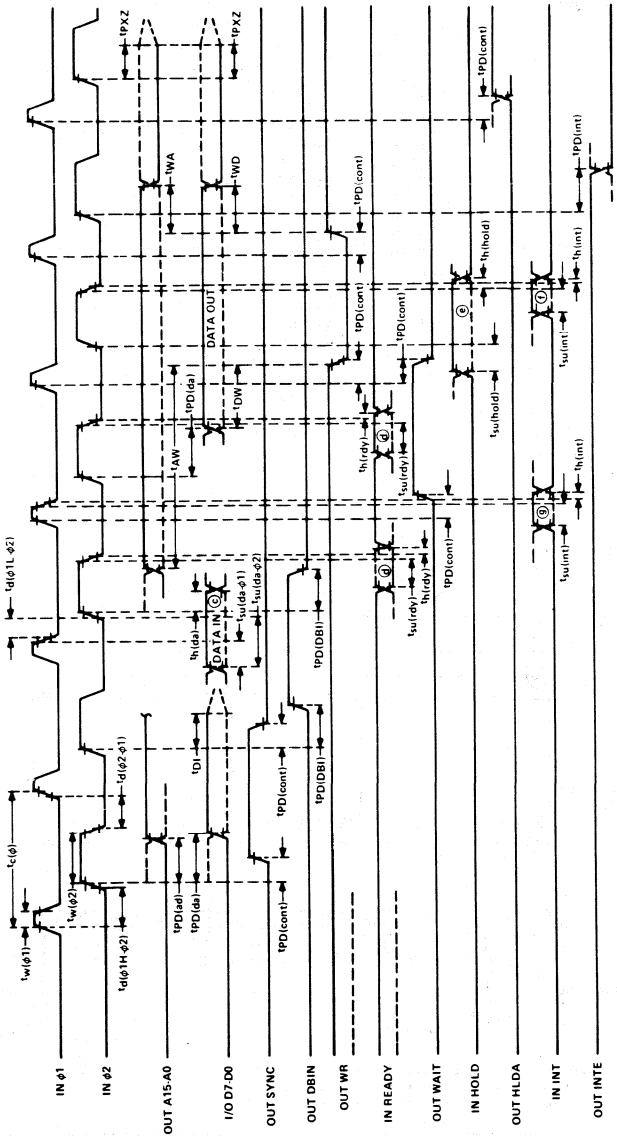
b) Maximum propagation delay times when measured to $V_{ref(H)}$ = 3 V (instead of 2 V) will be 60 ns more than as specified above with C_L as specified.



C_L includes probe and jig capacitance.

LOAD CIRCUIT

voltage waveforms (see notes a and b)

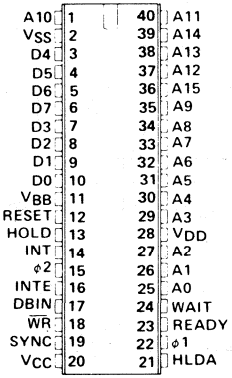


NOTES:
a. This timing diagram shows timing relationships only, it does not represent any specific machine cycle.
b. Time measurements are made at the following reference voltages: Clock $V_{ref(H)} = 9.5$ V, $V_{ref(L)} = 1$ V. Other inputs, $V_{ref(H)} = 2$ V, $V_{ref(L)} = 0.8$ V.
c. Data in must be stable for this period when DBIN is high during S3. Requirements for both $t_{su(da\text{-}ø1)}$ and $t_{su(da\text{-}ø2)}$ must be satisfied.
d. The ready signal must be stable for this period during S2 or SW. This requires external synchronization.
e. The hold signal must be stable for this period during S2 or SW when entering the hold mode and during S3, S4, S5 and SWH when in the hold mode. This requires external synchronization.
f. The interrupt signal must be stable during this period on the last clock cycle of any instruction to be recognized on the following instruction. External synchronization is not required.
g. During halt mode only, timing is with respect to the clock 1 falling edge.

FIGURE 2

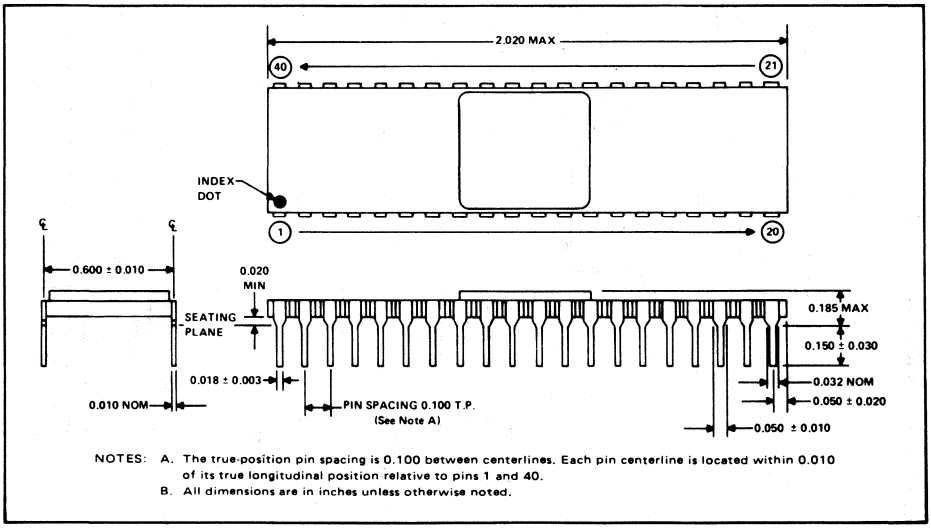
2.6 TERMINAL ASSIGNMENTS

TMS 8080



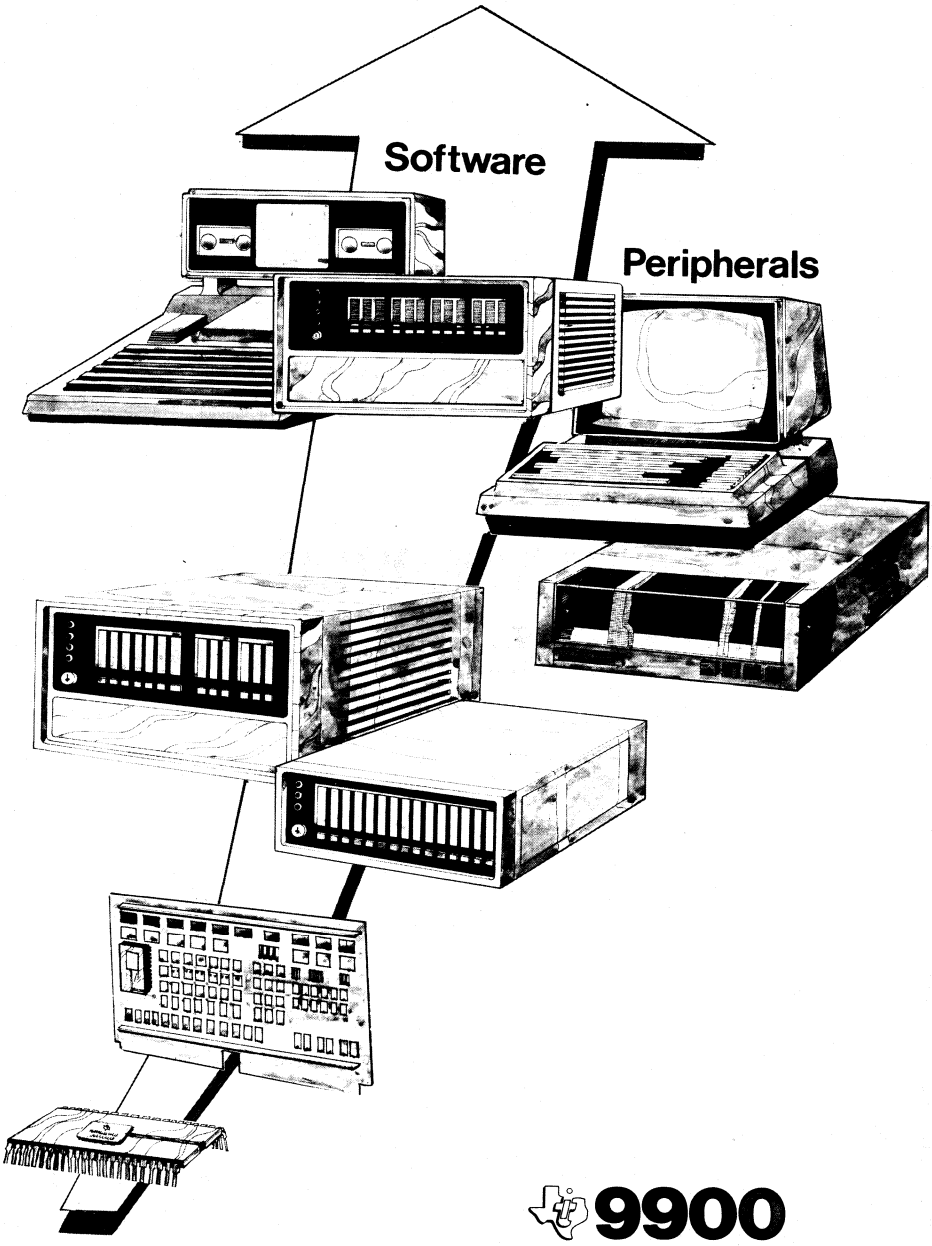
2.7 MECHANICAL DATA

40-PIN CERAMIC PACKAGE



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 40.
B. All dimensions are in inches unless otherwise noted.

TMS 9900
16-bit Microprocessor



9900

Total Family Concept

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1. INTRODUCTION

1.1 DESCRIPTION

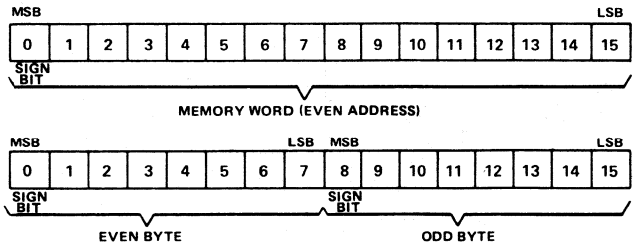
The TMS 9900 microprocessor is a single-chip 16-bit central processing unit (CPU) produced using N-channel silicon-gate MOS technology (see Figure 1). The instruction set of the TMS 9900 includes the capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. Texas Instruments provides a compatible set of MOS and TTL memory and logic function circuits to be used with a TMS 9900 system. The system is fully supported by software and a complete prototyping system.

1.2 KEY FEATURES

- 16-Bit Instruction Word
- Full Minicomputer Instruction Set Capability Including Multiply and Divide
- Up to 65,536 Bytes of Memory
- 3-MHz Speed
- Advanced Memory-to-Memory Architecture
- Separate Memory, I/O, and Interrupt-Bus Structures
- 16 General Registers
- 16 Prioritized Interrupts
- Programmed and DMA I/O Capability
- N-Channel Silicon-Gate Technology

2. ARCHITECTURE

The memory word of the TMS 9900 is 16 bits long. Each word is also defined as 2 bytes of 8 bits. The instruction set of the TMS 9900 allows both word and byte operands. Thus, all memory locations are on even address boundaries and byte instructions can address either the even or odd byte. The memory space is 65,536 bytes or 32,768 words. The word and byte formats are shown below.



2.1 REGISTERS AND MEMORY

The TMS 9900 employs an advanced memory-to-memory architecture. Blocks of memory designated as workspace replace internal-hardware registers with program-data registers. The TMS 9900 memory map is shown in Figure 2. The first 32 words are used for interrupt trap vectors. The next contiguous block of 32 memory words is used by the extended operation (XOP) instruction for trap vectors. The last two memory words, $FFFC_{16}$ and $FFFE_{16}$, are used for the trap vector of the LOAD signal. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory.

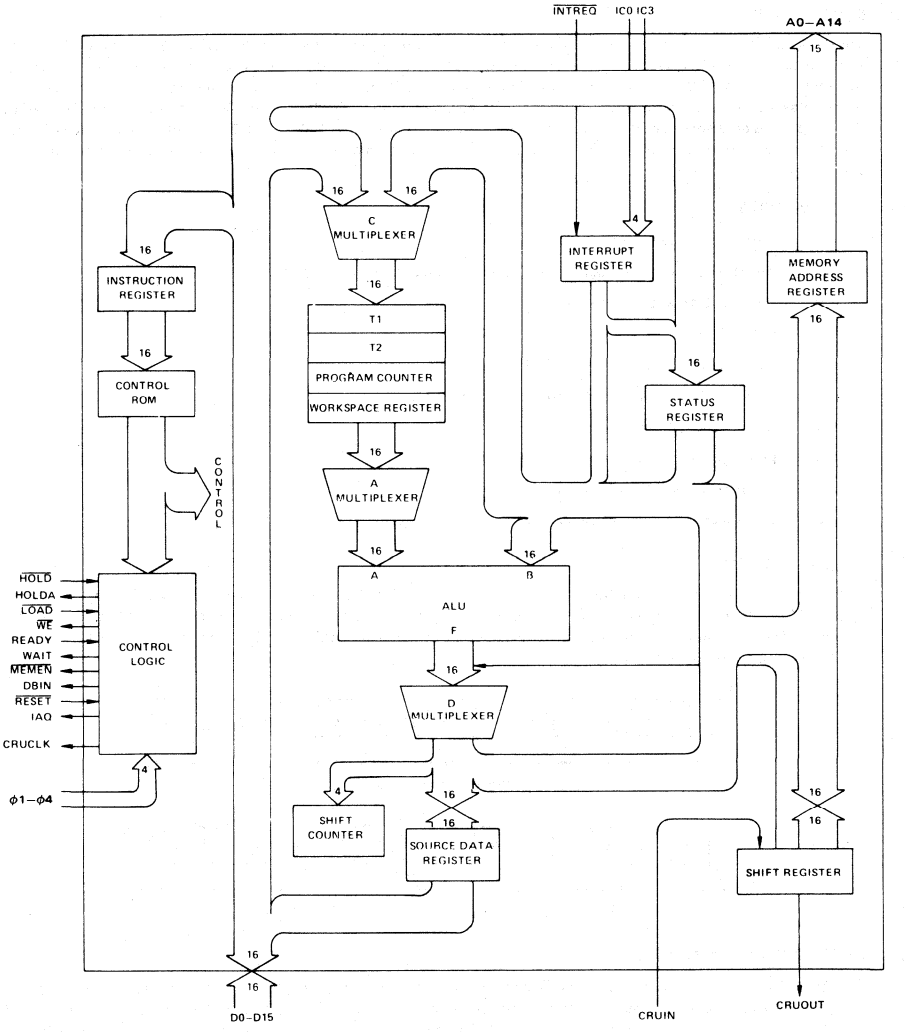
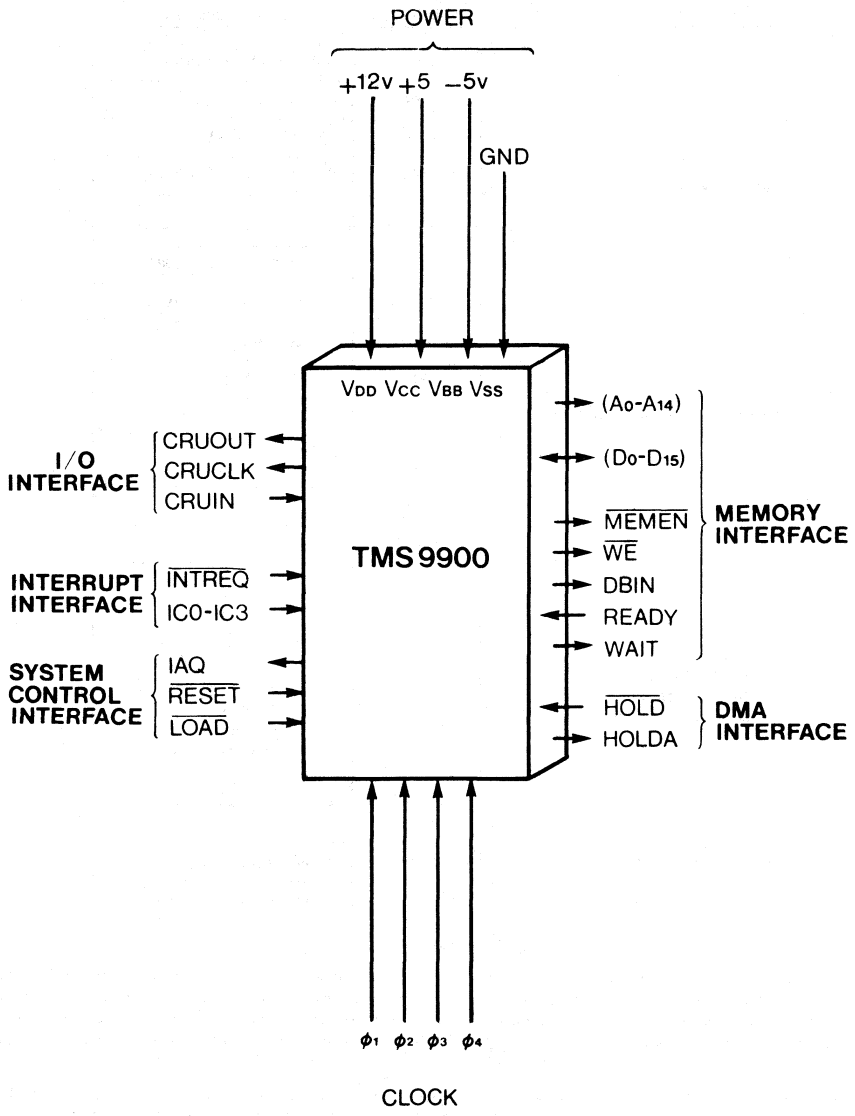


FIGURE 1 – ARCHITECTURE


POWER
+12v +5 −5v
GND
VDD VCC VBB VSS
TMS 9900
I/O INTERFACE
CRUOUT
CRUCLK
CRUIN
INTERRUPT INTERFACE
INTREQ
IC0-IC3
SYSTEM CONTROL INTERFACE
IAQ
RESET
LOAD
(A0-A14)
(D0-D15)
MEMEN
WE
DBIN
READY
WAIT
MEMORY INTERFACE
HOLD
HOLDA
DMA INTERFACE
φ1 φ2 φ3 φ4
CLOCK

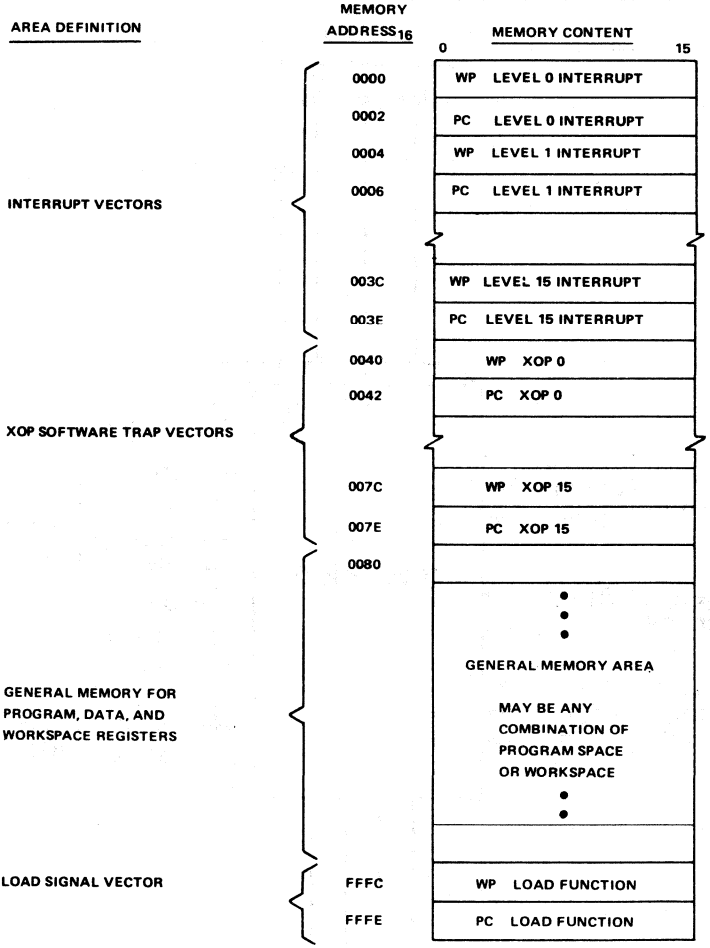
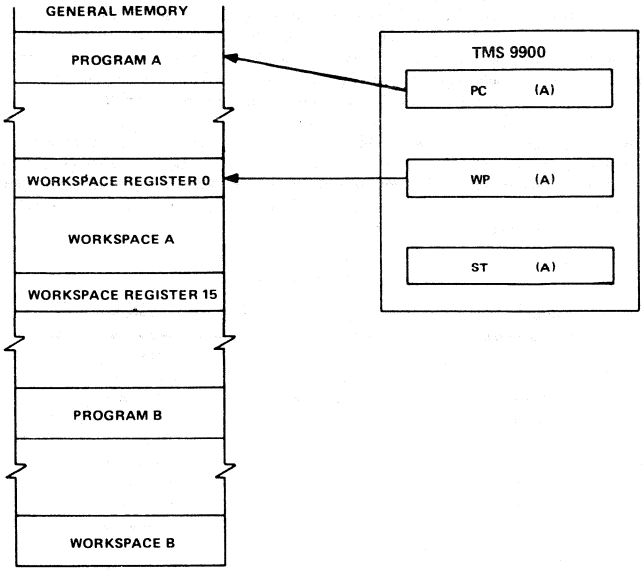


FIGURE 2 – MEMORY MAP

Three internal registers are accessible to the user. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented. The status register (ST) contains the present state of the processor and will be further defined in Section 3.4. The workspace pointer (WP) contains the address of the first word in the currently active set of workspace registers.

A workspace-register file occupies 16 contiguous memory words in the general memory area (see Figure 2). Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or

index registers. During instruction execution, the processor addresses any register in the workspace by adding the register number to the contents of the workspace pointer and initiating a memory request for the word. The relationship between the workspace pointer and its corresponding workspace is shown below.



The workspace concept is particularly valuable during operations that require a context switch, which is a change from one program environment to another (as in the case of an interrupt) or to a subroutine. Such an operation, using a conventional multi-register arrangement, requires that at least part of the contents of the register file be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the program counter, status register, and workspace pointer, the TMS 9900 accomplishes a complete context switch with only three store cycles and three fetch cycles. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use in the new routine. A corresponding time saving occurs when the original context is restored. Instructions in the TMS 9900 that result in a context switch include:

1. Branch and Load Workspace Pointer (BLWP)
2. Return from Subroutine (RTWP)
3. Extended Operation (XOP).

Device interrupts, $\overline{\text{RESET}}$, and $\overline{\text{LOAD}}$ also cause a context switch by forcing the processor to trap to a service subroutine.

2.2 INTERRUPTS

The TMS 9900 employs 16 interrupt levels with the highest priority level 0 and lowest level 15. Level 0 is reserved for the $\overline{\text{RESET}}$ function and all other levels may be used for external devices. The external levels may also be shared by several device interrupts, depending upon system requirements.

The TMS 9900 continuously compares the interrupt code (IC0 through IC3) with the interrupt mask contained in status-register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the processor recognizes the interrupt and initiates a context switch following

completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. Then, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15, respectively, of the new workspace. The TMS 9900 then forces the interrupt mask to a value that is one less than the level of the interrupt being serviced, except for level-zero interrupt, which loads zero into the mask. This allows only interrupts of higher priority to interrupt a service routine. The processor also inhibits interrupts until the first instruction of the service routine has been executed to preserve program linkage should a higher priority interrupt occur. All interrupt requests should remain active until recognized by the processor in the device-service routine. The individual service routines must reset the interrupt requests before the routine is complete.

If a higher priority interrupt occurs, a second context switch occurs to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower-priority interrupt. All interrupt subroutines should terminate with the return instruction to restore original program parameters. The interrupt-vector locations, device assignment, enabling-mask value, and the interrupt code are shown in Table 1.

TABLE 1
INTERRUPT LEVEL DATA

Interrupt Level	Vector Location (Memory Address In Hex)	Device Assignment	Interrupt Mask Values To Enable Respective Interrupts (ST12 thru ST15)	Interrupt Codes IC0 thru IC3
(Highest priority) 0	00	Reset	0 through F*	0000
1	04	External device	1 through F	0001
2	08	↓	2 through F	0010
3	0C	↓	3 through F	0011
4	10	↓	4 through F	0100
5	14	↓	5 through F	0101
6	18	↓	6 through F	0110
7	1C	↓	7 through F	0111
8	20	↓	8 through F	1000
9	24	↓	9 through F	1001
10	28	↓	A through F	1010
11	2C	↓	B through F	1011
12	30	↓	C through F	1100
13	34	↓	D through F	1101
14	38	↓	E and F	1110
(Lowest priority) 15	3C	External device	F only	1111

*Level 0 can not be disabled.

The TMS 9900 interrupt interface utilizes standard TTL components as shown in Figure 3. Note that for eight or less external interrupts a single SN74148 is required and for one external interrupt $\overline{\text{INTREQ}}$ is used as the interrupt signal with a hard-wired code IC0 through IC3.

2.3 INPUT/OUTPUT

The TMS 9900 utilizes a versatile direct command-driven I/O interface designated as the communications-register unit (CRU). The CRU provides up to 4096 directly addressable input bits and 4096 directly addressable output bits. Both input and output bits can be addressed individually or in fields of from 1 to 16 bits. The TMS 9900 employs three dedicated I/O pins (CRUIN, CRUOUT, and CRUCLK) and 12 bits (A3 through A14) of the address bus to interface with the CRU system. The processor instructions that drive the CRU interface can set, reset, or test any bit in the CRU array or move between memory and CRU data fields.

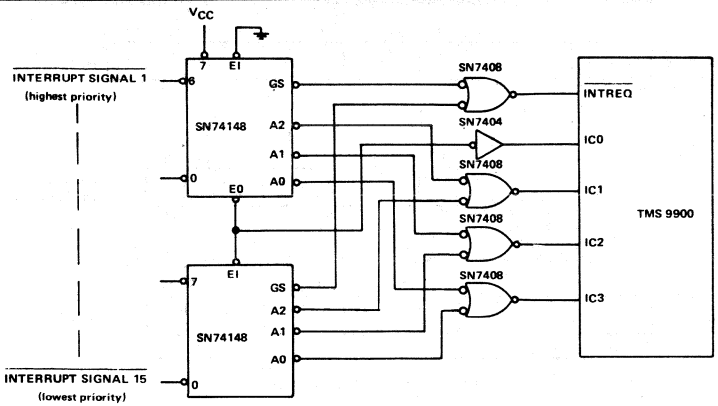


FIGURE 3 – TMS 9900 INTERRUPT INTERFACE

2.4 SINGLE-BIT CRU OPERATIONS

The TMS 9900 performs three single-bit CRU functions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the TMS 9900 develops a CRU-bit address and places it on the address bus, A3 to A14.

For the two output operations (SBO and SBZ), the processor also generates a CRUCLK pulse, indicating an output operation to the CRU device, and places bit 7 of the instruction word on the CRUOUT line to accomplish the specified operation (bit 7 is a one for SBO and a zero for SBZ). A test-bit instruction transfers the addressed CRU bit from the CRUIN input line to bit 2 of the status register (EQUAL).

The TMS 9900 develops a CRU-bit address for the single-bit operations from the CRU-base address contained in workspace register 12 and the signed displacement count contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from W12 is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 4 illustrates the development of a single-bit CRU address.

2.5 MULTIPLE-BIT CRU OPERATIONS

The TMS 9900 performs two multiple-bit CRU operations: store communications register (STCR) and load communications register (LDCR). Both operations perform a data transfer from the CRU-to-memory or from memory-to-CRU as illustrated in Figure 5. Although the figure illustrates a full 16-bit transfer operation, any number of bits from 1 through 16 may be involved. The LDCR instruction fetches a word from memory and right-shifts it to serially transfer it to CRU output bits. If the LDCR involves eight or fewer bits, those bits come from the right-justified field within the addressed byte of the memory word. If the LDCR involves nine or more bits, those bits come from the right-justified field within the whole memory word. When transferred to the CRU interface, each successive bit receives an address that is sequentially greater than the address for the previous bit. This addressing mechanism results in an order reversal of the bits; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressed bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

An STCR instruction transfers data from the CRU to memory. If the operation involves a byte or less transfer, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves from nine to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to zero.

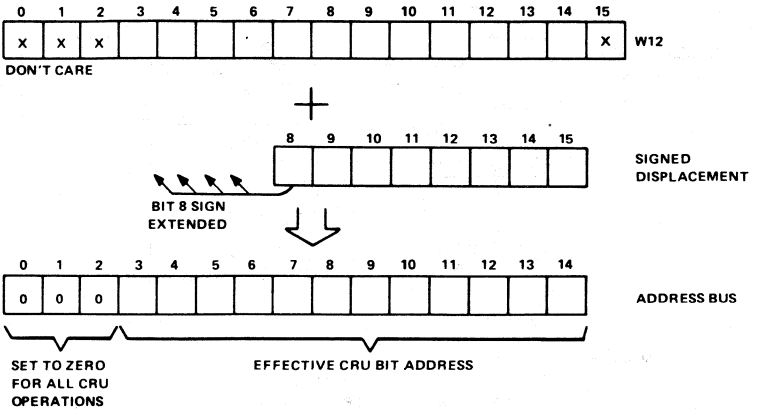


FIGURE 4 – TMS 9900 SINGLE-BIT CRU ADDRESS DEVELOPMENT

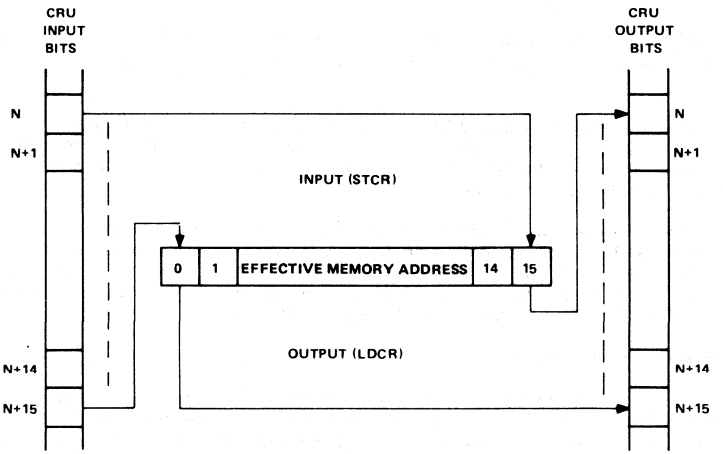


FIGURE 5 – TMS 9900 LDCR/STCR DATA TRANSFERS

When the input from the CRU device is complete, the first bit from the CRU is the least-significant-bit position in the memory word or byte.

Figure 6 illustrates how to implement a 16-bit input and a 16-bit output register in the CRU interface. CRU addresses are decoded as needed to implement up to 256 such 16-bit interface registers. In system application, however, only the exact number of interface bits needed to interface specific peripheral devices are implemented. It is not necessary to have a 16-bit interface register to interface an 8-bit device.

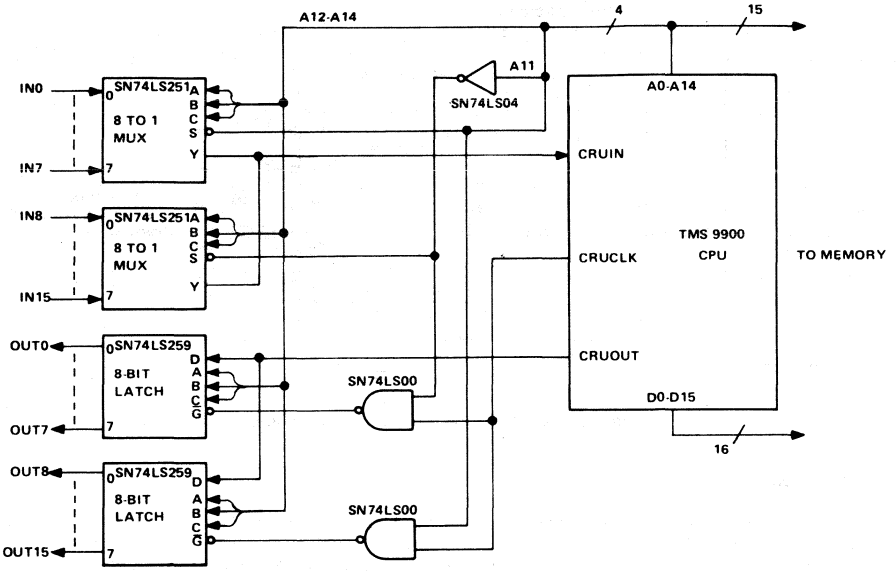


FIGURE 6 – TMS 9900 16-BIT INPUT/OUTPUT INTERFACE

2.6 EXTERNAL INSTRUCTIONS

The TMS 9900 has five external instructions that allow user-defined external functions to be initiated under program control. These instructions are CKON, CKOF, RSET, IDLE, and LREX. These mnemonics, except for IDLE, relate to functions implemented in the 990 minicomputer and do not restrict use of the instructions to initiate various user-defined functions. IDLE also causes the TMS 9900 to enter the idle state and remain until an interrupt, $\overline{\text{RESET}}$, or $\overline{\text{LOAD}}$ occurs. When any of these five instructions are executed by the TMS 9900, a unique 3-bit code appears on the most-significant 3 bits of the address bus (A0 through A2) along with a CRUCLK pulse. When the TMS 9900 is in an idle state, the 3-bit code and CRUCLK pulses occur repeatedly until the idle state is terminated. The codes are:

EXTERNAL INSTRUCTION	A0	A1	A2
LREX	H	H	H
CKOF	H	H	L
CKON	H	L	H
RSET	L	H	H
IDLE	L	H	L

Figure 7 illustrates typical external decode logic to implement these instructions. Note that a signal is generated to inhibit CRU decodes during external instructions.

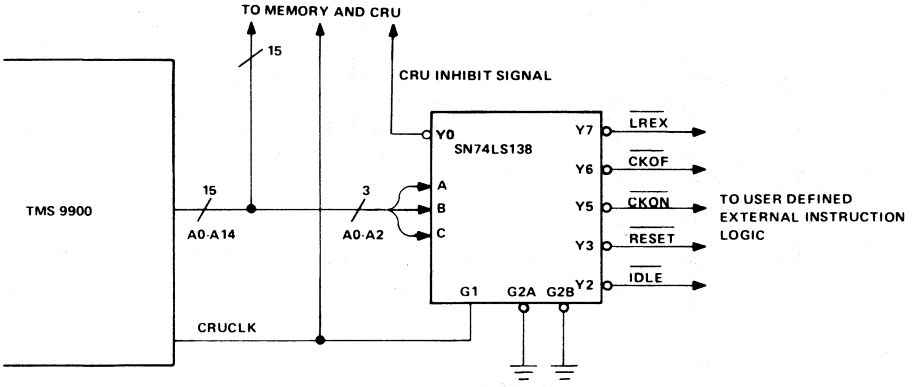
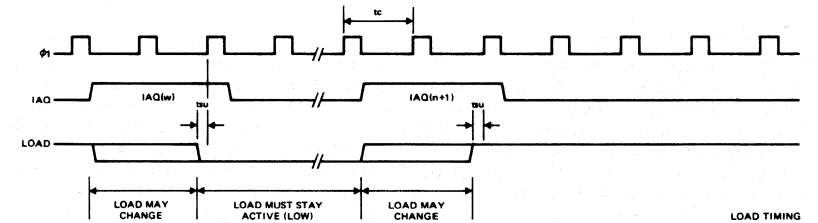
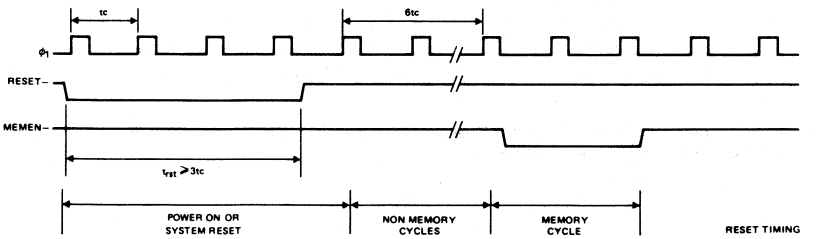


FIGURE 7 – EXTERNAL INSTRUCTION DECODE LOGIC

2.7 LOAD FUNCTION

The $\overline{\text{LOAD}}$ signal allows cold-start ROM loaders and front panels to be implemented for the TMS 9900. When active, $\overline{\text{LOAD}}$ causes the TMS 9900 to initiate an interrupt sequence immediately following the instruction being executed. Memory location FFFC is used to obtain the vector (WP and PC). The old PC, WP and ST are loaded into the new workspace and the interrupt mask is set to 0000. Then, program execution resumes using the new PC and WP.





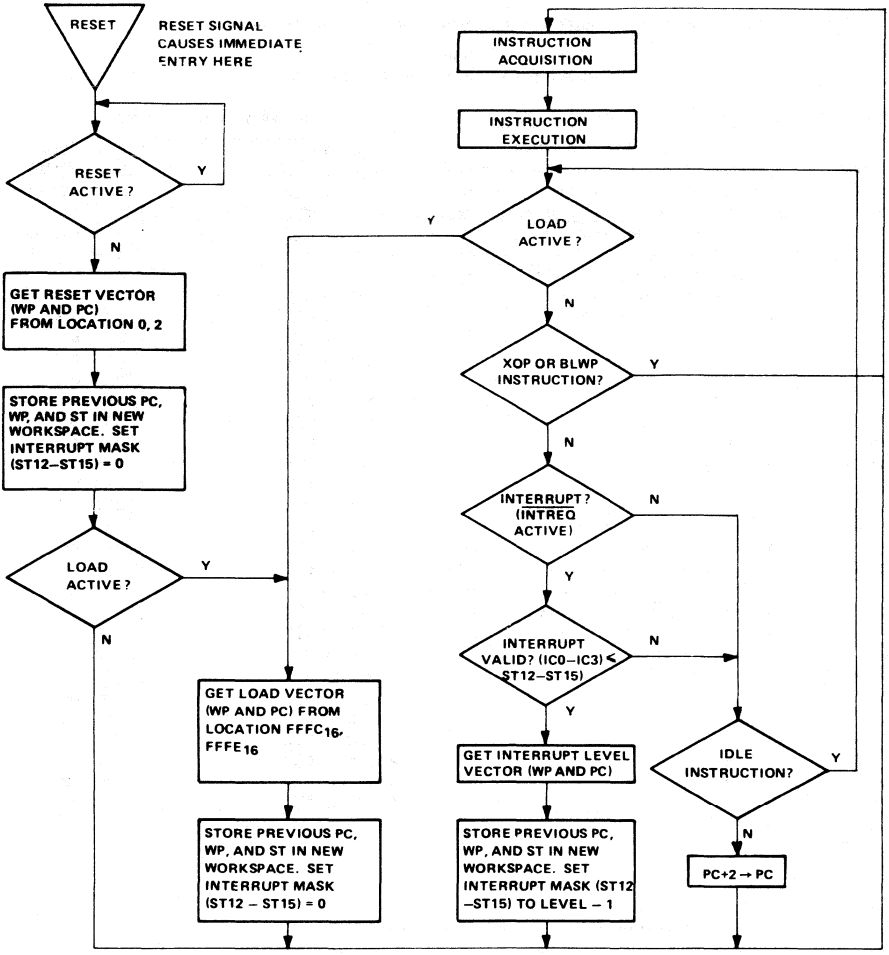


FIGURE 8 – TMS 9900 CPU FLOW CHART

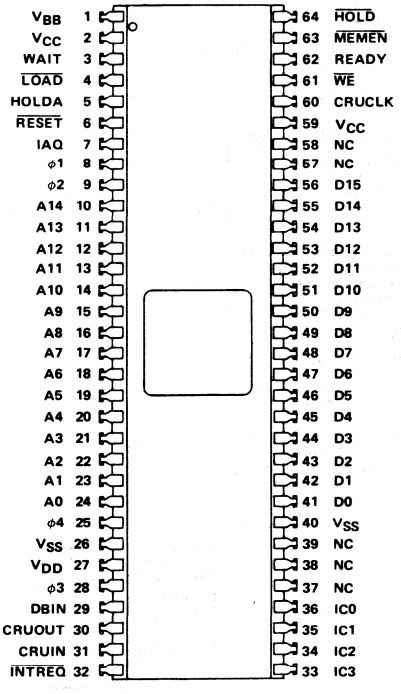
2.8 TMS 9900 PIN DESCRIPTION

Table 2 defines the TMS 9900 pin assignments and describes the function of each pin.

TABLE 2
TMS 9900 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
			ADDRESS BUS
A0 (MSB)	24	OUT	A0 through A14 comprise the address bus.
A1	23	OUT	This 3-state bus provides the memory-
A2	22	OUT	address vector to the external-memory
A3	21	OUT	system when MEMEN is active and I/O-bit
A4	20	OUT	addresses and external-instruction addresses
A5	19	OUT	to the I/O system when MEMEN is inactive.
A6	18	OUT	The address bus assumes the high-impedance
A7	17	OUT	state when HOLDA is active.
A8	16	OUT	
A9	15	OUT	
A10	14	OUT	
A11	13	OUT	
A12	12	OUT	
A13	11	OUT	
A14 (LSB)	10	OUT	
			DATA BUS
D0 (MSB)	41	I/O	D0 through D15 comprise the bidirectional
D1	42	I/O	3-state data bus. This bus transfers memory
D2	43	I/O	data to (when writing) and from (when
D3	44	I/O	reading) the external-memory system when
D4	45	I/O	MEMEN is active. The data bus assumes the
D5	46	I/O	high-impedance state when HOLDA is
D6	47	I/O	active.
D7	48	I/O	
D8	49	I/O	
D9	50	I/O	
D10	51	I/O	
D11	52	I/O	
D12	53	I/O	
D13	54	I/O	
D14	55	I/O	
D15 (LSB)	56	I/O	
			POWER SUPPLIES
V_{BB}	1		Supply voltage (–5 V NOM)
V_{CC}	2,59		Supply voltage (5 V NOM). Pins 2 and 59 must be connected in parallel.
V_{DD}	27		Supply voltage (12 V NOM)
V_{SS}	26,40		Ground reference. Pins 26 and 40 must be connected in parallel.
			CLOCKS
$\phi1$	8	IN	Phase-1 clock
$\phi2$	9	IN	Phase-2 clock
$\phi3$	28	IN	Phase-3 clock
$\phi4$	25	IN	Phase-4 clock

TMS 9900 PIN ASSIGNMENTS



NC – No internal connection

TABLE 2 (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
			BUS CONTROL
DBIN	29	OUT	Data bus in. When active (high), DBIN indicates that the TMS 9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during MEMEN. DBIN remains low in all other cases except when HOLDA is active.
MEMEN	63	OUT	Memory enable. When active (low), MEMEN indicates that the address bus contains a memory address.
WE	61	OUT	Write enable. When active (low), WE indicates that memory-write data is available from the TMS 9900 to be written into memory.
CRUCLK	60	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0 through A2.
CRUIN	31	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU data out. Serial I/O data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT should be sampled by external I/O interface logic when CRUCLK goes active (high).
			INTERRUPT CONTROL
INTREQ	32	IN	Interrupt request. When active (low), INTREQ indicates that an external interrupt is requested. If INTREQ is active, the processor loads the data on the interrupt-code-input lines IC0 through IC3 into the internal interrupt-code-storage register. The code is compared to the interrupt mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15) the TMS 9900 interrupt sequence is initiated. If the comparison fails, the processor ignores the request. INTREQ should remain active and the processor will continue to sample IC0 through IC3 until the program enables a sufficiently low priority to accept the request interrupt.
IC0 (MSB)	36	IN	Interrupt codes. IC0 is the MSB of the interrupt code, which is sampled when INTREQ is active. When IC0 through IC3 are LLLH, the highest external-priority interrupt is being requested and when HHHH, the lowest-priority interrupt is being requested.
IC1	35	IN	
IC2	34	IN	
IC3 (LSB)	33	IN	
			MEMORY CONTROL
HOLD	64	IN	Hold. When active (low), HOLD indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The TMS 9900 enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with WE, MEMEN, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When HOLD is removed, the processor returns to normal operation.
HOLDA	5	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs (WE, MEMEN, and DBIN) are in the high-impedance state.
READY	62	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the TMS 9900 enters a wait state and suspends internal operation until the memory systems indicate ready.
WAIT	3	OUT	Wait. When active (high), WAIT indicates that the TMS 9900 has entered a wait state because of a not-ready condition from memory.

*If the cycle following the present memory cycle is also a memory cycle, it, too, is completed before the TMS9900 enters the hold state. The maximum number of consecutive memory cycles is two.

TABLE 2 (CONCLUDED)

SIGNATURE	PIN	I/O	DESCRIPTION
			TIMING AND CONTROL
IAQ	7	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the TMS 9900 is acquiring an instruction. IAQ can be used to detect illegal op codes.
$\overline{\text{LOAD}}$	4	IN	Load. When active (low), $\overline{\text{LOAD}}$ causes the TMS 9900 to execute a nonmaskable interrupt with memory address $FFFC_{16}$ containing the trap vector (WP and PC). The load sequence begins after the instruction being executed is completed. $\overline{\text{LOAD}}$ will also terminate an idle state. If $\overline{\text{LOAD}}$ is active during the time $\overline{\text{RESET}}$ is released, then the $\overline{\text{LOAD}}$ trap will occur after the $\overline{\text{RESET}}$ function is completed. $\overline{\text{LOAD}}$ should remain active for one instruction period. IAQ can be used to determine instruction boundaries. This signal can be used to implement cold-start ROM loaders. Additionally, front-panel routines can be implemented using CRU bits as front-panel-interface signals and software-control routines to control the panel operations.
$\overline{\text{RESET}}$	6	IN	Reset. When active (low), $\overline{\text{RESET}}$ causes the processor to be reset and inhibits $\overline{\text{WE}}$ and CRUCLK. When $\overline{\text{RESET}}$ is released, the TMS 9900 then initiates a level-zero interrupt sequence that acquires WP and PC from locations 0000 and 0002, sets all status register bits to zero, and starts execution. $\overline{\text{RESET}}$ will also terminate an idle state. $\overline{\text{RESET}}$ must be held active for a minimum of three clock cycles.

2.9 TIMING

2.9.1 MEMORY

A basic memory read and write cycle is shown in Figure 9. The read cycle is shown with no wait states and the write cycle is shown with one wait state.

$\overline{\text{MEMEN}}$ goes active (low) during each memory cycle. At the same time that $\overline{\text{MEMEN}}$ is active, the memory address appears on the address bus bits A0 through A14. If the cycle is a memory-read cycle, DBIN will go active (high) at the same time $\overline{\text{MEMEN}}$ and A0 through A14 become valid. The memory-write signal $\overline{\text{WE}}$ will remain inactive (high) during a read cycle. If the read cycle is also an instruction acquisition cycle, IAQ will go active (high) during the cycle.

The READY signal, which allows extended memory cycles, is shown high during $\phi 1$ of the second clock cycle of the read operation. This indicates to the TMS 9900 that memory-read data will be valid during $\phi 1$ of the next clock cycle. If READY is low during $\phi 1$, then the TMS 9900 enters a wait state suspending internal operation until a READY is sensed during a subsequent $\phi 1$. The memory read data is then sampled by the TMS 9900 during the next $\phi 1$, which completes the memory-read cycle.

At the end of the read cycle, $\overline{\text{MEMEN}}$ and DBIN go inactive (high and low, respectively). The address bus may also change at this time, however, the data bus remains in the input mode for one clock cycle after the read cycle.

A write cycle is similar to the read cycle with the exception that $\overline{\text{WE}}$ goes active (low) as shown and valid write data appears on the data bus at the same time the address appears. The write cycle is shown as an example of a one-wait-state memory cycle. READY is low during $\phi 1$ resulting in the WAIT signal shown.

2.9.2 HOLD

Other interfaces may utilize the TMS 9900 memory bus by using the hold operation (illustrated in Figure 10) of the TMS 9900. When $\overline{\text{HOLD}}$ is active (low), the TMS 9900 enters the hold state at the next available non-memory cycle. Considering that there can be a maximum of two consecutive memory cycles, the maximum delay between $\overline{\text{HOLD}}$ going active to HOLDA going active (high) could be $t_{c(\phi)}$ (for setup) + (4+W) $t_{c(\phi)}$ + $t_{c(\phi)}$ (delay for HOLDA), where W is the number of wait states per memory cycle and $t_{c(\phi)}$ is the clock cycle time. When the TMS 9900 has entered the hold state, HOLDA goes active (high) and A0 through A15, D0 through D15 DBIN, $\overline{\text{MEMEN}}$, and $\overline{\text{WE}}$ go into a high-impedance state to allow other devices to use the memory buses. When $\overline{\text{HOLD}}$ goes inactive (high), the TMS 9900 resumes processing as shown. If hold occurs during a CRU operation, the TMS 9900 uses an extra clock cycle (after the removal of the $\overline{\text{HOLD}}$ signal) to reassert the CRU address providing the normal setup times for the CRU bit transfer that was interrupted.

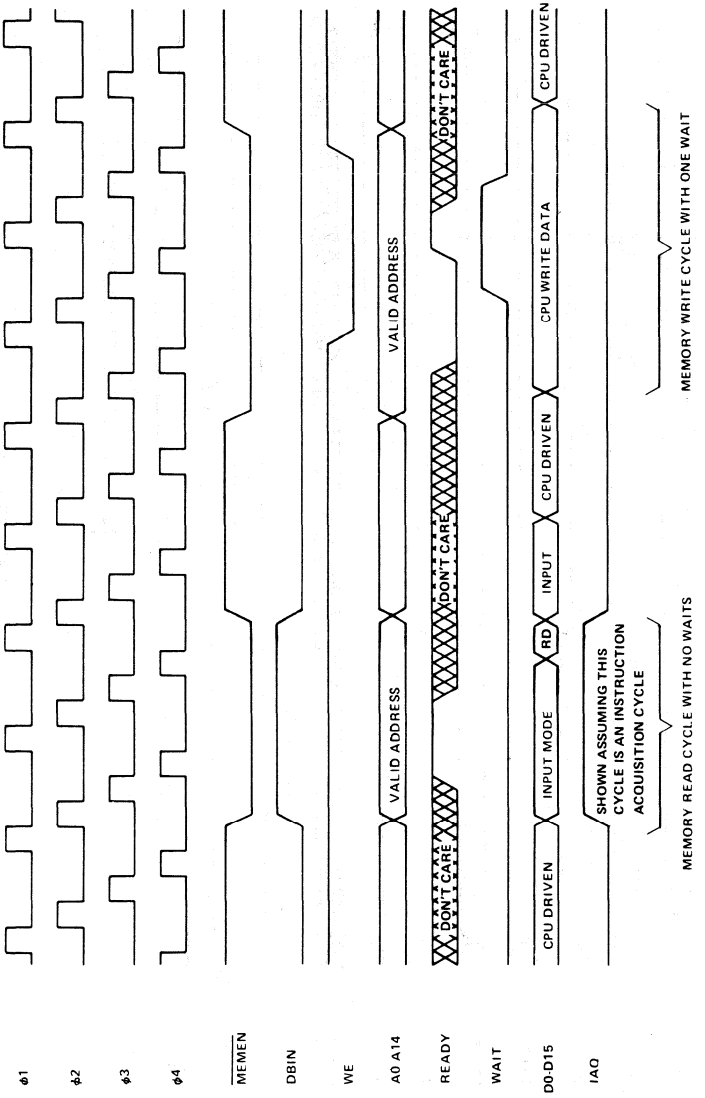


FIGURE 9 – TMS 9900 MEMORY BUS TIMING

6

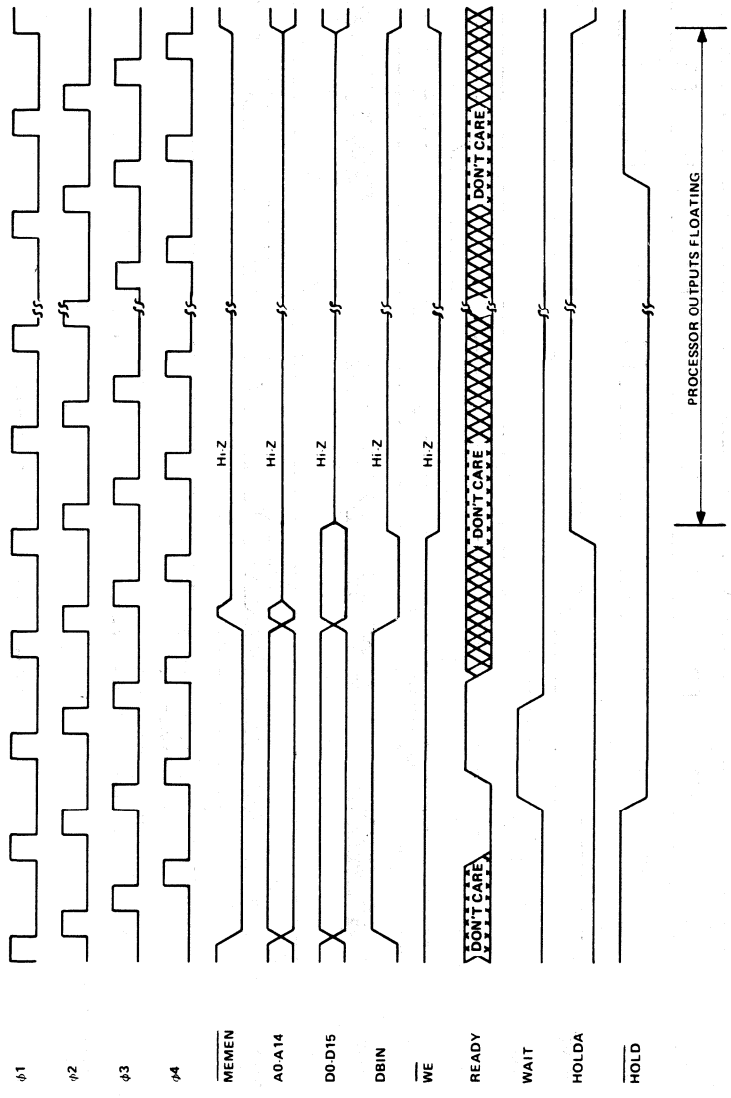


FIGURE 10 – TMS 9900 HOLD TIMING

2.9.3 CRU

CRU interface timing is shown in Figure 11. The timing for transferring two bits out and one bit in is shown. These transfers would occur during the execution of a CRU instruction. The other cycles of the instruction execution are not illustrated. To output a CRU bit, the CRU-bit address is placed on the address bus A0 through A14 and the actual bit data on CRUOUT. During the second clock cycle a CRU pulse is supplied by CRUCLK. This process is repeated until the number of bits specified by the instruction are completed.

The CRU input operation is similar in that the bit address appears on A0 through A14. During the subsequent cycle the TMS 9900 accepts the bit input data as shown. No CRUCLK pulses occur during a CRU input operation.

3. TMS 9900 INSTRUCTION SET

3.1 DEFINITION

Each TMS 9900 instruction performs one of the following operations:

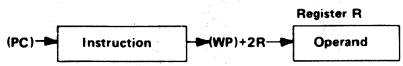
- Arithmetic, logical, comparison, or manipulation operations on data
- Loading or storage of internal registers (program counter, workspace pointer, or status)
- Data transfer between memory and external devices via the CRU
- Control functions.

3.2 ADDRESSING MODES

TMS 9900 instructions contain a variety of available modes for addressing random-memory data (e.g., program parameters and flags), or formatted memory data (character strings, data lists, etc.). The following figures graphically describe the derivation of the effective address for each addressing mode. The applicability of addressing modes to particular instructions is described in Section 3.5 along with the description of the operations performed by the instruction. The symbols following the names of the addressing modes [R, *R, *R+, @ LABEL, or @ TABLE (R)] are the general forms used by TMS 9900 assemblers to select the addressing mode for register R.

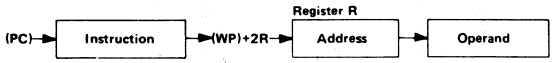
3.2.1 WORKSPACE REGISTER ADDRESSING R

Workspace Register R contains the operand.



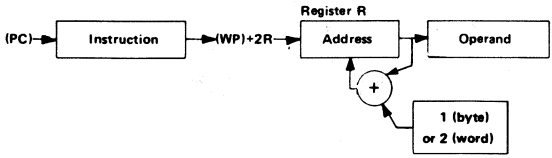
3.2.2 WORKSPACE REGISTER INDIRECT ADDRESSING *R

Workspace Register R contains the address of the operand.



3.2.3 WORKSPACE REGISTER INDIRECT AUTO INCREMENT ADDRESSING *R+

Workspace Register R contains the address of the operand. After acquiring the operand, the contents of workspace register R are incremented.



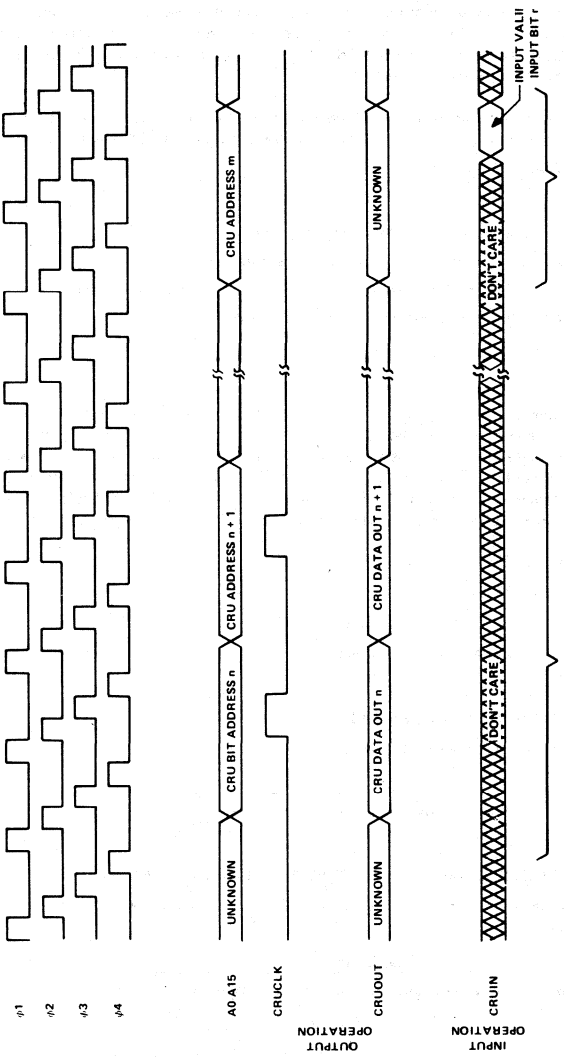
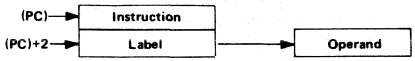


FIGURE 11 – TMS 9900 CRU INTERFACE TIMING

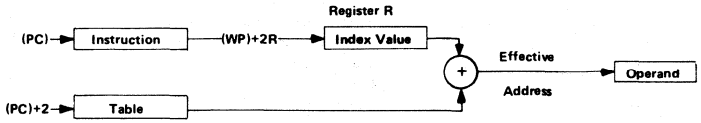
3.2.4 SYMBOLIC (DIRECT) ADDRESSING @ LABEL

The word following the instruction contains the address of the operand.



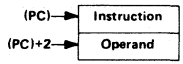
3.2.5 INDEXED ADDRESSING @ TABLE (R)

The word following the instruction contains the base address. Workspace register R contains the index value. The sum of the base address and the index value results in the effective address of the operand.



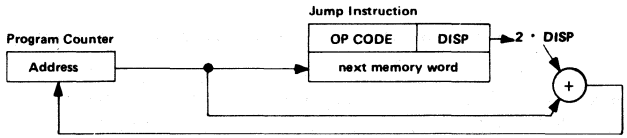
3.2.6 IMMEDIATE ADDRESSING

The word following the instruction contains the operand.



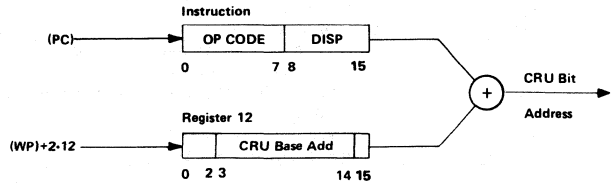
3.2.7 PROGRAM COUNTER RELATIVE ADDRESSING

The 8-bit signed displacement in the right byte (bits 8 through 15) of the instruction is multiplied by 2 and added to the updated contents of the program counter. The result is placed in the PC.



3.2.8 CRU RELATIVE ADDRESSING

The 8-bit signed displacement in the right byte of the instruction is added to the CRU base address (bits 3 through 14 of the workspace register 12). The result is the CRU address of the selected CRU bit.



3.3 TERMS AND DEFINITIONS

The following terms are used in describing the instructions of the TMS 9900:

TERM	DEFINITION
B	Byte indicator (1=byte, 0 = word)
C	Bit count
D	Destination address register
DA	Destination address
IOP	Immediate operand
LSB(n)	Least significant (right most) bit of (n)
MSB(n)	Most significant (left most) bit of (n)
N	Don't care
PC	Program counter
Result	Result of operation performed by instruction
S	Source address register
SA	Source address
ST	Status register
STn	Bit n of status register
T_D	Destination address modifier
T_S	Source address modifier
W	Workspace register
WRn	Workspace register n
(n)	Contents of n
a→b	a is transferred to b
|n|	Absolute value of n
+	Arithmetic addition
–	Arithmetic subtraction
AND	Logical AND
OR	Logical OR
⊕	Logical exclusive OR
$\overline{n}$	Logical complement of n

3.4 STATUS REGISTER

The status register contains the interrupt mask level and information pertaining to the instruction operation.

0	1	2	3	4	5	6	7 8 9 10 11	12 13 14 15
ST0	ST1	ST2	ST3	ST4	ST5	ST6	not used (=0)	ST12 ST13 ST14 ST15
L>	A>	=	C	O	P	X		Interrupt Mask

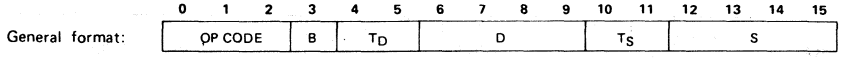
BIT	NAME	INSTRUCTION	CONDITION TO SET BIT TO 1
ST0	LOGICAL GREATER THAN	C,CB	If MSB(SA) = 1 and MSB(DA) = 0, or if MSB(SA) = MSB(DA) and MSB of (DA) – (SA) = 1
		CI	If MSB(W) = 1 and MSB of IOP = 0, or if MSB(W) = MSB of IOP and MSB of IOP – (W) = 1
		ABS	If (SA) ≠ 0
		All Others	If result ≠ 0
ST1	ARITHMETIC GREATER THAN	C,CB	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB(DA) – (SA) = 1
		CI	If MSB(W) = 0 and MSB of IOP = 1, or if MSB(W) = MSB of IOP and MSB of IOP – (W) = 1
		ABS	If MSB(SA) = 0 and (SA) ≠ 0
		All Others	If MSB of result = 0 and result ≠ 0

– Continued

BIT	NAME	INSTRUCTION	CONDITION TO SET BIT TO 1
ST2	EQUAL	C, CB	If (SA) = (DA)
		C1	If (W) = IOP
		COC	If (SA) and $\overline{(DA)}$ = 0
		CZC	If (SA) and (DA) = 0
		TB	If CRUIN = 1
		ABS	If (SA) = 0
		All others	If result = 0
ST3	CARRY	A, AB, ABS, AI, DEC, DECT, INC, INCT, NEG, S, SB	If CARRY OUT = 1
		SLA, SRA, SRC, SRL	If last bit shifted out = 1
ST4	OVERFLOW	A, AB	If MSB(SA) = MSB(DA) and MSB of result ≠ MSB(DA)
		AI	If MSB(W) = MSB of IOP and MSB of result ≠ MSB(W)
		S, SB	If MSB(SA) ≠ MSB(DA) and MSB of result ≠ MSB(DA)
		DEC, DECT	If MSB(SA) = 1 and MSB of result = 0
		INC, INCT	If MSB(SA) = 0 and MSB of result = 1
		SLA	If MSB changes during shift
		DIV	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of (DA) − (SA) = 0
		ABS, NEG	If (SA) = 8000_{16}
ST5	PARITY	CB, MOVB	If (SA) has odd number of 1's
		LDCR, STCR	If 1 ≤ C ≤ 8 and (SA) has odd number of 1's
		AB, SB, SOCB, SZCB	If result has odd number of 1's
ST6	XOP	XOP	If XOP instruction is executed
ST12–ST15	INTERRUPT MASK	LIMI	If corresponding bit of IOP is 1
		RTWP	If corresponding bit of WR15 is 1

3.5 INSTRUCTIONS

3.5.1 Dual Operand Instructions with Multiple Addressing Modes for Source and Destination Operand



If B = 1 the operands are bytes and the operand addresses are byte addresses. If B = 0 the operands are words and the operand addresses are word addresses.

The addressing mode for each operand is determined by the T field of that operand.

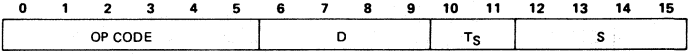
T_S OR T_D	S OR D	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	1
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	4
10	1, 2, . . . 15	Indexed	2,4
11	0, 1, . . . 15	Workspace register indirect auto-increment	3

NOTES: 1. When a workspace register is the operand of a byte instruction (bit 3 = 1), the left byte (bits 0 through 7) is the operand and the right byte (bits 8 through 15) is unchanged.
2. Workspace register 0 may not be used for indexing.
3. The workspace register is incremented by 1 for byte instructions (bit 3 = 1) and is incremented by 2 for word instructions (bit 3 = 0).
4. When $T_S = T_D = 10$, two words are required in addition to the instruction word. The first word is the source operand base address and the second word is the destination operand base address.

MNEMONIC	OP CODE 0 1 2	B 3	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
A	1 0 1	0	Add	Yes	0-4	(SA)+(DA) → (DA)
AB	1 0 1	1	Add bytes	Yes	0-5	(SA)+(DA) → (DA)
C	1 0 0	0	Compare	No	0-2	Compare (SA) to (DA) and set appropriate status bits
CB	1 0 0	1	Compare bytes	No	0-2,5	Compare (SA) to (DA) and set appropriate status bits
S	0 1 1	0	Subtract	Yes	0-4	(DA) – (SA) → (DA)
SB	0 1 1	1	Subtract bytes	Yes	0-5	(DA) – (SA) → (DA)
SOC	1 1 1	0	Set ones corresponding	Yes	0-2	(DA) OR (SA) → (DA)
SOCB	1 1 1	1	Set ones corresponding bytes	Yes	0-2,5	(DA) OR (SA) → (DA)
SZC	0 1 0	0	Set zeroes corresponding	Yes	0-2	(DA) AND ($\overline{SA}$) → (DA)
SZCB	0 1 0	1	Set zeroes corresponding bytes	Yes	0-2,5	(DA) AND ($\overline{SA}$) → (DA)
MOV	1 1 0	0	Move	Yes	0-2	(SA) → (DA)
MOVB	1 1 0	1	Move bytes	Yes	0-2,5	(SA) → (DA)

3.5.2 Dual Operand Instructions with Multiple Addressing Modes for the Source Operand and Workspace Register Addressing for the Destination

General format:



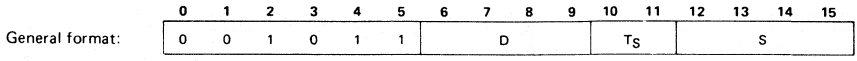
The addressing mode for the source operand is determined by the T_S field.

T_S	S	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	
10	1, 2, . . . 15	Indexed	1
11	0, 1, . . . 15	Workspace register indirect auto increment	2

NOTES: 1. Workspace register 0 may not be used for indexing.
2. The workspace register is incremented by 2.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
COC	0 0 1 0 0 0	Compare ones corresponding	No	2	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set ST2.
CZC	0 0 1 0 0 1	Compare zeros corresponding	No	2	Test (D) to determine if 0's are in each bit position where 1's are in (SA). If so, set ST2.
XOR	0 0 1 0 1 0	Exclusive OR	Yes	0-2	(D) ⊕ (SA) → (D)
MPY	0 0 1 1 1 0	Multiply	No		Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D+1 (least significant). If WR15 is D, the next word in memory after WR15 will be used for the least significant half of the product.
DIV	0 0 1 1 1 1	Divide	No	4	If unsigned (SA) is less than or equal to unsigned (D), perform no operation and set ST4. Otherwise, divide unsigned (D) and (D+1) by unsigned (SA). Quotient → (D), remainder → (D+1). If D = 15, the next word in memory after WR 15 will be used for the remainder.

3.5.3 Extended Operation (XOP) Instruction

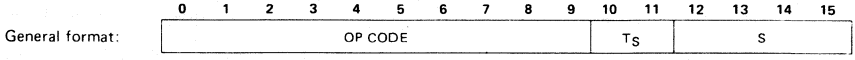


The T_S and S fields provide multiple mode addressing capability for the source operand. When the XOP is executed, ST6 is set and the following transfers occur:

$(40_{16} + 4D) \rightarrow (WP)$
$(42_{16} + 4D) \rightarrow (PC)$
SA → (new WR11)
(old WP) → (new WR13)
(old PC) → (new WR14)
(old ST) → (new WR15)

The TMS 9900 does not test interrupt requests ($\overline{INTREQ}$) upon completion of the XOP instruction.

3.5.4 Single Operand Instructions



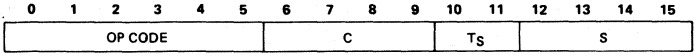
The T_S and S fields provide multiple mode addressing capability for the source operand.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
B	0 0 0 0 0 1 0 0 0 1	Branch	No	–	SA → (PC)
BL	0 0 0 0 0 1 1 0 1 0	Branch and link	No	–	(PC) → (WR11); SA → (PC)
BLWP	0 0 0 0 0 1 0 0 0 0	Branch and load workspace pointer	No	–	(SA) → (WP);(SA+1) → (PC); (old WP) → (new WR13); (old PC) → (new WR14); (old ST) → (new WR15); the interrupt input ($\overline{INTREQ}$) is not tested upon completion of the BLWP instruction.
CLR	0 0 0 0 0 1 0 0 1 1	Clear operand	No	–	0 → (SA)
SETO	0 0 0 0 0 1 1 1 0 0	Set to ones	No	–	$FFFF_{16}$ → (SA)
INV	0 0 0 0 0 1 0 1 0 1	Invert	Yes	0-2	$\overline{(SA)}$ → (SA)
NEG	0 0 0 0 0 1 0 1 0 0	Negate	Yes	0-4	–(SA) → (SA)
ABS	0 0 0 0 0 1 1 1 0 1	Absolute value*	No	0-4	|(SA)| → (SA)
SWPB	0 0 0 0 0 1 1 0 1 1	Swap bytes	No	–	(SA), bits 0 thru 7 → (SA), bits 8 thru 15; (SA), bits 8 thru 15 → (SA), bits 0 thru 7.
INC	0 0 0 0 0 1 0 1 1 0	Increment	Yes	0-4	(SA) + 1 → (SA)
INCT	0 0 0 0 0 1 0 1 1 1	Increment by two	Yes	0-4	(SA) + 2 → (SA)
DEC	0 0 0 0 0 1 1 0 0 0	Decrement	Yes	0-4	(SA) – 1 → (SA)
DECT	0 0 0 0 0 1 1 0 0 1	Decrement by two	Yes	0-4	(SA) – 2 → (SA)
X†	0 0 0 0 0 1 0 0 1 0	Execute	No	–	Execute the instruction at SA.

* Operand is compared to zero for status bit.
† If additional memory words for the execute instruction are required to define the operands of the instruction located at SA, these words will be accessed from PC and the PC will be updated accordingly. The instruction acquisition signal (IAQ) will not be true when the TMS 9900 accesses the instruction at SA. Status bits are affected in the normal manner for the instruction executed.

3.5.5 CRU Multiple-Bit Instructions

General format:



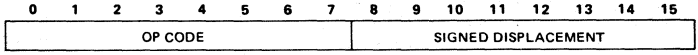
The C field specifies the number of bits to be transferred. If C = 0, 16 bits will be transferred. The CRU base register (WR12, bits 3 through 14) defines the starting CRU bit address. The bits are transferred serially and the CRU address is incremented with each bit transfer, although the contents of WR12 is not affected. T_S and S provide multiple mode addressing capability for the source operand. If 8 or fewer bits are transferred (C = 1 through 8), the source address is a byte address. If 9 or more bits are transferred (C = 0, 9 through 15), the source address is a word address. If the source is addressed in the workspace register indirect auto increment mode, the workspace register is incremented by 1 if C = 1 through 8, and is incremented by 2 otherwise.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
LDCR	0 0 1 1 0 0	Load communcation register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from (SA) to the CRU.
STCR	0 0 1 1 0 1	Store communcation register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from the CRU to (SA). Load unfilled bit positions with 0.

†ST5 is affected only if $1 \leq C \leq 8$.

3.5.6 CRU Single-Bit Instructions

General format:

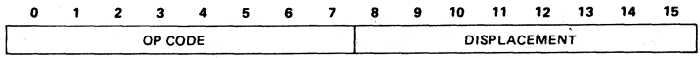


CRU relative addressing is used to address the selected CRU bit.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	STATUS BITS AFFECTED	DESCRIPTION
SBO	0 0 0 1 1 1 0 1	Set bit to one	–	Set the selected CRU output bit to 1.
SBZ	0 0 0 1 1 1 1 0	Set bit to zero	–	Set the selected CRU output bit to 0.
TB	0 0 0 1 1 1 1 1	Test bit	2	If the selected CRU input bit = 1, set ST2.

3.5.7 Jump Instructions

General format:

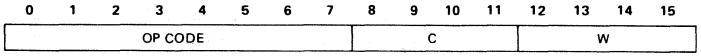


Jump instructions cause the PC to be loaded with the value selected by PC relative addressing if the bits of ST are at specified values. Otherwise, no operation occurs and the next instruction is executed since PC points to the next instruction. The displacement field is a word count to be added to PC. Thus, the jump instruction has a range of –128 to 127 words from memory-word address following the jump instruction. No ST bits are affected by jump instruction.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	ST CONDITION TO LOAD PC
JEQ	0 0 0 1 0 0 1 1	Jump equal	ST2 = 1
JGT	0 0 0 1 0 1 0 1	Jump greater than	ST1 = 1
JH	0 0 0 1 1 0 1 1	Jump high	ST0 = 1 and ST2 = 0
JHE	0 0 0 1 0 1 0 0	Jump high or equal	ST0 = 1 or ST2 = 1
JL	0 0 0 1 1 0 1 0	Jump low	ST0 = 0 and ST2 = 0
JLE	0 0 0 1 0 0 1 0	Jump low or equal	ST0 = 0 or ST2 = 1
JLT	0 0 0 1 0 0 0 1	Jump less than	ST1 = 0 and ST2 = 0
JMP	0 0 0 1 0 0 0 0	Jump unconditional	unconditional
JNC	0 0 0 1 0 1 1 1	Jump no carry	ST3 = 0
JNE	0 0 0 1 0 1 1 0	Jump not equal	ST2 = 0
JNO	0 0 0 1 1 0 0 1	Jump no overflow	ST4 = 0
JOC	0 0 0 1 1 0 0 0	Jump on carry	ST3 = 1
JOP	0 0 0 1 1 1 0 0	Jump odd parity	ST5 = 1

3.5.8 Shift Instructions

General format:

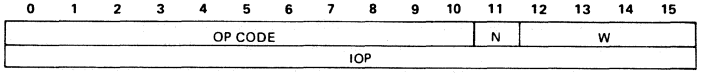


If C = 0, bits 12 through 15 of WR0 contain the shift count. If C = 0 and bits 12 through 15 of WR0 = 0, the shift count is 16.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
SLA	0 0 0 0 1 0 1 0	Shift left arithmetic	Yes	0-4	Shift (W) left. Fill vacated bit positions with 0.
SRA	0 0 0 0 1 0 0 0	Shift right arithmetic	Yes	0-3	Shift (W) right. Fill vacated bit positions with original MSB of (W).
SRC	0 0 0 0 1 0 1 1	Shift right circular	Yes	0-3	Shift (W) right. Shift previous LSB into MSB.
SRL	0 0 0 0 1 0 0 1	Shift right logical	Yes	0-3	Shift (W) right. Fill vacated bit positions with 0's.

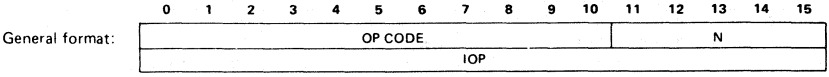
3.5.9 Immediate Register Instructions

General format:



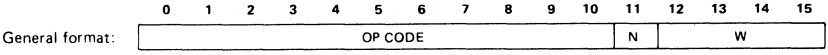
MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
AI	0 0 0 0 0 0 1 0 0 0 1	Add immediate	Yes	0-4	(W) + IOP → (W)
ANDI	0 0 0 0 0 0 1 0 0 1 0	AND immediate	Yes	0-2	(W) AND IOP → (W)
CI	0 0 0 0 0 0 1 0 1 0 0	Compare immediate	Yes	0-2	Compare (W) to IOP and set appropriate status bits
LI	0 0 0 0 0 0 1 0 0 0 0	Load immediate	Yes	0-2	IOP → (W)
ORI	0 0 0 0 0 0 1 0 0 1 1	OR immediate	Yes	0-2	(W) OR IOP → (W)

3.5.10 Internal Register Load Immediate Instructions



MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
LWPI	0 0 0 0 0 0 0 1 0 1 1 1	Load workspace pointer immediate	IOP → (WP), no ST bits affected
LIMI	0 0 0 0 0 0 0 1 1 0 0 0	Load interrupt mask	IOP, bits 12 thru 15 → ST12 thru ST15

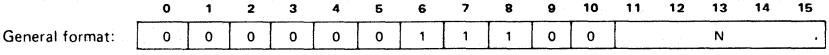
3.5.11 Internal Register Store Instructions



No ST bits are affected.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
STST	0 0 0 0 0 0 0 1 0 1 1 0	Store status register	(ST) → (W)
STWP	0 0 0 0 0 0 0 1 0 1 0 1	Store workspace pointer	(WP) → (W)

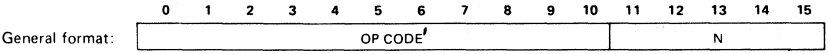
3.5.12 Return Workspace Pointer (RTWP) Instruction



The RTWP instruction causes the following transfers to occur:

(WR15) → (ST)
(WR14) → (PC)
(WR13) → (WP)

3.5.13 External Instructions



External instructions cause the three most-significant address lines (A0 through A2) to be set to the below-described levels and the CRUCLK line to be pulsed, allowing external control functions to be initiated.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	STATUS BITS AFFECTED	DESCRIPTION	ADDRESS BUS A0	A1	A2
IDLE	0 0 0 0 0 0 1 1 0 1 0	Idle	–	Suspend TMS 9900 instruction execution until an interrupt, $\overline{\text{LOAD}}$, or $\overline{\text{RESET}}$ occurs	L	H	L
RSET	0 0 0 0 0 0 1 1 0 1 1	Reset	12–15	0 → ST12 thru ST15	L	H	H
CKOF	0 0 0 0 0 0 1 1 1 1 0	User defined		---	H	H	L
CKON	0 0 0 0 0 0 1 1 1 0 1	User defined		---	H	L	H
LREX	0 0 0 0 0 0 1 1 1 1 1	User defined		---	H	H	H

3.6 TMS 9900 INSTRUCTION EXECUTION TIMES

Instruction execution times for the TMS 9900 are a function of:

1) Clock cycle time, $t_{c(\phi)}$
2) Addressing mode used where operands have multiple addressing mode capability
3) Number of wait states required per memory access.

Table 3 lists the number of clock cycles and memory accesses required to execute each TMS 9900 instruction. For instructions with multiple addressing modes for either or both operands, the table lists the number of clock cycles and memory accesses with all operands addressed in the workspace-register mode. To determine the additional number of clock cycles and memory accesses required for modified addressing, add the appropriate values from the referenced tables. The total instruction-execution time for an instruction is:

$$T = t_{c(\phi)} \quad (C + W*M)$$

where:

T = total instruction execution time;
$t_{c(\phi)}$ = clock cycle time;
C = number of clock cycles for instruction execution plus address modification;
W = number of required wait states per memory access for instruction execution plus address modification;
M = number of memory accesses.

TABLE 3
INSTRUCTION EXECUTION TIMES

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	ADDRESS MODIFICATION† DEST
A	14	4	A	A
AB	14	4	B	B
ABS (MSB = 0)	12	2	A	–
(MSB = 1)	14	3	A	–
AI	14	4	–	–
ANDI	14	4	–	–
B	8	2	A	–
BL	12	3	A	–
BLWP	26	6	A	–
C	14	3	A	A
CB	14	3	B	B
CI	14	3	–	–
CKOF	12	1	–	–
CKON	12	1	–	–
CLR	10	3	A	–
COC	14	3	A	–
CZC	14	3	A	–
DEC	10	3	A	–
DECT	10	3	A	–
DIV (ST4 is set)	16	3	A	–
DIV (ST4 is reset)*	92-124	6	A	–
IDLE	12	1	–	–
INC	10	3	A	–
INCT	10	3	A	–
INV	10	3	A	–
Jump (PC is changed)	10	1	–	–
(PC is not changed)	8	1	–	–
LDCR (C = 0)	52	3	A	–
(1< C<8)	20+2C	3	B	–
(9 < C< 15)	20+2C	3	A	–
LI	12	3	–	–
LIMI	16	2	–	–
LREX	12	1	–	–
RESET function	26	5	–	–
LOAD function	22	5	–	–
Interrupt context switch	22	5	–	–

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	ADDRESS MODIFICATION† DEST
LWPI	10	2	–	–
MOV	14	4	A	A
MOVB	14	4	B	B
MPY	52	5	A	–
NEG	12	3	A	–
ORI	14	4	–	–
RSET	12	1	–	–
RTWP	14	4	–	–
S	14	4	A	A
SB	14	4	B	B
SBO	12	2	–	–
SBZ	12	2	–	–
SETO	10	3	A	–
Shift (C≠0)	12+2C	3	–	–
(C=0, Bits 12–15 of WR0=0)	52	4	–	–
(C=0, Bits 12–15 of WR0=N≠0)	20+2N	4	–	–
SOC	14	4	A	A
SOCB	14	4	B	B
STCR (C=0).	60	4	A	–
(1<C< 7)	42	4	B	–
(C=8)	44	4	B	–
(9< C< 15)	58	4	A	–
STST	8	2	–	–
STWP	8	2	–	–
SWPB	10	3	A	–
SZC	14	4	A	A
SZCB	14	4	B	B
TB	12	2	–	–
X **	8	2	A	–
XOP	36	8	A	–
XOR	14	4	A	–
Undefined op codes 0000-01FF,0320-033F,0C00-0FFF, 0780-07FF	6	1	–	–

*Execution time is dependent upon the partial quotient after each clock cycle during execution.
**Execution time is added to the execution time of the instruction located at the source address minus 4 clock cycles and 1 memory access time.
†The letters A and B refer to the respective tables that follow.

ADDRESS MODIFICATION – TABLE A

ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	8	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D ≠ 0)	8	2

ADDRESS MODIFICATION – TABLE B

ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	6	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D ≠ 0)	8	2

As an example, the instruction MOVB is used in a system with $t_{c(\phi)} = 0.333\ \mu s$ and no wait states are required to access memory. Both operands are addressed in the workspace register mode:

$$T = t_{c(\phi)}\ (C + W \cdot M) = 0.333\ (14 + 0 \cdot 4)\ \mu s = 4.662\ \mu s.$$

If two wait states per memory access were required, the execution time is:

$$T = 0.333\ (14 + 2 \cdot 4)\ \mu s = 7.326\ \mu s.$$

If the source operand was addressed in the symbolic mode and two wait states were required:

$$T = t_{c(\phi)}\ (C + W \cdot M)$$
$$C = 14 + 8 = 22$$
$$M = 4 + 1 = 5$$
$$T = 0.333\ (22 + 2 \cdot 5)\ \mu s = 10.656\ \mu s.$$

4. TMS 9900 ELECTRICAL AND MECHANICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1) . . . . . –0.3 to 20 V
Supply voltage, V_{DD} (see Note 1) . . . . . –0.3 to 20 V
Supply voltage, V_{SS} (see Note 1) . . . . . –0.3 to 20 V
All input voltages (see Note 1) . . . . . –0.3 to 20 V
Output voltage (with respect to V_{SS}) . . . . . –2 V to 7 V
Continuous power dissipation . . . . . 1.2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the most negative supply, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this section, voltage values are with respect to V_{SS}.

4.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−5.25	−5	−4.75	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (all inputs except clocks)		2.4		V
High-level clock input voltage, $V_{IH(\phi)}$		V_{DD}		V
Low-level input voltage, V_{IL} (all inputs except clocks)		0.4		V
Low-level clock input voltage, $V_{IL(\phi)}$		0.3		V
Operating free-air temperature, T_A	0		70	°C

4.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	Data bus during DBIN	$V_I = V_{SS}$ to V_{CC}		±75		μA
		$\overline{WE}$, $\overline{MEMEN}$, DBIN during HOLDA	$V_I = V_{SS}$ to V_{CC}		±75		
		Clock	V_I = −1 V to 13.6 V		±75		
		Any other inputs	$V_I = V_{SS}$ to V_{CC}		±10		
V_{OH}	High-level output voltage		I_O = −0.4 mA		2.4		V
V_{OL}	Low-level output voltage		I_O = 3.2 mA		0.4		V
I_{BB}	Supply current from V_{BB}				1		mA
I_{CC}	Supply current from V_{CC}				125		mA
I_{DD}	Supply current from V_{DD}				30		mA
C_i	Input capacitance (any inputs except clock and data bus)		f = 1 MHz, unmeasured pins at V_{SS}		15		pF
$C_{i(\phi1)}$	Clock-1 input capacitance		f = 1 MHz, unmeasured pins at V_{SS}		100		pF
$C_{i(\phi2)}$	Clock-2 input capacitance		f = 1 MHz, unmeasured pins at V_{SS}		200		pF
$C_{i(\phi3)}$	Clock-3 input capacitance		f = 1 MHz, unmeasured pins at V_{SS}		100		pF
$C_{i(\phi4)}$	Clock-4 input capacitance		f = 1 MHz, unmeasured pins at V_{SS}		100		pF
C_{DB}	Data bus capacitance		f = 1 MHz, unmeasured pins at V_{SS}		25		pF
C_o	Output capacitance (any output except data bus)		f = 1 MHz, unmeasured pins at V_{SS}		15		pF

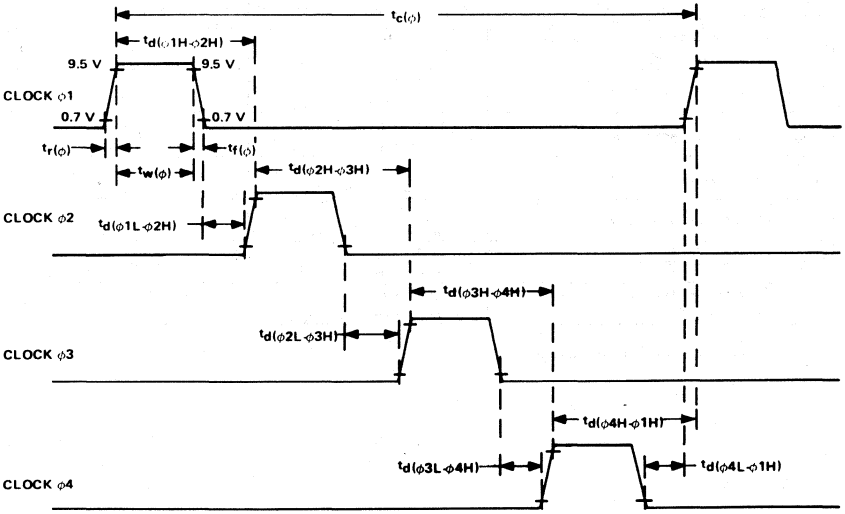
† All typical values are at T_A = 25°C and nominal voltages.

4.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 12 AND 13)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time		0.333		μs
$t_{r(\phi)}$	Clock rise time		12		ns
$t_{f(\phi)}$	Clock fall time		12		ns
$t_{w(\phi)}$	Pulse width, any clock high		45		ns
$t_{d(\phi 1L\text{-}\phi 2H)}$	Delay time, clock 1 low to clock 2 high (time between clock pulses)		5		ns
$t_{d(\phi 2L\text{-}\phi 3H)}$	Delay time, clock 2 low to clock 3 high (time between clock pulses)		5		ns
$t_{d(\phi 3L\text{-}\phi 4H)}$	Delay time, clock 3 low to clock 4 high (time between clock pulses)		5		ns
$t_{d(\phi 4L\text{-}\phi 1H)}$	Delay time, clock 4 low to clock 1 high (time between clock pulses)		5		ns
$t_{d(\phi 1H\text{-}\phi 2H)}$	Delay time, clock 1 high to clock 2 high (time between leading edges)		80		ns
$t_{d(\phi 2H\text{-}\phi 3H)}$	Delay time, clock 2 high to clock 3 high (time between leading edges)		80		ns
$t_{d(\phi 3H\text{-}\phi 4H)}$	Delay time, clock 3 high to clock 4 high (time between leading edges)		80		ns
$t_{d(\phi 4H\text{-}\phi 1H)}$	Delay time, clock 4 high to clock 1 high (time between leading edges)		80		ns
t_{su}	Data or control setup time before clock 1		40		ns
t_h	Data hold time after clock 1		10		ns

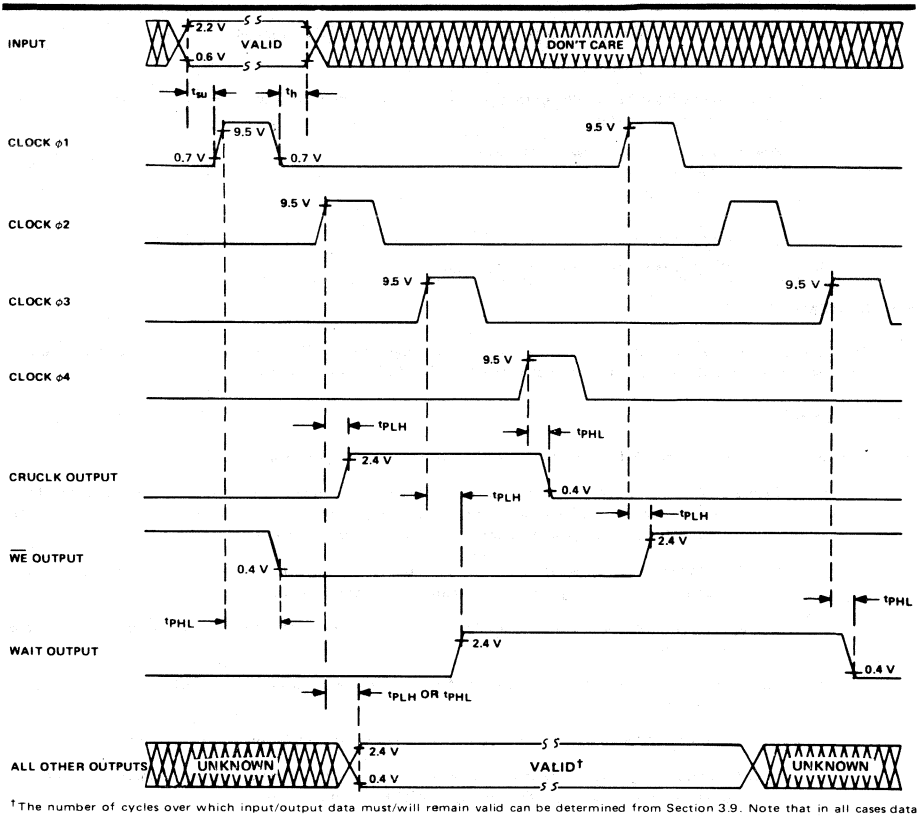
4.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURE 13)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} or t_{PHL}	Propagation delay time, clocks to outputs	C_L = 200 pF		20		ns



NOTE: All timing and voltage levels shown on φ1 applies to φ2, φ3, and φ4 in the same manner.

FIGURE 12 – CLOCK TIMING



†The number of cycles over which input/output data must/will remain valid can be determined from Section 3.9. Note that in all cases data should not change during φ1.

FIGURE 13–SIGNAL TIMING

5. TMS 9900 PROTOTYPING SYSTEM

5.1 HARDWARE

The TMS 9900 prototyping system enables the user to generate and debug software and to debug I/O controller interfaces. The prototyping system consists of:

- 990/4 computer with TMS 9900 microprocessor
- 1024 bytes of ROM containing the bootstrap loader for loading prototyping system software, the front-panel and maintenance utility, and the CPU self-testing feature
- 16,896 bytes of RAM with provisions for expansion up to 57,334 bytes of RAM
- Programmable-write-protect feature for RAM
- Interface for Texas Instruments Model 733 ASR* Electronic Data Terminal with provisions for up to five additional interface moculdes

*Requires remote device control and 1200 baud EIA interface option on 733 ASR.

- Available with Texas Instruments Model 733 ASR Electronic Data Terminal
- 7-inch-high table-top chassis
- Programmer's front panel with controls for run, halt, single-instruction execute, and entering and displaying memory or register contents
- Power supply with the following voltages:
  5 V dc @ 20 A
  12 V dc @ 2 A
  −12 V dc @ 1 A
  −5 V dc @ 0.1 A
- Complete hardware and software documentation.

5.2 SYSTEM CONSOLE

The system console for the prototyping system is the 733 ASR, which provides keyboard entry, 30-character-per-second thermal printer, and dual cassette drives for program loading and storage.

5.3 SOFTWARE

The following software is provided on cassette for loading into the prototyping system:

- Debug Monitor – Provides full control of the prototyping system during program development and includes single instruction, multiple breakpoints, and entry and display capability for register and memory contents for debugging user software under 733 ASR console control.
- One-Pass Assembler – Converts source code stored on cassette to relocatable object on cassette and generates program listing. (Object is upward compatible with other 990 series assemblers).
- Linking Loader – Allows loading of absolute and relocatable object modules and links object modules as they are loaded.
- Source Editor – Enables user modification of both source and object from cassette with resultant storage on cassette.
- Trace Routine – Allows user to monitor status of computer at completion of each instruction.
- PROM Programming/Documentation Facility – Provides documentation for ROM mask generation, or communicates directly with the optional PROM Programmer Unit.

5.4 OPTIONS

The following optional equipment is offered for the prototyping system:

- Battery-pack/standby-power supply
- PROM programming unit and adapter boards
- Universal wire-wrap modules
- Expansion RAM modules
- Expansion EPROM modules
- I/O modules and other interfaces
- Rack-mounted version
- International ac voltage option

6. TMS 9900 SUPPORT CIRCUITS

MEMORY DEVICE	ORGANIZATION/FUNCTION	I/O STRUCTURE	PACKAGE	ACCESS TIME
		RAMS		
TMS 4036-2	64 x 8 static	Common bus	20 pin	450 ns MAX
TMS 4033	1024 x 1 static	Dedicated bus	16 pin	450 ns MAX
TMS 4039-2	256 x 4 static	Dedicated bus	22 pin	450 ns MAX
TMS 4042-2	256 x 4 static	Common bus	18 pin	450 ns MAX
TMS 4050	4096 x 1 dynamic	Common bus	18 pin	300 ns MAX
TMS 4060	4096 x 1 dynamic	Dedicated bus	22 pin	300 ns MAX
		ROMS/PROMS		
TMS 4700	1024 x 8 ROM		24 pin	450 ns MAX
SN74S371	256 x 8 ROM		20 pin	70 ns MAX
SN74S471	256 x 8 PROM		20 pin	70 ns MAX
SN74S472	512 x 8 PROM		20 pin	55 ns TYP
		PERIPHERALS		
SN74LS259†	Addressable latch		16 pin	
SN74LS251†	Data multiplexer		16 pin	
SN74148	Priority encoder		16 pin	
SN74S412	8-bit I/O port		24 pin	
SN75355†	Quad TTL-to-MOS driver		16 pin	
TMS 6011	UART		40 pin	
SN74S241	Bidirectional bus driver		20 pin	

†To be announced.

7. SYSTEM DESIGN EXAMPLES

Figure 14 illustrates a typical minimum TMS 9900 system. Eight bits of input and output interface are implemented. The memory system contains 1024 x 16 ROM and 256 x 16 RAM memory blocks. The total package count for this system is 15 packages.

A maximum TMS 9900 microprocessor system is illustrated in Figure 15. ROM and RAM are both shown for a total of 65,536 bytes of memory. The I/O interface supports 4096-output bits and 4096-input bits. Fifteen external interrupts are implemented in the interrupt interface. The clock generator and control section contains memory decode logic, synchronization logic, and the clock electronics. Bus buffers, required for this maximally configured system, are indicated on the system buses.

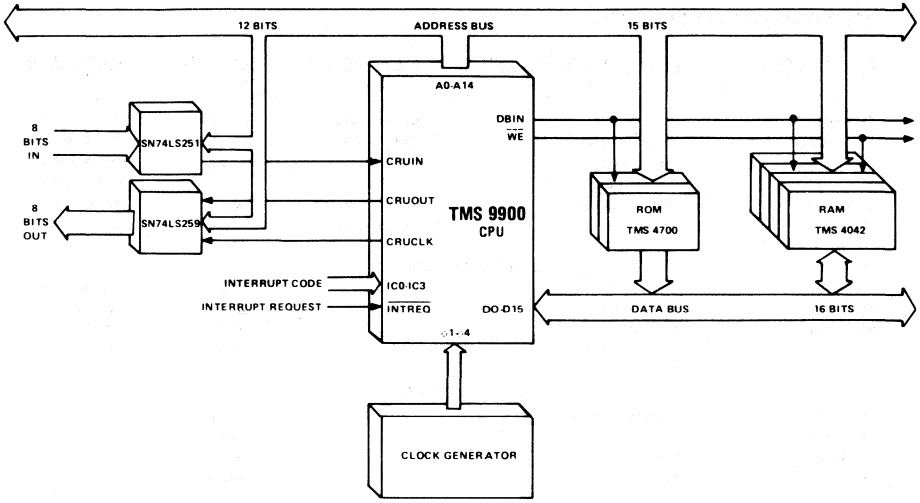


FIGURE 14 – MINIMUM TMS 9900 SYSTEM

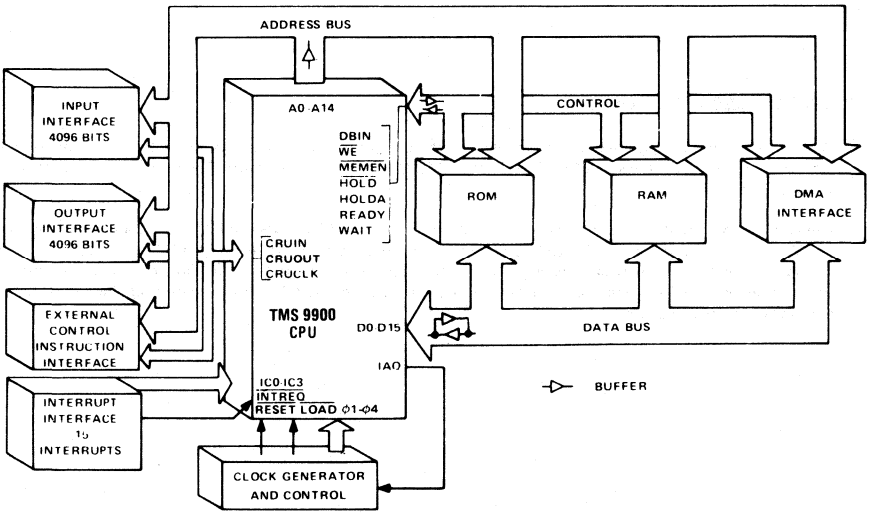
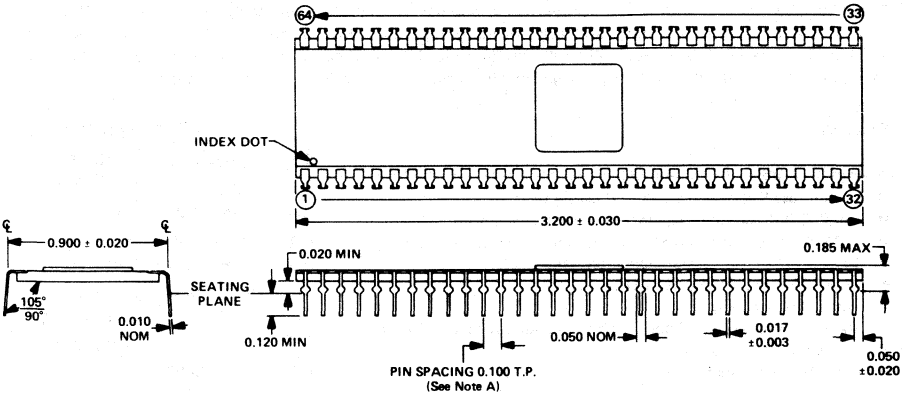


FIGURE 15 – MAXIMUM TMS 9900 SYSTEM

8. MECHANICAL DATA

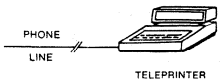


NOTE A. Each pin centerline is located within 0.010 of its true longitudinal position.

9900

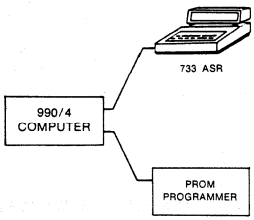
SOFTWARE DEVELOPMENT AIDES

TIMESHARE



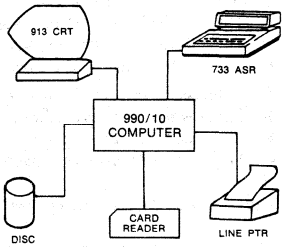
- CROSS-ASSEMBLER AND SIMULATOR AVAILABLE ON:
  - G.E.
  - NCSS
  - TYMESHARE
- BATCH AVAILABLE FOR IBM 360/370

9900 PROTOTYPING SYSTEM



- DEBUG MONITOR
- ONE PASS ASSEMBLER
- SOURCE EDITOR
- SOFTWARE TRACE
- RELOCATABLE LINKING LOADER
- PROM PROGRAMMING
- ROM MASK DOCUMENTATION

9900/990 SOFTWARE DEVELOPMENT SYSTEM



- MULTI-USER SOFTWARE DEVELOPMENT SYSTEM
- MULTI-TASKING DISC BASED OPERATOR SYSTEM
- MULTI-PASS MICROASSEMBLER
- FORTRAN COMPLIER
- SYSTEMS THROUGHPUT

6

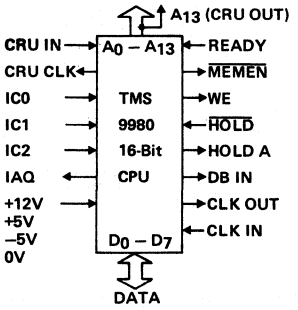
NEW MEMBERS OF THE 9900 FAMILY OF SOFTWARE COMPATIBLE MICROPROCESSORS

TMS 9980 – 8 BIT LOW COST FIXED INSTRUCTION SET MPU.

The TMS 9980 is an 8 bit low cost version of the popular TMS 9900 16 bit MPU. It uses the full 9900 instruction set including 16 bit multiply/16 bit divide and multi-bit shifts plus the 9900's memory to memory architecture. The 9980 is in fact a TMS 9900 with a multiplexed data bus and reduced memory addressing capability enabling the device to be packaged in a low cost 40 pin plastic (or ceramic) package.

Features:-

- Full TMS 9900 Instruction Set.
- 14 Address line giving a 16K addressing field.
- Single T.T.L. compatible clock or Internal oscillator.
- 2048 directly addressable Input/Output parts using the C.R.U.
- 4 levels of vectored, maskable interrupt.
- Direct Memory Access (DMA) capability.
- Reset and Load Inputs.
- Standard N-Channel Silicon gate power supplies +12, ± 5V, O.
- Low cost 40 pin package.
- Available December 1976.

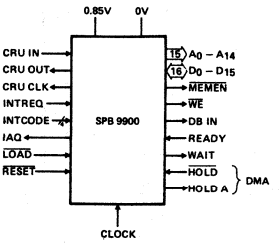


SBP 9900 – 16 BIT FIXED INSTRUCTION SET MICROPROCESSOR

The SBP 9900 is an I^2L implementation of the TMS 9900 N-Channel Silicon gate 16 bit MPU which has been designed specifically to military applications. The operating temperature range of the SBP 9900 will be -55^oC to $+125^oC$. I^2L being a bipolar design technique means that the device inherits all the benefits of a bipolar technology i.e. demonstrated reliability at extended temperature range, simple production process, speed enhancement and single power supplies.

Features:-

- Full TMS 9900 Instruction Set.
- -55 to $+125^oC$ Operating Temp. range.
- Single 0.85 volt power supply.
- Single T.T.L. compatible clock.
- 15 levels of vectored interrupt.
- Direct Memory Access (DMA) capability.
- 16 Bit Data, 15 Bit Address Bus.
- Pin compatible with TMS 9900.



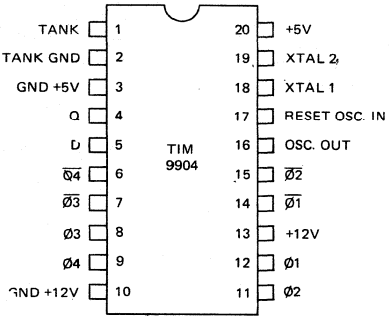
TMS 99XX – 8 BIT MICROCOMPUTER FOR HIGH VOLUME LOW COST APPLICATIONS.

The TMS 99XX is an 8 bit microcomputer i.e. a microprocessor with control ram and data ram on the same I.C. The device will operate from a 3MHz on chip clock and will have 2 levels of interrupt. Input/Output capability is a choice between 18 or 30 depending upon the package size of 28 or 40 pin respectively. The TMS 99XX uses a sub-set of the most important TMS 9900 instructions making the device software compatible with other members of the family.

TMS9900 SUPPORT CIRCUITS

TIM 9904 (SN74LS362) 4 Phase Clock Generator

The TIM 9904 has been designed to make the 4 phase 12 volt clock of TMS 9900 simple to implement. The TIM 9904 requires only two power supplies: +12 volts, +5 volts and three external components: a 48MHz 3rd overtone crystal and an L-C tank circuit. The clock generator supplies a 4 phase clock at +12 volts, 4 phase clock at T.T.L. levels for external circuit synchronisation and one synchronised Q output. The Q output is supplied from an internal D type flip flop which derives its clock from $\overline{3\phi}$ and D input from the external circuit via a Schmitt gate. This can then be used as an auto-sync. input to the TMS 9900 for such functions as reset or load.

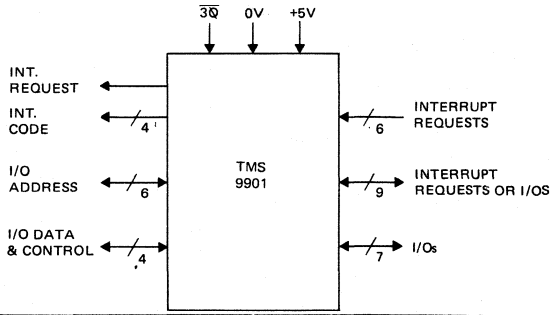


TMS 9901 — Programmable Interrupt and I/O Controller

The TMS 9901 is a dedicated TMS 9900 peripheral circuit which has been designed to control data input/output functions and generate the interrupt request signal and interrupt code. The device is programmable under control of the TMS 9900 to select the function of the input pins. The 22 input/output and interrupt pins are allocated as:

- 6 Dedicated Interrupt Ports
- 7 Dedicated I/O Ports
- 9 Programmable as I/O Ports or Interrupts

The TM9901 is a CRU (Communications Register Unit) peripheral and all data exchanges between the processor and the system are via the CRU line. The device is manufactured using N-channel silicon gate technology and requires only a single 5 Volt power supply.



NEW MEMBERS OF THE 9900 FAMILY OF SOFTWARE COMPATIBLE MICROPROCESSORS

TMS 9902/3 – Asynchronous/Synchronous Communications Controller

The TMS 9902/3 are two dedicated TMS 9900 peripheral circuits which can be used as communications interfaces between terminals, modems and computer. Both devices are CRU (Communications Register Unit) peripherals interfacing between the TMS 9900 and the communications link via the CRU line.

Features

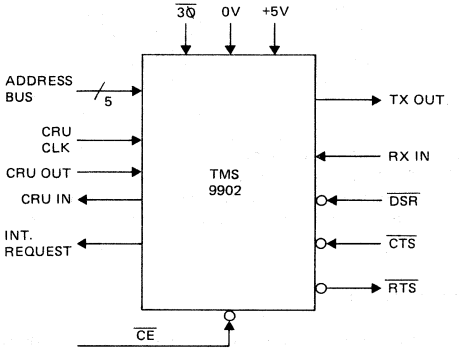
TMS 9902

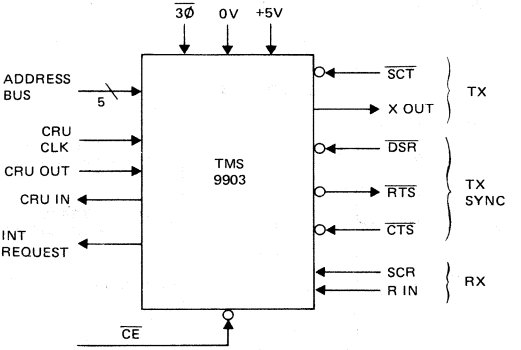
- Programmable Data Rate 110 to 76800 Baud.
- Programmable Character Length
  5–8 Bits 1–1½–2 Stop Bits
  Odd – Even – No Parity
- On Chip Interval Timer 64μsec to 16,384μsec.
- N-Channel Silicon Gate Process, Single 5 Volt Power Supply

TMS 9903

- DC to 250k Bits/Sec
- Programmable Sync. Register and Character Length
- Bi-Sync and SDLC Compatible
- On Chip Interval Timer 64μsec to 16384μsec.
- N-Channel Silicon Gate Process, Single 5 Volt Power Supply

The two devices are designed to be compatible so that in most applications they can be exchanged with only a minor adjustment in pin-out.





Microprocessor Support Circuits

TYPES SN54259, SN74259
8-BIT ADDRESSABLE LATCHES

OCTOBER 1975

features

- 8-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion With Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplifies Expansion

characteristics

- Typical Propagation Delay Times:
  - Enable-to-Output . . . 12 ns
  - Data-to-Output . . . 12 ns
  - Address-to-Output . . 16 ns
  - Clear-to-Output . . . 16 ns
- Fan-Out:
  - I_{OL} (Sink Current) . . . 16 mA
  - I_{OH} (Source Current) . . . −0.8 mA
- Typical I_{CC} . . . 60 mA

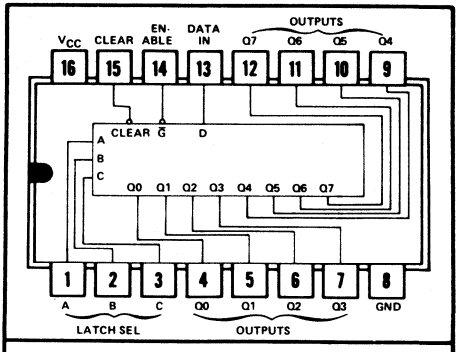
description

These general-purpose TTL octal-addressable latches can be used to implement multiple-function storage elements such as working registers, serial-holding registers, or active-high decoders or demultiplexers. A buffered common clear line is available for initializing.

Four distinct modes of operation are selectable by controlling the clear and $\overline{G}$ inputs as enumerated in the function table. In the addressable-latch mode transparency exists in the addressed latch (see latch selection table) and the respective Q output will follow the data (D) input. When the enable ($\overline{G}$) input is taken high and clear is inactive (H) the memory mode is initiated during which the contents of the eight latches will remain unchanged. During the demultiplexing mode the addressed latch will read out its data content while the remaining seven outputs will be low.

- DIRECT REPLACEMENT FOR FAIRCHILD 9334
- EXPANDABLE FOR N-BIT APPLICATIONS
- FOUR DISTINCT FUNCTIONAL MODES

SN54259 . . . J OR W PACKAGE
SN74259 . . . J OR N PACKAGE
(TOP VIEW)



logic: See function table

FUNCTION TABLE

INPUTS CLEAR	INPUTS $\overline{G}$	OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

LATCH SELECTION TABLE

SELECT INPUTS C	B	A	LATCH ADDRESSED
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H ≡ high level, L ≡ low level
D ≡ the level at the data input
Q_{i0} ≡ the level of Q_i (i = 0, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.

TEXAS INSTRUMENTS

recommended operating conditions

		SN54259			SN74259			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Width of enable pulse, $t_{w(enable)}$		15			15			ns
Width of clear pulse, $t_{w(clear)}$		15			15			ns
Setup time, t_{su}	Data	15↑			15↑			ns
	Address	5↑			5↑			
Hold time, t_h	Data	0↑			0↑			ns
	Address	20↑			20↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54259			SN74259			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = 12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Enable	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Enable	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18		−57	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX		60	90		60	90	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

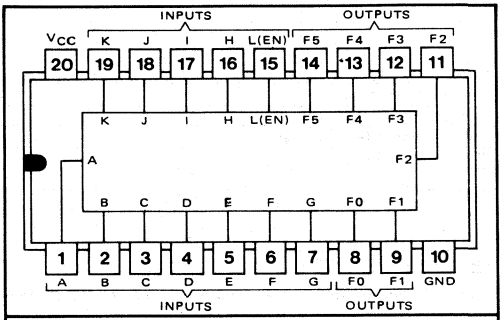
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable	C_L = 15 pF, R_L = 400 Ω		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable			11	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output from data			14	24	ns
t_{PHL}	Propagation delay time, high-to-low-level output from data			11	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output from address			15	28	ns
t_{PHL}	Propagation delay time, high-to-low-level output from address			17	28	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			16	25	ns

SN54S330,SN54S331,SN74S330,SN74S331
12-INPUT/6-OUTPUT EXPANDABLE FIELD-PROGRAMMABLE LOGIC ARRAYS

- Field-Programmable Logic Array Organized 12-Inputs/50-Product Terms/6-Outputs
- Programmable Options Include:
  - Active High or Low Inputs/Outputs
  - Input L Can Be Logic Input Or Dedicated As An Enable Input
  - Automatic Disabling If Product Term Is Not Used
  - Dedicated Enable and Automatic Disabling Facilities Expansion of Number of Inputs, Outputs, and Product Terms
- Compact 20-Pin Package with Pin-Rows On 300-Mil Spacing
- Fully Schottky Clamping for High-Performance:
  - 35 ns Typical Data Delay Time
  - 20 ns Typical Enable Time
- Reliable Ti-W Fuse Links for Fast, Low-Voltage Programming
- Choice of 3-State ('S330) or 2.5 kΩ Passive-Pullup ('S331) Outputs
- 'S331 Drives Low-Threshold MOS Directly

J OR N PACKAGE (TOP VIEW)



positive logic: see description and function diagram

description

These high-performance, Schottky-clamped 12-input, 6-output logic arrays can be field programmed to provide 50 product terms derived from the 12 inputs and sum the 50 products onto 6-output lines. They feature an input (L/EN) which can be dedicated during programming to serve as an output enable line making the FPLA expandable with respect to product terms. As the enable can be programmed active high or low, package selection can be implemented for two FPLA's with no external components.

For every product term, 12 input variables can be programmed as high or low. Logic flexibility is further enhanced by the feature that the six outputs can be programmed individually to be active high or low. Unused product terms can be programmed to disable all outputs.

The SN54S/74S330 is implemented with bus-driving 3-state outputs and can be connected directly to similar outputs in a bus-organized system.

The SN54S/74S331 is implemented with a 2.5 kΩ passive pull-up resistor on each output meaning that:

a. The output can be combined with other similar or open-collector outputs to perform the logical wire-AND or a simple enable/disable function.

b. The outputs are also rated to source 250 μA of current at V_{OH} = 3.7 V minimum for direct interface with low threshold logic families such as MOS.

The Ti-W fuse links, also used in these FPLA's, feature the same low-voltage programming characteristics and proven reliability which Texas Instruments PROM's have demonstrated over a number of years.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S330, SN54S331 . . . . . −55°C to 125°C
SN74S330, SN74S331 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S330, SN54S331			SN74S330, SN74S331			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	'S330 (T-S)			−2			−6.5	mA
	'S331 (2.5 kΩ Pullup)			−0.5			−0.65	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

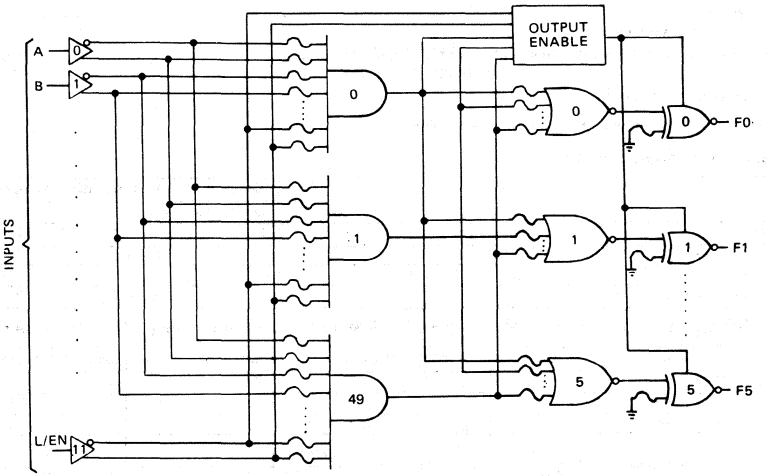
PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	'S330	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = MAX	2.4	3.4		2.4	3.1		V
		'S331		I_{OH} = 250 μA	3.7	4.3		3.7	4.3		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_{OZH} or I_{off}	Off-state output current, high-level voltage applied	'S330	V_{CC} = MAX	V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	'S330	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}	Short-circuit output current*	'S330	V_{CC} = MAX		−30		−100	−30		−100	mA
		'S331	V_{CC} = 5 V		−1.5		−2.9	−1.5		−2.9	
I_{CC}	Supply current	'S330	V_{CC} = MAX,	See Note 2		110			110		mA
		'S331				122			122		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
*Not more than one output of the 'S330 should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any input	Any output	C_L = 30 pF		35		ns
t_{PHL}					35		
t_{ZL}	Enable	Any output			15		ns
t_{ZH}					15		
t_{HZ}	Enable	Any output	C_L = 5 pF		20		ns
t_{LZ}					20		

functional block diagram



$F_i = [(A+\bar{A})\cdot(B+\bar{B})\ldots\ldots(L+\bar{L})] + [(A+\bar{A})\cdot(B+\bar{B})\ldots\ldots(L+\bar{L})]_1 + \ldots\ldots + [(A+\bar{A})\cdot(B+\bar{B})\ldots\ldots(L+\bar{L})]_{49}$

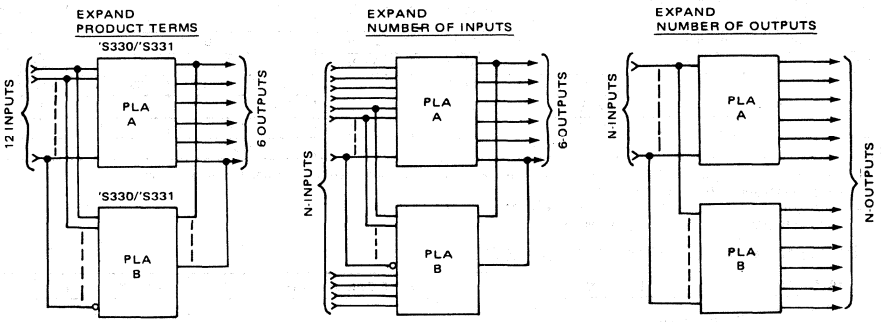
$F_i = (ABC\ldots\ldots L)_0 + (ABC\ldots\ldots L) + \ldots\ldots + (ABC\ldots\ldots L)_{49}$

WHERE:

$F_i = F_0, F_1, F_2, F_3, F_4$, or F_5

$(ABC\ldots\ldots L)_i$ = 12 PROGRAMMABLE INPUTS FOR EACH OF 50 PRODUCT TERMS

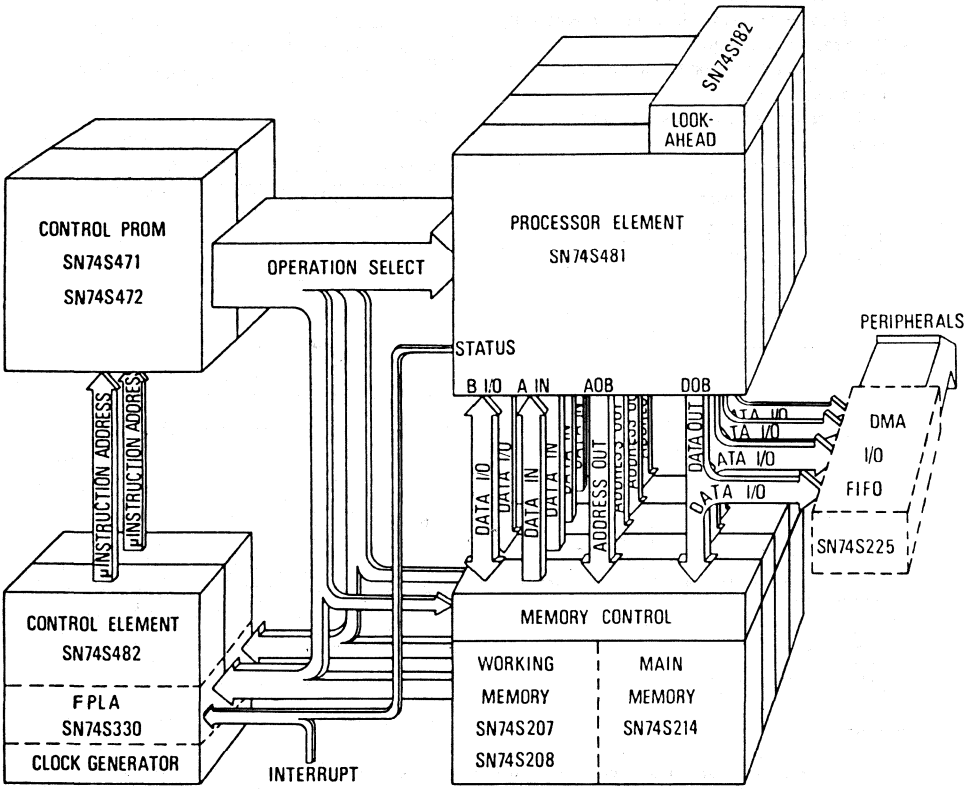
expanding product term, inputs and outputs



- CODE OUTPUT ENABLES TO ENABLE PLA "A" FOR SOME INPUT PATTERNS AND PLA "B" FOR THE REST
- OVERLAP INPUTS BY N-BITS
- CODE OUTPUT ENABLES TO ENABLE PLA "A" OR "B" AS APPROPRIATE
- USE OUTPUTS INDEPENDENTLY
- CODE OUTPUT ENABLES THE SAME FOR BOTH PLA A AND B

TEXAS INSTRUMENTS

SCHOTTKY BIT-SLICE MICROCOMPUTER



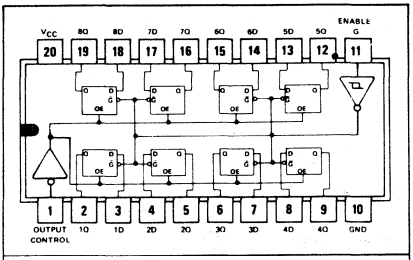
6

TYPES SN54S373, SN54S374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

OCTOBER 1975

- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading and Reloading
- Buffered Control Inputs
- Clock/Enable Input has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines

SN54S373 . . . J PACKAGE
SN74S373 . . . J OR N PACKAGE
(TOP VIEW)

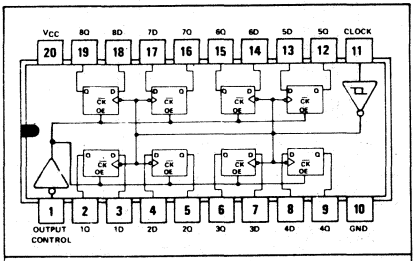


logic: see function table

SN74S373

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Hi-Z

SN54S374 . . . J PACKAGE
SN74S374 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

SN74S374

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Hi-Z

Q_0 = the level of Q before the indicated steady-state input conditions were established.
H = high level
L = low level
Hi-Z = high impedance
X = irrelevant
↑ = transition from low to high level

description

These 8-bit registers feature totem-pole 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing:

Buffer Registers

I/O Ports

Bidirectional Bus Drivers

Working Registers.

The SN54S373 and SN74S373 are transparent D-type latches meaning that while the enable (G) is high the Q output will follow the data (D) input. When the enable is taken low the output will be latched at the data that was setup.

TEXAS INSTRUMENTS

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

description (continued)

The SN54S374 and SN74S374 are edge-triggered D-type flip-flops. On the positive transition of the clock the Q output will be set to the logic state that was setup at the D input.

Schmitt-trigger buffered inputs at the enable ('S373) and clock ('S374) lines simplifies system design as a-c and d-c noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state (Hi-Z). In the Hi-Z state the outputs neither load nor drive the bus line significantly.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S373, SN54S374 . . . . . −55°C to 125°C
SN74S373, SN74S374 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S373, SN54S374			SN74S373, SN74S374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				2			6.5	mA
Width of clock/enable pulse, t_w	High	6			6			ns
	Low	7.3			7.3			
Data setup time, t_{su}	'S373	0↓			0↓			ns
	'S374	5↑			5↑			
Data hold time, t_h	'S373	10↓			10↓			ns
	'S374	2↑			2↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓ The arrow indicates the transition of the clock/enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

6

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	SN54S'	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		V
		SN74S'			2.4	3.1		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			50	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V			−250	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX	'S373		105	160	mA
				'S374		90	140	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

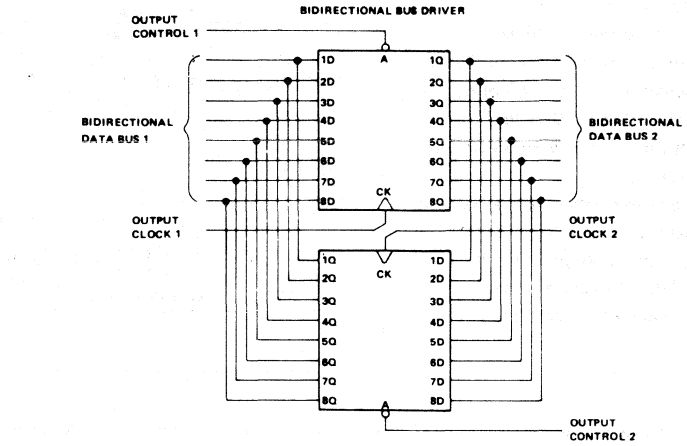
switching characteristics, V_{CC} = 5 V, T_A = 25°C

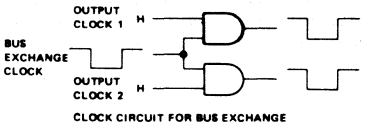
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373 MIN	'S373 TYP	'S373 MAX	'S374 MIN	'S374 TYP	'S374 MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Note				75	100		MHz
t_{PLH}	Data	Any Q			5	9				ns
t_{PHL}					9	13				
t_{PLH}	Clock or enable	Any Q			7	14		8	15	ns
					12	18		11	17	
t_{ZH}	Output Control	Any Q			8	15		8	15	ns
t_{ZL}					11	18		11	18	
t_{HZ}	Output Control	Any Q	C_L = 5 pF, R_L = 280 Ω, See Note		6	9		5	9	ns
t_{LZ}					8	12		7	12	

NOTE: f_{max} is tested with all outputs loaded. See load circuits and waveforms on page S-87 of *Supplement to The TTL Data Book for Design Engineers*, CC416.

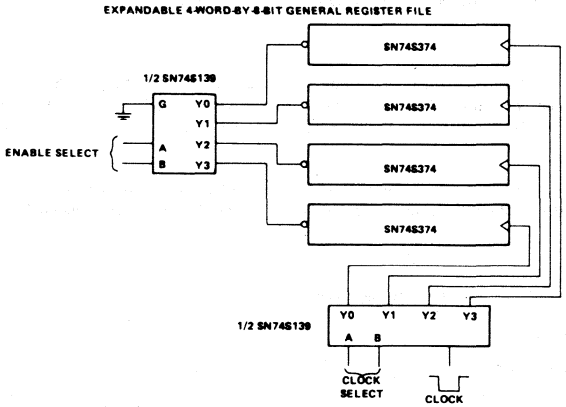
f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high level
t_{PHL} ≡ propagation delay time, high-to-low level
t_{ZH} ≡ output enable time to high level
t_{ZL} ≡ output enable time to low level
t_{HZ} ≡ output disable time from high level
t_{LZ} ≡ output disable time from low level

APPLICATIONS





CLOCK CIRCUIT FOR BUS EXCHANGE

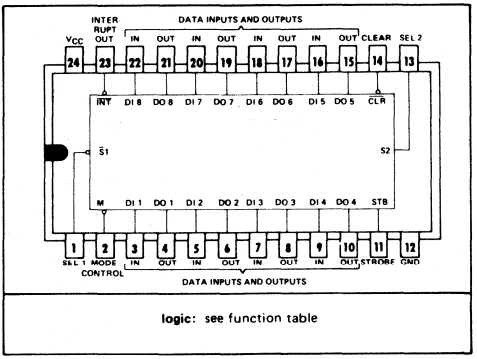


TYPES SN54S412, SN74S412
MULTI-MODE BUFFERED LATCHES

OCTOBER 1975

- P-N-P Inputs and 3-State Outputs Maximize I/O and Data Bus Capabilities
- Data Latch Transparency Permits Asynchronous or Latched Receiver Modes
- Mode and Select Inputs Permit Storing With Outputs Enabled or Disabled
- Strobe-Controlled Flag Flip-Flop Indicates Status or Interrupt
- Asynchronous Clear Sets All Eight Data Lines Low and Initializes Status Flag
- High-Level Output Voltage, Typically 4 V, Drives Most MOS Functions Directly
- Direct Replacement for Intel 3212 or 8212

SN54S412 . . . J OR W PACKAGE
SN74S412 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The three-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides package busy or request interrupt commands. The outputs, with a 4-volt typical high-level voltage, are compatible for driving low-threshold MOS directly.

DATA LATCHES

The eight data latches are fully transparent when the internal gate enable, G, input is high and the outputs are enabled (OE = H). Latch transparency is selected by the mode control (M), select ($\overline{S1}$ and S2), and the strobe (STB) inputs and during transparency each data output (DO_i) follows its respective data input (DI_i). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches. See data latches function table.

MODE SELECTION

An input mode or an output mode is selectable from this single input line. In the input mode, MD = L, the eight data latch inputs are enabled when the strobe is high regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken low, the latches will store the most-recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S1}$ and S2) inputs. See data latches function table.

STATUS FLIP-FLOP

The status flip-flop provides a low-level output signal when:

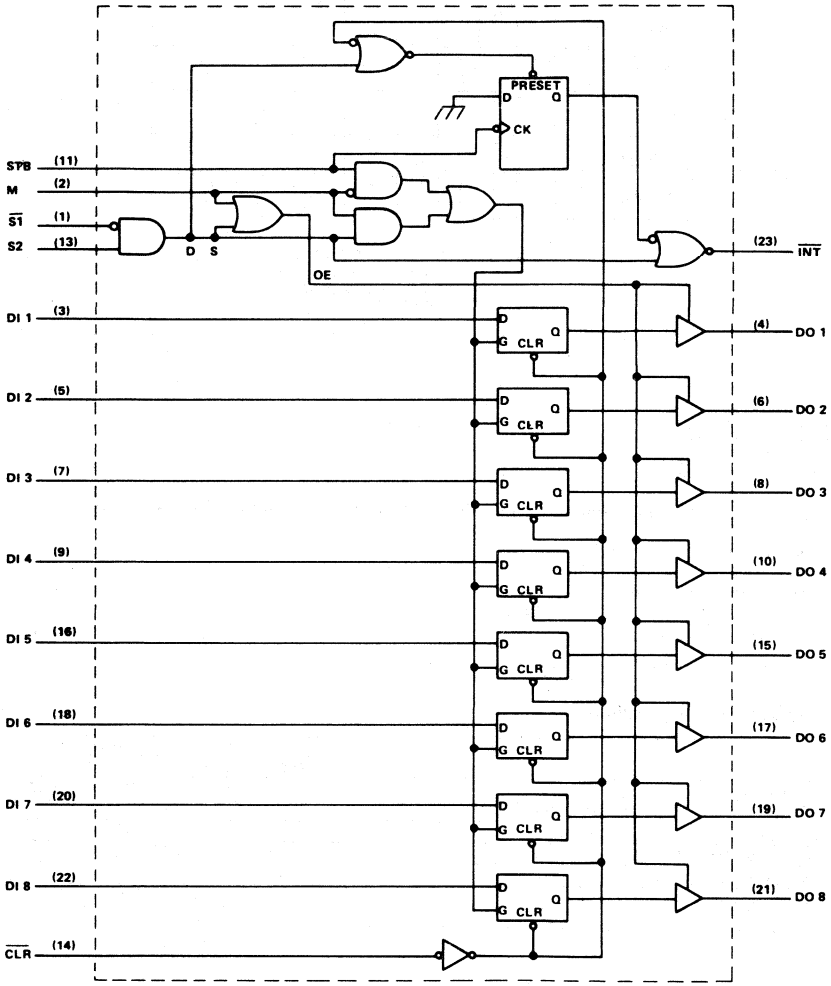
a. the package is selected

b. a strobe input is received.

This status signal can be used to indicate that the register is busy or to initiate an interrupt type command.

† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

functional block diagram



DATA LATCHES FUNCTION TABLE

FUNCTION	CLEAR	M	$\overline{S1}$	S2	STB	DATA IN	DATA OUT
Clear	L	H	H	X	X	X	L
	L	L	L	H	L	X	L
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	Q_O
	H	L	L	H	L	X	Q_O
Data Bus	H	H	L	H	X	L	L
	H	H	L	H	X	H	H
Data Bus	H	L	L	H	H	L	L
	H	L	L	H	H	H	H

STATUS FLIP-FLOP FUNCTION TABLE

CLEAR	$\overline{S1}$	S2	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	L	H	X	L

H ≡ high level (steady state)
L ≡ low level (steady state)
X ≡ irrelevant (any input, including transitions)
Z ≡ high impedance (off)
↓ ≡ transition from low to high level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S412 . . . . . −55°C to 125°C
SN74S412 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S412			SN74S412			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Pulse width, t_w (see Figures 1, 2, and 4)	STB or $\overline{S1}$ · S2	25			25			ns
	Clear low	25			25			
Setup time, t_{su} (see Figure 3)		15↓			15↓			ns
Hold time, t_h (see Figures 1 and 3)		20↓			20↓			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S412			SN74S412			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.85			0.85	V
V_{IK}	Input clamp voltage		V_{CC} = MIN;	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	3.65	4		3.65	4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 15 mA			0.45			0.45	V
				I_{OL} = 20 mA			0.5			0.5	
I_{OZH}	Off-state output current, high-level voltage applied	DO 1 thru DO 8	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	DO 1 thru DO 8	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 5.25 V			20			10	μA
I_{IL}	Low-level input current	$\overline{S1}$	V_{CC} = MAX,	V_I = 0.4 V			−1			−1	mA
		M					−0.75			−0.75	
		All others					−0.25			−0.25	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−65	−20		−65	mA
I_{CC}	Supply current		V_{CC} = MAX,	see Note 2		82			82	130	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open, clear input at 4.5 V, and all other inputs grounded.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	STB, $\overline{S1}$, or S2	Any DO	1	C_L = 30 pF, See Note 3		18	27	ns
t_{PHL}						15	25	
t_{PHL}	$\overline{CLR}$	Any DO	2			18	27	ns
t_{PLH}	DI_i	DO_i	3			12	20	ns
t_{PHL}						10	20	
t_{PLH}	$\overline{S1}$ or S2	$\overline{INT}$	4	C_L = 30 pF, See Note 4		12	20	ns
t_{PHL}	STB	$\overline{INT}$	4			16	25	
t_{ZH}	$\overline{S1}$, S2, or M	Any DO	5	C_L = 30 pF, See Note 3		21	35	ns
t_{ZL}						25	40	
t_{HZ}	$\overline{S1}$, S2, or M	Any DO	5	C_L = 5 pF, See Note 3		9	20	ns
t_{LZ}						12	20	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{ZH} ≡ output enable time to high level
t_{ZL} ≡ output enable time to low level
t_{HZ} ≡ output disable time from high level
t_{LZ} ≡ output disable time from low level

NOTES: 3. Three-state output load circuit is shown on page S-87 of the *Supplement to the TTL Data Book for Design Engineers*, CC-416.
4. Bi-state totem-pole output load circuit is shown on page S-87 of the *Supplement to the TTL Data Book for Design Engineers*, CC-416.

PARAMETER MEASUREMENT INFORMATION

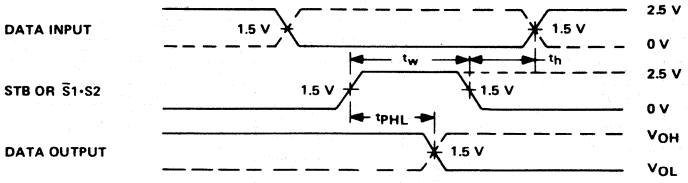


FIGURE 1 – STROBE OR SELECT TO DATA OUTPUT

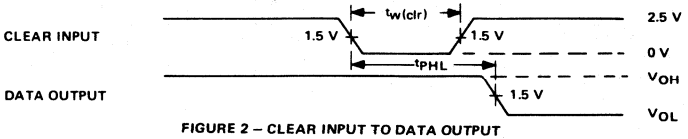


FIGURE 2 – CLEAR INPUT TO DATA OUTPUT

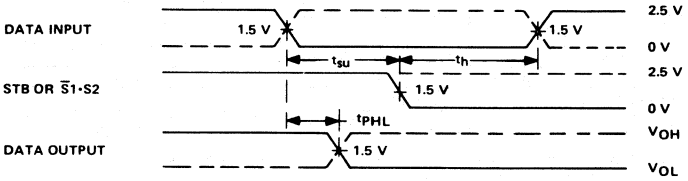


FIGURE 3 – DATA INPUT TO DATA OUTPUT

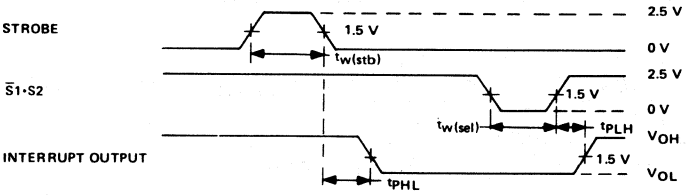


FIGURE 4 – STROBE OR SELECT TO INTERRUPT OUTPUT

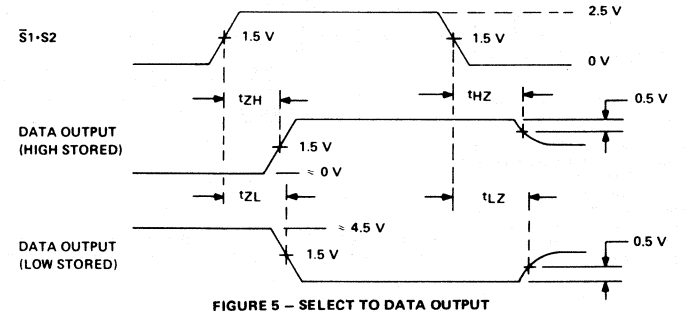
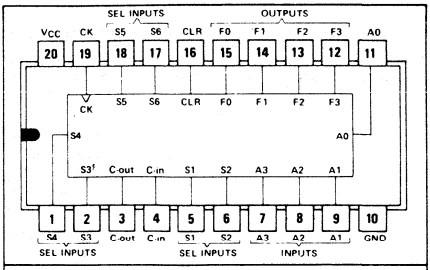


FIGURE 5 – SELECT TO DATA OUTPUT

TEXAS INSTRUMENTS

- 4-Bit Slice is Cascadable to N-Bits
- Designed Specifically for Microcontroller/ Next-Address Generator Functions
- Increment/Decrement by One (Immediate or Direct Symbolic Addressing Modes)
- Offset, Vector, or Branch (Indexed or Relative Addressing Modes)
- Store Up to Four Returns or Links (Program Return Address from Subroutine)
- Program Start or Initialize (Return to Zero or Clear Mode)
- On-Chip Edge-Triggered Output Register (Provides Steady-State Micro-Address/ Instruction)
- High-Density 20-Pin Dual-in-Line Package with 300-Mil Row Pin Spacing

SN54S482 . . . J PACKAGE
SN74S482 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: See function table.

description

The 'S482 is a high-performance Schottky TTL 4-bit-slice control element for use in any computer/control application requiring the coupling of high-performance bipolar speeds with the flexibility of microprogram control and bit-slice expandability. When used as a next-address generator, two 'S482 elements can address up to 256 words of microprogram; three elements can addresss up to 4096 words of microprogram; or a number of 'S482 elements can generate N words in multiples of four lines.

Comprised of an output register, push-pop stack, and a full adder, the 'S482 provides the capability to implement multiway testing needed to generate or to determine and select the source of the next function of microprogram address.

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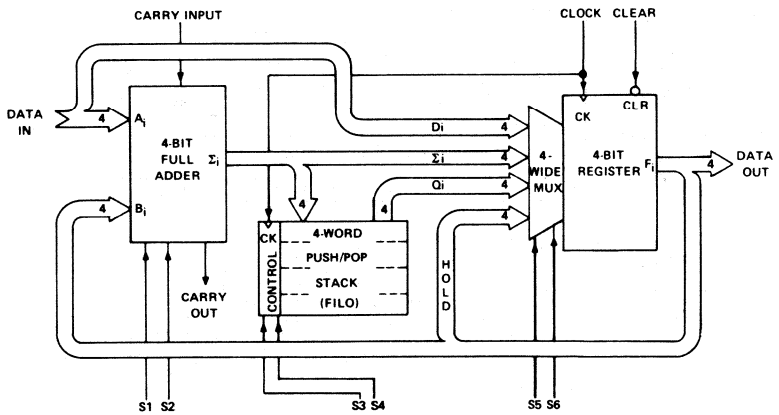
functional block diagram



output register and source functions

The 4-bit edge-triggered register provides a steady-state output throughout each system clock cycle. An asynchronous clear extends the multiway testing to directly implement system initialization at ROM address zero.

Two source-select lines (S5, S6) provide the output register with access to either the current instruction (no change), an operand or address stored in the push-pop stack, the output of a four-function full adder, or a direct data-in address port. The sources and functions are summarized in Tables I and II.

TABLE I. REGISTER SOURCE FUNCTIONS

SELECT		REGISTER INPUT SOURCE
S5	S6	
L	L	DATA-IN PORT (Di)
L	H	FULL ADDER OUTPUTS (Σi)
H	L	PUSH-POP STACK OUTPUTS (Qi)
H	H	REGISTER OUTPUTS (HOLD)

H ≡ high level, L ≡ low level

TABLE II. PUSH-POP STACK CONTROL AND REGISTER-SOURCE FUNCTIONS

	INPUTS						INTERNAL	OUTPUTS
	S3	S4	S5	S6	CLOCK	CLEAR	QiA	Fi
HOLD	X	X	X	X	L	H	QiA0	Fi0
CLEAR	X	X	X	X	X	L	QiA0	L
PUSH-POP STACK "HOLD"	L	L	L	L	↑	H	QiA0*	Di
	L	L	L	H	↑	H	QiA0*	Σi
	L	L	H	L	↑	H	QiA0*	QiA0
	L	L	H	H	↑	H	QiA0*	Fi0
PUSH-POP STACK "LOAD"	L	H	L	L	↑	H	Σi*	Di
	L	H	L	H	↑	H	Σi*	Σi
	L	H	H	L	↑	H	Σi*	QiA0
	L	H	H	H	↑	H	Σi*	Fi0
PUSH-POP STACK "POP"	H	L	L	L	↑	H	QiB0†	Di
	H	L	L	H	↑	H	QiB0†	Σi
	H	L	H	L	↑	H	QiB0†	QiA0
	H	L	H	H	↑	H	QiB0†	Fi0
PUSH-POP STACK "PUSH"	H	H	L	L	↑	H	Σi‡	Di
	H	H	L	H	↑	H	Σi‡	Σi
	H	H	H	L	↑	H	Σi‡	QiA0
	H	H	H	H	↑	H	Σi‡	Fi0

MSB LSB
i ≡ 3, 2, 1, 0
Ai ≡ Data inputs
QiA ≡ Push-pop stack word A output (internal)
QiA0 ≡ the level of Qi before the indicated inputs conditions were established.

Fi ≡ Device outputs
Fi0 ≡ the level of Fi before the indicated input conditions were established.
Σi ≡ Adder outputs (internal)
*QiB, QiC, QiD do not change
†QiD0 → QiD, QiD0 → QiC, QiC0 → QiB, QiB0 → QiA
‡QiA0 → QiB, QiB0 → QiC, QiC0 → QiD

push-pop stack control

The 4-word push-pop stack can be used for nesting up to four levels of program or return (link) addresses. In the load mode, the first (top) word is filled with new data from the output of the full adder, and no push occurs meaning that previous data at that location is lost. However, all other word locations in the push-pop stack remain unchanged. In the push mode, the new word is again entered in the first (top) location; however, previous data residing in the top three words are pushed down one word location and retained at their new locations. The bottom word is written over and lost.

In the pop mode, words in the push-pop stack move up one location on each clock transition. A unique function is provided by the bottom (fourth) register as its content is retained during the pop mode, and after 3 clock transitions, all words in the stack are filled with the operand/address that occupied the bottom register.

The operand/address will remain available indefinitely if stack functions are limited to the pop or hold modes.

The push-pop stack functions are shown in Tables II and III.

TABLE III. PUSH-POP STACK FUNCTIONS

	FUNCTION	SEL. S3	SEL. S4	REG. D	REG. C	REG. B	REG. A	INPUT/ OUTPUT
BIT 0	LOAD	L	H	QiD0	QiC0	QiB0	← Σi	Σi IN
BIT 1	PUSH	H	H	← QiC0	← QiB0	← QiA0	← Σi	Σi IN
BIT 2	POP	H	L	↶ → QiD0	→ QiD0	→ QiC0	→ QiB0	QiA OUT
BIT 3	HOLD	L	L	QiD0	QiC0	QiB0	QiA0	QiA OUT

μlink operations show previous data location after clock transition.

6

full adder

The four-function full adder is controllable from select inputs S1 and S2 to perform:

A or B incrementation, or decrementation of B

Unconditional jumps or relative offsets

No change

Return to zero or one

Incrementation can be implemented by forcing a carry (high) into the ALU. In this mode either of the following options are possible:

1. Increment (A plus zero plus carry)
2. Increment B (zero plus B plus carry), or decrement B (all highs at A then A plus B with carry input low and disregard, don't use, carry out)
3. Increment the jump or offset (A plus B plus carry)

full adder (continued)

4. Start at zero or one and increment on each clock (select zero plus zero plus carry, then select zero plus B plus carry), or set register to N and decrement B (see 2 above).
5. No change (carry input is always active and removal of carry combined with either the ALU or register hold mode will retain the current address).

Unconditional jumps can be implemented by applying and selecting the jump directly from the data inputs to the output register. Offset can be accomplished by summing the output register with the offset magnitude (A plus B) with carry low.

The ALU functions are shown in Table IV.

TABLE IV. ADDRESS CONTROL FUNCTIONS

INPUTS		INTERNAL
S1	S2	Σi
H	H	0 PLUS 0 PLUS C-in
H	L	0 PLUS Bi PLUS C-in
L	H	Ai PLUS 0 PLUS C-in
L	L	Ai PLUS Bi PLUS C-in

compound generator functions

As the function-select lines of the register sources, push-pop stack, and adder are independent, compound functions can be selected to occur on the next clock transition.

Subroutine branches and returns can be simplified by saving the return or link addresses in the push-pop stack. This branch-and-save function can be accomplished on the same clock time as follows:

DATA-IN	ADDER	PUSH-POP STACK	REGISTER SOURCE
Branch address	Zero plus B plus one (S1 = H, S2 = L)	Push (S3 = S4 = H)	Data-in (S5 = S6 = L)

Up to four branches can be made with the return stored in the 4-word push-pop stack.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S482 . . . . . −55°C to 125°C
SN74S482 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. All voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S482			SN74S482			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Carry output			−1			−1	mA
	Any F output			−2			−2	
Low-level output current, I_{OL}	Carry output			10			10	mA
	Any F output			16			16	
Setup time, t_{su}	Data-in, S5, S6	0↑			0↑			ns
	Data-in via adder	20↑			15↑			
	S1, S2	40↑			30↑			
	S3, S4	20↑			15↑			
	Clear-inactive state	0↑			0↑			
Pulse width, t_w	Clock (high or low)	50			30			ns
	Clear (low)	15			15			
Clock input rise time, t_r		20			25			ns
Hold time, t_h	Data-in, S5, S6	30↑			25↑			ns
	Data-in via adder	15↑			10↑			
	S1, S2	15↑			10↑			
	S3, S4	25↑			20↑			
Operating free-air temperature, T_A		−55		125	0	25	70	°C

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S482			SN74S482			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	S1, S2, Cin	V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
		S3, S4, S5, S6, clock					100			100	
		Clear					250			250	
		Any A					150			150	
I_{IL}	Low-level input current	S1, S2	V_{CC} = MAX,	V_I = 0.5 V			−1			−1	mA
		C-in					−0.8			−0.8	
		S3, S4					−1.2			−1.2	
		Any A, S5, S6, CK					−2			−2	
		Clear					−4			−4	
		Clock					−2.8			−2.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−110	−40		−110	mA
I_{CC}	Supply current		V_{CC} = MAX			90	130		90	140	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	SN54S482			SN74S482			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLOCK	DATA OUT	C_L = 15 pF, R_L = 280 Ω		12	30		12	25	ns
t_{PHL}					15	30		15	25	
t_{PHL}	CLEAR	DATA OUT			12	25		12	20	ns
t_{PLH}	CARRY IN	CARRY OUT			12	22		12	18	ns
t_{PHL}					10	22		10	18	
t_{PLH}	DATA IN	CARRY OUT			17	30		17	25	ns
t_{PHL}					12	30		12	25	

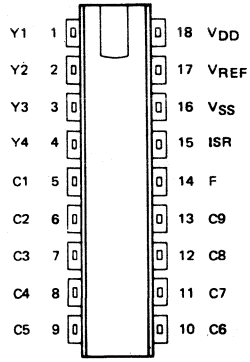
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

TMS 1976 JL, NL
CAPACITIVE-TOUCH-KEYBOARD-TO-MOS INTERFACE

JANUARY 1976

- Variable Sensitivity to Capacitive Inputs
- Nine Inputs for Capacitive-Key Interface
- Designed for Multiplex Operation to Increase Key Count
- Capacitive Inputs Prioritized and Encoded On-Chip
- Direct Interface to CMOS and most PMOS Logic Devices
- Single-Voltage Supply Operation
- Open-Drain Outputs (Compatible with TMS 1000 Inputs)
- PMOS Technology

18-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 1976 JL, NL converts outputs of a capacitive-touch keyboard to signals compatible with the TMS 1000/1100 series microcomputers. Capacitive-touch keys are formed by placing two capacitors in series. These capacitive-touch keys are located in an array, which is scanned. Application of an AC grounded external capacitor, such as the human body, to the junction of the two capacitors alters the net capacitive value of the key, which lowers the voltage on the capacitive-input lines. The TMS 1976 detects this voltage change and prioritizes and encodes it into a 4-bit binary word. The priority system prevents the generation of invalid encoder outputs if two or more keys are touched simultaneously.

The TMS 1976 is offered in 18-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. The series is characterized for operation from 0°C to 70°C.

6

operation

capacitive inputs (C1 through C9)

The capacitive-input section consists of three functional elements: input buffers, latches, and an encoder. The nine capacitive-input lines, C1 through C9, are inputs to nine identical buffers. The input buffers perform a dual function. First, the input line is biased through a very-low-current source to a high input level. Second, the buffer is designed to detect negative transitions from the bias point. An externally generated reference voltage applied to the V_{REF} pin is supplied to the input buffers. C-input levels are compared to this reference voltage. Input buffers supply set commands to nine identical latches. An input level on a C line 0.5 volt more negative than the reference voltage is detected and the buffer sets the corresponding latch to a logic low.

Outputs from the latched inputs are supplied to the encoder. The encoder performs two functions. First, it prioritizes the inputs assigning highest priority to the C1 line and lowest priority to the C9 line. Second, it encodes the touched input having the highest priority input on to four output lines, according to the code defined in Table 1.

operation (continued)

TABLE 1

ISR INPUT	DETECTED INPUT	OUTPUTS			
		Y4	Y3	Y2	Y1
L	C1	L	L	L	H
L	C2	L	L	H	L
L	C3	L	L	H	H
L	C4	L	H	L	L
L	C5	L	H	L	H
L	C6	L	H	H	L
L	C7	L	H	H	H
L	C8	H	L	L	L
L	C9	H	L	L	H
L	NO KEY	L	L	L	L
L	RESET	L	L	L	L

fixed input (F)

The F input is similar to a TMS 1000 input in that it can be used with a standard mechanical key or logic-voltage-level input. The F input structure consists of only a buffer to match the voltage range of the F input to levels compatible with TMS 1000 type inputs. The F-input data will appear unchanged on output Y1 as seen in Table 2.

TABLE 2

INPUTS		OUTPUTS			
ISR	F	Y4	Y3	Y2	Y1
H	L	L	L	L	L
H	H	L	L	L	H

input select and reset control (ISR)

The ISR control line selects either the capacitive inputs (C1 through C9) or the fixed input (F). A high level on ISR will select the F input. A low level or floating condition on ISR will cause the C inputs to be selected. ISR also resets the capacitive-input latches in preparation for the next keyboard-scan pulse. A high level on ISR will unconditionally reset these latches and maintain a reset condition until returned to a low level. All reset latches will generate the same output as if no keys were pressed. Automatic reset of the capacitive latches can be performed by alternate scanning by a TMS 1000. Odd scans can address the keys while even scans can reset the latches.

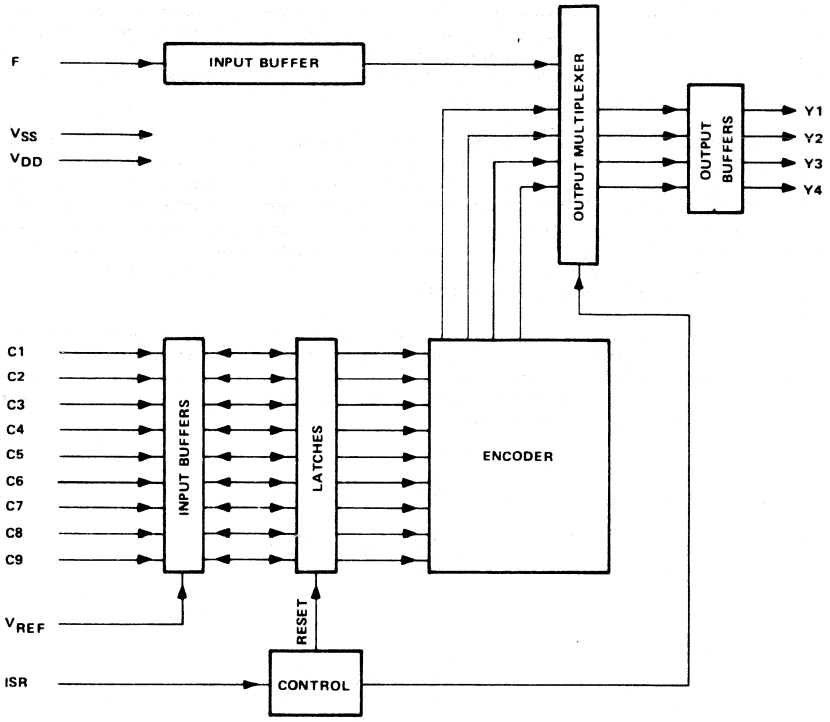
voltage reference (V_{REF})

The voltage level at V_{REF} sets the input compare levels for the capacitive inputs. Thus to operate as a capacitive-touch circuit V_{REF} must always be applied. To detect a high level, the voltage on the capacitive-input line must be more positive than V_{REF} +0.3 volts. To detect a low level, the voltage on the capacitive-input line must be more negative than V_{REF} −0.5 volts.

outputs (Y1 through Y4)

The open-drain outputs are compatible with TMS 1000 type inputs. ISR controls the output multiplexer, which directs either the fixed input or the encoded capacitive inputs to the output buffer.

functional block diagram



typical keyboard interface

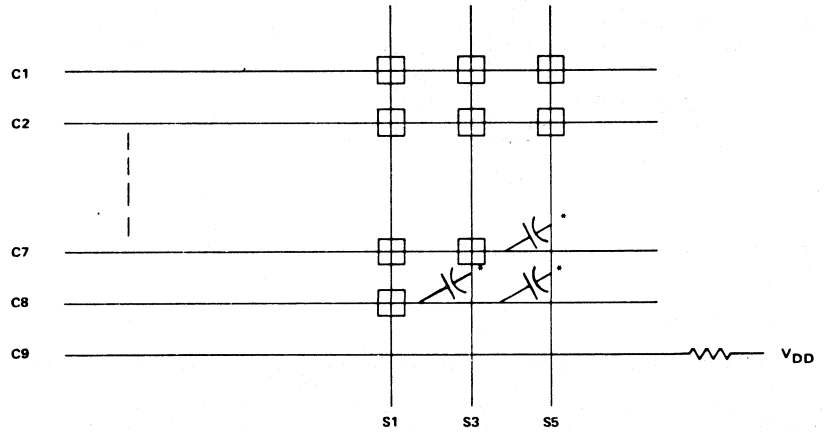
In a typical operation it is recommended that a buffer circuit be used to drive (scan) the capacitive keys. Application of a scan pulse when no key is touched generates transitions that are at least 0.5 volt more negative than the reference voltage causing all the latches to be set. Key touches will cause one or more of the latches to remain reset at a logic low, since the transition when a key is touched is more positive than the reference voltage. For multiplex operation the ratio of load-side stray capacitive to scanned-key capacitive is high, resulting in a low coupling ratio of output-to-input voltage. In order to make level detection as reliable as possible, the key-drive voltage should be large. Voltages in the −30- to −60-volt range are recommended. The voltage required is a function of key capacitance and number of keys scanned. The V_{REF} signal can be adjusted accordingly to detect the key pushes. The type of buffer/driver used depends on the switching characteristics of the scan signal. (Note that the input buffers are designed to detect negative transitions.) If the scan signal normally makes a positive transition to scan, then an inverting buffer should be used. A normally negative transition to scan requires a non-inverting buffer. The negative transition time will affect the voltage supplied to the capacitive inputs and, hence, the required drive voltage and the required reference voltage needed to detect the key touch. Fall times in the 500-ns range are sufficient.

typical keyboard interface (continued)

The stray capacitance on the input lines should be kept at a minimum and should not differ from one C-input line to another. Stray capacitance lowers the input level voltage, which increases the voltage required to drive the keyboard for accurate key detection. Coupling from adjacent lines must be minimized. PC board leakage on the input lines is critical and must be kept under 1 microampere at −1 volt. PC boards should be constructed so that contamination buildup during operation will not increase leakage beyond this limit.

Because of the common reference voltage used to sense key touches, the total capacitance on each of the input lines should be the same. In the case where the keyboard is an unbalanced array, that is, where there are a different number of keys on each input line, extra capacitors should be added to replace the missing keys. Figure 1 represents an example of an unbalanced array. Note that three key locations are unoccupied: crosspoints of C7-S5, C8-S3, and C8-S5. In order to assure the same relative input levels on all C input lines, external capacitors equal in value to the capacitance of one untouched key should be added to the C7 input while capacitors equal to two capacitive keys should be connected to the C8 input. These added capacitors must be scanned by the appropriate scan pulse. Unused C input lines must each be tied to V_{DD} through a resistor of approximately 100 kilohm.

Blank-key positions should always be positioned on the input line in the array of lowest priority as shown in Figure 1. Since a no-key position gives the indication that a key has been touched, any keys on the same scan line as the blank key but of lower priority will never be seen on the outputs. An alternative to this is to generate a dummy key. This can be accomplished by scanning a fixed capacitor tied to the input line and equal in magnitude to one untouched key. The scan line to be used is the same line used in the blank position.



*Under some conditions, if the scanning voltages are large and software is programmed to recognize blank-key spots, the external balancing capacitors can be omitted and replaced by resistors. However, it is recommended that they be included in all applications.

FIGURE 1 – CAPACITIVE KEYBOARD CROSSPOINTS

Figure 2 shows a possible system configuration using the TMS 1976 and one of the TMS 1000 series microcomputers. The capacitive inputs (C1 through C9) run directly from the capacitive-touch keyboard to the TMS 1976. The scan lines on this keyboard are activated by TMS 1000 R outputs through inverting drivers to provide correct polarity and

typical keyboard interface (continued)

sufficient drive voltage. Notice that the same R outputs used to scan the keyboard can also be used to scan the display. A 50- Hz source feeds the fixed input (F) to provide timing information for functions such as a clock or elapsed time indicator. No interface is required between the Y outputs of the TMS 1976 and the K inputs of the TMS 1000. The display is driven through a BCD-to-7-segment decoder thus making three O outputs available for additional control and indicator functions (such as the alarm output shown). Also note that since the ISR control directs F to only the Y1 output, additional functions can be wire-ORed to output lines Y2, Y3, Y4, and scanned by appropriate R lines during ISR high.

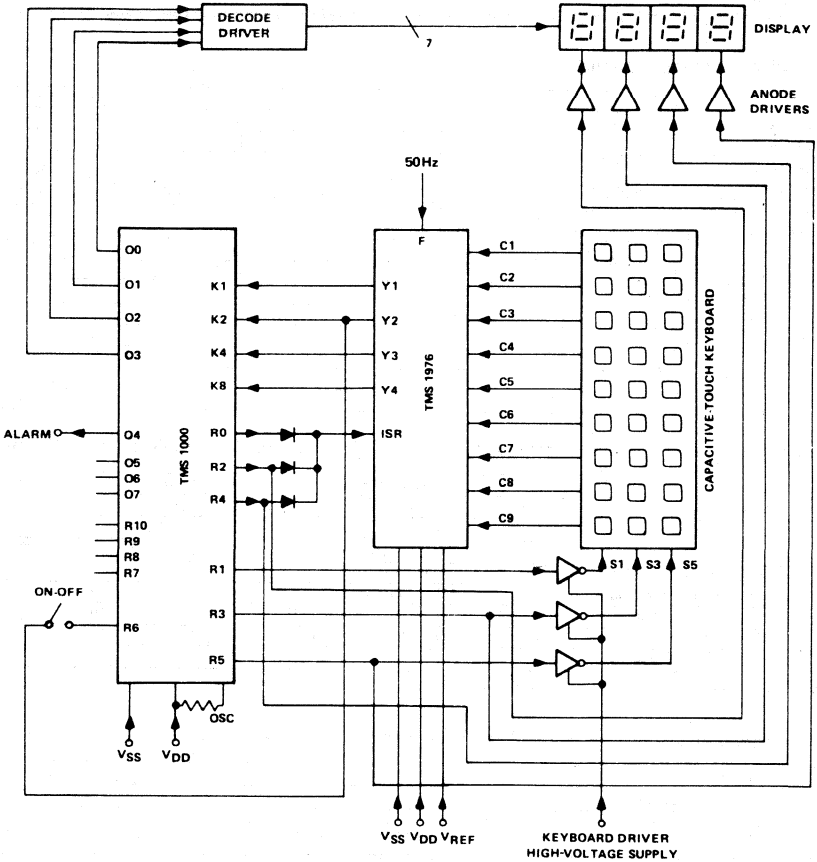


FIGURE 2 – TYPICAL SYSTEM CONFIGURATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Voltage applied to any device terminal (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Reference voltage, V_{REF} (see Note 1)	−20 V to 0.3 V
Input voltage (any input) (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE 1. Voltage values are with respect to V_{SS} (substrate).

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	−13	−15	−17.5	V
Supply voltage, V_{SS}		0		V
Reference voltage, V_{REF}	−3.5		V_{DD} +5	V
High-level fixed input voltage, V_{IH} (see Note 2)	−1.3	−0.8		V
High-level capacitive input voltage, V_{IH} (see Note 2)	V_{REF} +0.3			V
Low-level fixed input voltage, V_{IL} (see Note 2)			−4.5	V
Low-level capacitive input voltage, V_{IL} (see Note 2)		V_{REF}	−0.5	V
External leakage current on C inputs			1	μA
ISR pulse width (to reset C latches), $t_{w(ISR)}$	6			μs
Scan pulse width, $t_{w(S)}$	12			μs
Rise time, t_r		400	1000	μs
Fall time, t_f		400	1000	μs
Delay time, ISR to scan, $t_{d(ISR,S)}$	2			μs
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (see Note 2)	I_{OH} = −1 mA	−1			V
$I_{I(F)}$	F input current	V_I = 0 V	50	200	500	μA
I_{OL}	Low-level output current	$V_{OL} = V_{DD}$			−100	μA
$I_{DD(av)}$	Average supply current from V_{DD}	All outputs open		−1		mA
$P_{D(av)}$	Average power dissipation	All outputs open		15		mW
$C_{i(C)}$	Small-signal input capacitance, C input	V_I = 0 V, f = 1 kHz		10		pF
$C_{i(F)}$	Small-signal input capacitance, F input	V_I = 0 V, f = 1 kHz		10		pF
$r_{i(C)}$	Input resistance, C input	V_I = −1 V		1.5		MΩ

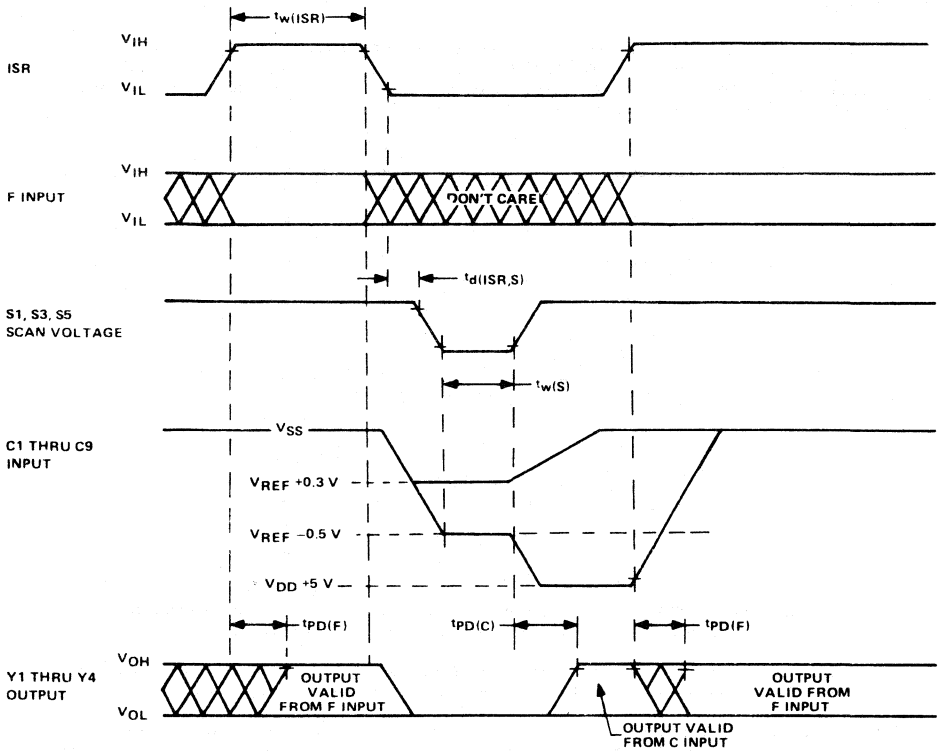
†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over full range of recommended operating conditions

	PARAMETER	MIN	MAX	UNIT
$t_{PD(C)}$	Propagation delay time from C input		2	μs
$t_{PD(F)}$	Propagation delay time from F input		4	μs

NOTE 2. The algebraic convention where the most-negative limit is designated as minimum is used in this specification for logic voltage levels only.

timing diagrams



NOTE: Timing points are 90% (high) and 10% (low).

6

1. INTRODUCTION

1.1 DESCRIPTION

The TMS 5501 is a multifunction input/output circuit for use with TI's TMS 8080 CPU. It is fabricated with the same N-channel silicon-gate process as the TMS 8080 and has compatible timing, signal levels, and power supply requirements. The TMS 5501 provides a TMS 8080 microprocessor system with an asynchronous communications interface, data I/O buffers, interrupt control logic, and interval timers.

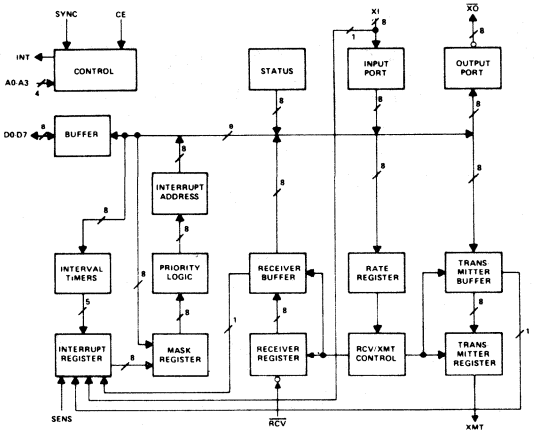


FIGURE 1–TMS 5501 BLOCK DIAGRAM

The I/O section of the TMS 5501 contains an eight-bit parallel input port and a separate eight-bit parallel output port with storage register. Five programmable interval timers provide time intervals from 64 μs to 16.32 ms.

The interrupt system allows the processor to effectively communicate with the interval timers, external signals, and the communications interface by providing TMS 8080-compatible interrupt logic with masking capability.

Data transfers between the TMS 5501 and the CPU are carried by the data bus and controlled by the interrupt, chip enable, sync, and address lines. The TMS 8080 uses four of its memory-address lines to select one of 14 commands to which the TMS 5501 will respond. These commands allow the CPU to:

- read the receiver buffer
- read the input port
- read the interrupt address
- read TMS 5501 status
- issue discrete commands
- load baud rate register
- load the transmitter buffer
- load the output port
- load the mask register
- load an interval timer

The commands are generated by executing memory referencing instructions such as MOV (register to memory) with the memory address being the TMS 5501 command. This provides a high degree of flexibility for I/O operations by letting the systems programmer use a variety of instructions.

1.2 SUMMARY OF OPERATION

Addressing the TMS 5501

A convenient method for addressing the TMS 5501 is to tie the chip enable input to the highest order address line of the CPU's 16-bit address bus and the four TMS 5501 address inputs to the four lowest order bits of the bus. This, of course, limits the system to 32,768 words of memory but in many applications the full 65,536 word memory addressing capability of the TMS 8080 is not required.

Communications Functions

The communications section of the TMS 5501 is an asynchronous transmitter and receiver for serial communications and provides the following functions:

Programmable baud rate – A CPU command selects a baud rate of 110, 150, 300, 1200, 2400, 4800, or 9600 baud.

Incoming character detection – The receiver detects the start and stop bits of an incoming character and places the character in the receive buffer.

Character transmission – The transmitter generates start and stop bits for a character received from the CPU and shifts it out.

Status and command signals – Via the data bus, the TMS 5501 signals the status of: framing error and overrun error flags; data in the receiver and transmitter buffers; start and data bit detectors; and end-of-transmission (break) signals from external equipment. It also issues break signals to external equipment.

Data Interface

The TMS 5501 moves data between the CPU and external devices through its internal data bus, input port, and output port. When data is present on the bus that is to be sent to an external device, a Load Output Port (LOP) command from the CPU puts the data on the $\overline{XO}$ pins of the TMS 5501 by latching it in the output port. The data remains in the port until another LOP command is received. When the CPU requires data that is present on the External Input (XI) lines, it issues a command that gates the data onto the internal data bus of the TMS 5501 and consequently onto the CPU's data bus at the correct time during the CPU cycles.

Interval Timers

To start a countdown by any of the five interval timers, the program selects the particular timer by an address to the TMS 5501 and loads the required interval into the timer via the data bus. Loading the timer activates it and it counts down in increments of 64 microseconds. The 8-bit counters provide intervals that vary in duration from 64 to 16,320 microseconds. Much longer intervals can be generated by cascading the timers through software. When a timer reaches zero, it generates an interrupt that typically will be used to point to a subroutine that performs a servicing function such as polling a peripheral or scanning a keyboard. Loading an interval value of zero causes an immediate interrupt. A new value loaded while the interval timer is counting overrides the previous value and the interval timer starts counting down the new interval. When an interval timer reaches zero it remains inactive until a new interval is loaded.

Servicing Interrupts

The TMS 5501 provides a TMS 8080 system with several interrupt control functions by receiving external interrupt signals, generating interrupt signals, masking out undersired interrupts, establishing the priority of interrupts, and generating RST instructions for the TMS 8080. An external interrupt is received on pin 22, SENS. An additional external interrupt can be received on pin 32, XI7, if selected by a discrete command from the TMS 8080 (See Figure 4). The TMS 5501 generates an interrupt when any of the five interval timers count to zero. Interrupts are also generated when the receiver buffer is loaded and when the transmitter buffer is empty.

When an interrupt signal is received by the interrupt register from a particular source, a corresponding bit is set and gated to the mask register. A pattern will have previously been set in the mask register by a load-mask-register command from the TMS 8080. This pattern determines which interrupts will pass through to the priority logic. The priority logic allows an interrupt to generate an RST instruction to the TMS 8080 only if there is no higher priority interrupt that has not been accepted by the TMS 8080. The TMS 5501 prioritizes interrupts in the order shown below:

1st – Interval Timer #1
2nd – Interval Timer #2
3rd – External Sensor
4th – Interval Timer #3
5th – Receiver Buffer Loaded
6th – Transmitter Buffer Emptied
7th – Interval Timer #4
8th – Interval Timer #5 or an External Input (XI 7)

The highest priority interrupt passes through to the interrupt address logic, which generates the RST instruction to be read by the TMS 8080. See Table 3 for relationship of interrupt sources to RST instructions and Figures 6 and 8 for timing relationships.

The TMS 5501 provides two methods of servicing interrupts; an interrupt-driven system or a polled-interrupt system. In an interrupt-driven system, the INT signal of the TMS 5501 is tied to the INT input of the TMS 8080. The sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt signal and readies the appropriate RST instruction. (2) The TMS 5501 INT output, tied to the TMS 8080 INT input, goes high signaling the TMS 8080 that an interrupt has occured. (3) If the TMS 8080 is enabled to accept interrupts, it sets the INTA (interrupt acknowledge) status bit high at SYNC time of the next machine cycle. (4) If the TMS 5501 has previously received an interrupt-acknowledge-enable command from the CPU (see Bit 3, Paragraph 2.2.5), the RST instruction is transferred to the data bus.

In a polled-interrupt system, INT is not used and the sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt and readies the RST instruction. (2) The TMS 5501 interrupt-pending status bit (see Bit 5, Paragraph 2.2.4) is set high (the interrupt-pending status bit and the INT output go high simultaneously). (3) At the prescribed time, the TMS 8080 polls the TMS 5501 to see if an interrupt has occurred by issuing a read-TMS 5501-status command and reading the interrupt-pending bit. (4) If the bit is high, the TMS 8080 will then issue a read-interrupt-address command, which causes the TMS 5501 to transfer the RST instruction to the data bus as data for the instruction being executed by the TMS 8080.

1.3 APPLICATIONS

Communications Terminals

The functions of the TMS 5501 make it particularly useful in TMS 8080-based communications terminals and generally applicable in systems requiring periodic or random servicing of interrupts, generation of control signals to external devices, buffering of data, and transmission and reception of asynchronous serial data. As an example, a system configuration such as shown in Figure 2 can function as the controller for a terminal that governs employee entrance into a plant or security areas within a plant. Each terminal is identified by a central computer through ID switches. The central system supplies each terminal's RAM with up to 16 employee access categories applicable to that terminal. These categories are compared with an employee's badge character when he inserts his badge into the badge sensor. If a

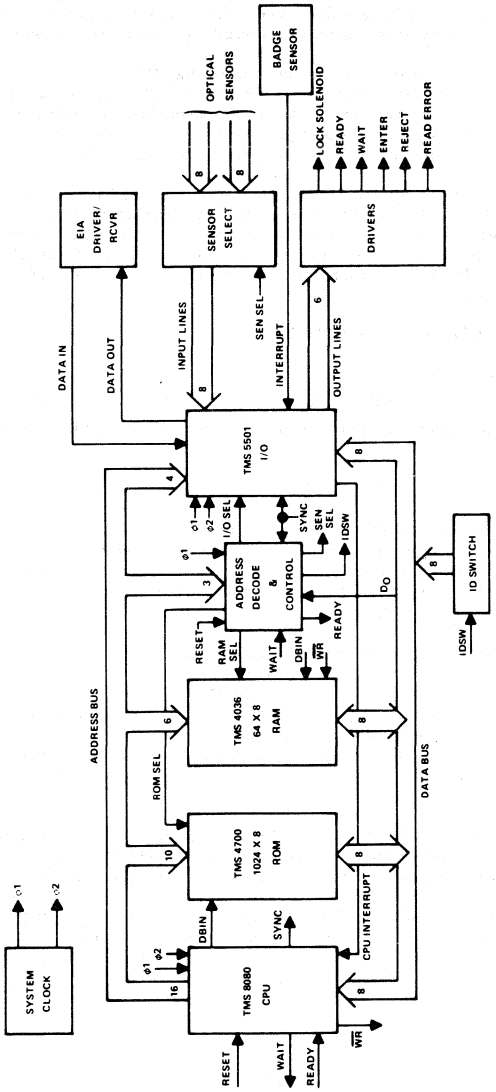


FIGURE 2–ACCESS CONTROL SYSTEM BLOCK DIAGRAM

match is not found, a reject light will be activated. If a match is found, the terminal will transmit the employee's badge number and access category to the central system, and a door unlock solenoid will be activated for 4 seconds. The central computer then may take the transmitted information and record it along with time and date of access.

The TMS 4700 is a 1024 x 8 ROM that contains the system program, and the TMS 4036 is a 64 x 8 RAM that serves as the stack for the TMS 8080 and storage for the access category information. TTL circuits control chip-enable information carried by the address bus. Signals from the CPU gate the address bits from the ROM, the RAM, or the TMS 5501 onto the data bus at the correct time in the CPU cycle. The clock generator consists of four TTL circuits along with a crystal, needed to maintain accurate serial data assembly and disassembly with the central computer.

The TMS 5501 handles the asynchronous serial communication between the TMS 8080 and the central system and gates data from the badge reader onto the data bus. It also gates control and status data from the TMS 8080 to the door lock and badge reader and controls the time that the door lock remains open. The TMS 5501 signals the TMS 8080 when the badge reader or the communication lines need service. The functions that the TMS 5501 is to perform are selected by an address from the TMS 8080 with the highest order address line tied to the TMS 5501 chip enable input and the four lowest order lines tied to the address inputs.

2. OPERATIONAL AND FUNCTIONAL DESCRIPTION

This detailed description of the TMS 5501 consists of:

INTERFACE SIGNALS – a definition of each of the circuit's external connections

COMMANDS – the address required to select each of the TMS 5501 commands and a description of the response to the command.

2.1 INTERFACE SIGNALS

The TMS 5501 communicates with the TMS 8080 via four address lines: a chip enable line, an eight-bit bidirectional data bus, an interrupt line, and a sync line. It communicates with system components other than the CPU via eight external inputs, eight external outputs, a serial receiver input, a serial transmitter output, and an external sensor input. Table 1 defines the TMS 5501 pin assignments and describes the function of each pin.

TABLE 1
TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION
		INPUTS
CE	18	Chip enable—When CE is low, the TMS 5501 address decoding is inhibited, which prevents execution of any of the TMS 5501 commands.
A3	17	Address bus—A3 through A0 are the lines that are addressed by the TMS 8080 to select a particular
A2	16	TMS 5501 function.
A1	15	
A0	14	
SYNC	19	Synchronizing signal—The SYNC signal is issued by the TMS 8080 and indicates the beginning of a machine cycle and availability of machine status. When the SYNC signal is active (high), the TMS 5501 will monitor the data bus bits DO (interrupt acknowledge) and D1 ($\overline{WO}$, data output function).
$\overline{RCV}$	5	Receiver serial data input line—$\overline{RCV}$ must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receive circuitry.

TABLE 1 (continued)
TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION
		INPUTS
XI 0	39	External inputs—These eight external inputs are gated to the data bus when the read-external-inputs function is addressed. External input n is gated to data bus bit n without conversion.
XI 1	38	
XI 2	37	
XI 3	36	
XI 4	35	
XI 5	34	
XI 6	33	
XI 7	32	
SENS	22	External interrupt sensing — A transition from low to high at SENS sets a bit in the interrupt register, which, if enabled, generates an interrupt to the TMS 8080.
		OUTPUTS
$\overline{XO}$ 0	24	External outputs—These eight external outputs are driven by the complement of the output register; i.e., if output register bit n is loaded with a high (low) from data bus bit n by a load-output register command, the external output n will be a low (high). The external outputs change only when a load-output-register function is addressed.
$\overline{XO}$ 1	25	
$\overline{XO}$ 2	26	
$\overline{XO}$ 3	27	
$\overline{XO}$ 4	28	
$\overline{XO}$ 5	29	
$\overline{XO}$ 6	30	
$\overline{XO}$ 7	31	
XMT	40	Transmitter serial data output line—This line remains high when the TMS 5501 is not transmitting.
		DATA BUS INPUT/OUTPUT
D0	13	Data bus — Data transfers between the TMS 5501 and the TMS 8080 are made via the 8-bit bidirectional data bus. D0 is the LSB. D7 is the MSB.
D1	12	
D2	11	
D3	10	
D4	9	
D5	8	
D6	7	
D7	6	
INT	23	Interrupt—When active (high), the INT output indicates that at least one of the interrupt conditions has occurred and that its corresponding mask-register bit is set.
		POWER AND CLOCKS
V_{SS}	4	Ground reference
V_{BB}	1	Supply voltage (−5 V nominal)
V_{CC}	2	Supply voltage (5 V nominal)
V_{DD}	3	Supply voltage (12 V nominal)
$\phi 1$	20	Phase 1 clock
$\phi 2$	21	Phase 2 clock

6

2.2 TMS 5501 COMMANDS

The TMS 5501 operates as memory device for the TMS 8080. Functions are initiated via the TMS 8080 address bus and the TMS 5501 address inputs. Address decoding to determine the command function being issued is defined in Table 2.

TABLE 2
COMMAND ADDRESS DECODING
When Chip Enable Is High

A3	A2	A1	A0	COMMAND	FUNCTION	PARAGRAPH
L	L	L	L	Read receiver buffer	RBn → Dn	2.2.1
L	L	L	H	Read external inputs	XIn → Dn	2.2.2
L	L	H	L	Read interrupt address	RST → Dn	2.2.3
L	L	H	H	Read TMS 5501 status	(Status) → Dn	2.2.4
L	H	L	L	Issue discrete commands	See Figure 4	2.2.5
L	H	L	H	Load rate register	See Figure 4	2.2.6
L	H	H	L	Load transmitter buffer	Dn → TBn	2.2.7
L	H	H	H	Load output port	Dn → $\overline{XO}$n	2.2.8
H	L	L	L	Load mask register	Dn → MRn	2.2.9
H	L	L	H	Load interval timer 1	Dn → Timer 1	2.2.10
H	L	H	L	Load interval timer 2	Dn → Timer 2	2.2.10
H	L	H	H	Load interval timer 3	Dn → Timer 3	2.2.10
H	H	L	L	Load interval timer 4	Dn → Timer 4	2.2.10
H	H	L	H	Load interval timer 5	Dn → Timer 5	2.2.10
H	H	H	L	No function		
H	H	H	H	No function		

RBn Receiver buffer bit n
Dn Data bus I/O terminal n
XIn External input terminal n
RST 11 (IA_2) (IA_1) (IA_0) 1 1 1 (see Table 3)
TBn Transmit buffer bit n
$\overline{XO}$n Output register bit n
MRn Mask register bit n

TABLE 3
RST INSTRUCTIONS

DATA BUS BIT								INTERRUPT CAUSED BY
0	1	2	3	4	5	6	7	
H	H	H	L	L	L	H	H	Interval Timer 1
H	H	H	H	L	L	H	H	Interval Timer 2
H	H	H	L	H	L	H	H	External Sensor
H	H	H	H	H	L	H	H	Interval Timer 3
H	H	H	L	L	H	H	H	Receiver Buffer
H	H	H	H	L	H	H	H	Transmitter Buffer
H	H	H	L	H	H	H	H	Interval Timer 4
H	H	H	H	H	H	H	H	Interval Timer 5 or X17

The following paragraphs define the functions of the TMS 5501 commands.

2.2.1 Read receiver buffer

Addressing the read-receiver-buffer function causes the receiver buffer contents to be transferred to the TMS 8080 and clears the receiver-buffer-loaded flag.

2.2.2 Read external input lines

Addressing the read-external-inputs function transfers the states of the eight external input lines to the TMS 8080.

2.2.3 Read interrupt address

Addressing the read interrupt address function transfers the current highest priority interrupt address onto the data bus as read data. After the read operation is completed, the corresponding bit in the interrupt register is reset.

If the read-interrupt-address function is addressed when there is no interrupt pending, a false interrupt address will be read. TMS 5501 status function should be addressed in order to determine whether or not an interrupt condition is pending.

2.2.4 Read TMS 5501 status

Addressing the read-TMS 5501-status function gates the various status conditions of the TMS 5501 onto the data bus. The status conditions, available as indicated in Figure 3, are described in the following paragraphs.

BIT:	7	6	5	4	3	2	1	0
	START BIT DETECT	FULL BIT DETECT	INTRPT PENDING	XMIT BUFFER EMPTY	RCV BUFFER LOADED	SERIAL RCVD	OVERRUN ERROR	FRAME ERROR

FIGURE 3–DATA BUS ASSIGNMENTS FOR TMS 5501 STATUS

Bit 0, framing error

A high in bit 0 indicates that a framing error was detected on the last character received (either one or both stop bits were in error). The framing error flag is updated at the end of each character. Bit 0 of the TMS 5501 status will remain high until the next valid character is received.

Bit 1, overrun error

A high in bit 1 indicates that a new character was loaded into the receiver buffer before a previous character was read out. The overrun error flag is cleared each time the read-I/O-status function is addressed or a reset command is issued.

Bit 2, serial received data

Bit 2 monitors the receiver serial data input line. This line is provided as a status input for use in detecting a break and for test purposes. Bit 2 is normally high when no data is being received.

Bit 3, receiver buffer loaded

A high in bit 3 indiciates that the receiver buffer is loaded with a new character. The receiver-buffer-loaded flag remains high until the read-receiver-buffer function is addressed (at which time the flag is cleared). The reset function also clears this flag.

Bit 4, transmitter buffer empty
A high in bit 4 indicates that the transmitter buffer register is empty and ready to accept a character. Note, however, that the serial transmitter register may be in the process of shifting out a character. The reset function sets the transmitter-buffer-empty flag high.

Bit 5, interrupt pending
A high in bit 5 indicates that one or more of the interrupt conditions has occured and the corresponding interrupt is enabled. This bit is the status of the interrupt signal INT.

Bit 6, full bit detected
A high in bit 6 indicates that the first data bit of a receive-data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

Bit 7, start bit detected
A high in bit 7 indicates that the start bit of an incoming data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

2.2.5 Issue discrete commands

Addressing the discrete command function causes the TMS 5501 to interpret the data bus information according to the following descriptions. See Figure 4 for the discrete command format. Bits 1 through 5 are latched until a different discrete command is received.

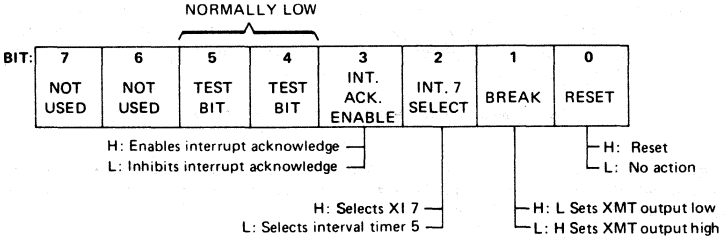


FIGURE 4–DISCRETE COMMAND FORMAT

Bit 0, reset
A high in bit 0 will cause the following:

1) The receiver buffer and register are cleared to the search mode including the receiver-buffer-loaded flag, the start-bit-detected flag, the full-bit-detected flag, and the overrun-error flag. The receiver buffer is not cleared and will contain the last character received.
2) The transmitter data output is set high (marking). The transmitter-buffer-empty flag is set high indicating that the transmitter buffer is ready to accept a character from the TMS 8080.
3) The interrupt register is cleared except for the bit corresponding to the transmitter buffer interrupt, which is set high.
4) The interval timers are inhibited.

A low in bit 0 causes no action. The reset function has no affect on the output port, the external inputs, interrupt acknowledge enable, the mask register, the rate register, the transmitter register, or the transmitter buffer.

Bit 1, break
A low in bit 1 causes the transmitter data output to be reset low (spacing).

If bit 0 and bit 1 are both high, the reset function will override.

Bit 2, interrupt 7 select
Interrupt 7 may be generated either by a low to high transition of external input 7 or by interval timer 5.

A high in bit 2 selects the interrupt 7 source to be the transition of external input 7. A low in bit 2 selects the interrupt 7 source to be interval timer 5.

Bit 3, interrupt acknowledge enable
The TMS 5501 decodes data bus (CPU status) bit 0 at SYNC of each machine cycle to determine if an interrupt acknowledge is being issued.

A high in bit 3 enables the TMS 5501 to accept the interrupt acknowledge decode. A low in bit 3 causes the TMS 5501 to ignore the interrupt acknowledge decode.

Bit 4 and bit 5 are used only during testing of the TMS 5501. For correct system operation both bits must be kept low.

Bit 6 and bit 7 are not used and can assume any value.

2.2.6 Load rate register

Addressing the load-rate-register function causes the TMS 5501 to load the rate register from the data bus and interpret the data bits (See Figure 5) as follows.

BIT:	7	6	5	4	3	2	1	0
	STOP BIT(s)	9600 baud	4800 baud	2400 baud	1200 baud	300 baud	150 baud	110 baud

H: One stop bit
L: Two stop bits

FIGURE 5—DATA BUS ASSIGNMENTS FOR RATE COMMANDS

Bits 0 through 6, rate select

The rate select bits (bits 0 through 6) are mutually exclusive, i.e., only one bit may be high. A high in bits 0 through 6 will select the baud rate for both the transmitter and receiver circuitry as defined below and in Figure 5:

Bit 0 110 baud
Bit 1 150 baud
Bit 2 300 baud
Bit 3 1200 baud
Bit 4 2400 baud
Bit 5 4800 baud
Bit 6 9600 baud

If more than one bit is high, the highest rate indicated will result. If bits 0 through 6 are all low, both the receiver and the transmitter circuitry will be inhibited.

Bit 7, stop bits

Bit 7 determines whether one or two stop bits are to be used by both the transmitter and receiver circuitry. A high in bit 7 selects one stop bit. A low in bit 7 selects two stop bits.

2.2.7 Load transmitter buffer

Addressing the load-transmitter-buffer function transfers the state of the data bus into the transmitter buffer.

2.2.8 Load output port

Addressing the load-output-port function transfers the state of the data bus into the output port. The data is latched and remains on $\overline{XO\ 0}$ through $\overline{XO\ 7}$ as the complement of the data bus until new data is loaded.

2.2.9 Load mask register

Addressing the load-mask-register function loads the contents of the data bus into the mask register. A high in data bus bit n enables interrupt n. A low inhibits the corresponding interrupt.

2.2.10 Load timer n

Addressing the load-timer-n function loads the contents of the data bus into the appropriate interval timer. Time intervals of from 64 μs (data bus = LLLLLLLH) to 16,320 μs (data bus HHHHHHHH) are counted in 64-μs, steps. When the count of interval timer n reaches 0, the bit in the interrupt register that corresponds to timer n is set and an interrupt is generated. Loading all lows causes an interrupt immediately.

3. TMS 5501 ELECTRICAL AND MECHANICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1	−0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 V to 20 V
All input and output voltages (see Note 1)	−0.3 V to 20 V
Continuous power dissipation	1.1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{SS} unless otherwise noted.

3.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (all inputs except clocks)	3.3		V_{CC}+1	V
High-level clock input voltage, $V_{IH(\phi)}$	V_{DD}−1		V_{DD}+1	V
Low-level input voltage, V_{IL} (all inputs except clocks) (see Note 2)	−1		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 2)	−1		0.6	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only.

3.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_I	Input current (any input except clocks and data bus)	V_I = 0 V to V_{CC}		±10	μA
$I_{I(\phi)}$	Clock input current	$V_{I(\phi)}$ = 0 V to V_{DD}		±10	μA
$I_{I(DB)}$	Input current, data bus	$V_{I(DB)}$ = 0 V to V_{CC}, CE at 0 V		−100	μA
V_{OH}	High-level output voltage	I_{OH} = 400 μA	3.7		V
V_{OL}	Low-level output voltage	I_{OL} = 1.7 mA,		0.45	V
$I_{BB(av)}$	Average supply current from V_{BB}	Operating at $t_{c(\phi)}$ = 480 ns, T_A = 25 C		−1	mA
$I_{CC(av)}$	Average supply current from V_{CC}			100	mA
$I_{DD(av)}$	Average supply current from V_{DD}			40	mA
C_i	Capacitance, any input except clock	V_{CC} = V_{DD} = V_{SS} = 0 V, V_{BB} = −4.75 to −5.25 V, f = 1 MHz, All other pins at 0 V		10	pF
$C_{I(\phi)}$	Clock input capacitance			75	pF
C_o	Output capacitance			20	pF

3.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 5 AND 6)

		MIN	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time	480	2000	ns
$t_{r(\phi)}$	Clock rise time	5	50	ns
$t_{f(\phi)}$	Clock fall time	5	50	ns
$t_{w(\phi 1)}$	Pulse width, clock 1 high	60		ns
$t_{w(\phi 2)}$	Pulse width, clock 2 high	200	300	ns
$t_{d(\phi 1L\text{-}\phi 2)}$	Delay time, clock 1 low to clock 2	0		ns
$t_{d(\phi 2\text{-}\phi 1)}$	Delay time, clock 2 to clock 1	70		ns
$t_{d(\phi 1H\text{-}\phi 2)}$	Delay time, clock 1 high to clock 2 (time between leading edges)	130		ns
$t_{su(ad)}$	Address setup time	50		ns
$t_{su(CE)}$	Chip-enable setup time	50		ns
$t_{su(da)}$	Data setup time	50		ns
$t_{su(sync)}$	Sync setup time	50		ns
$t_{su(XI)}$	External input setup time	50		ns
$t_{h(ad)}$	Address hold time	0		ns
$t_{h(CE)}$	Chip-enable hold time	10		ns
$t_{h(da)}$	Data hold time	10		ns
$t_{h(sync)}$	Sync hold time	10		ns
$t_{h(XI)}$	External input hold time	40		ns
$t_{w(sens\ H)}$	Pulse width, sensor input high	500		ns
$t_{w(sens\ L)}$	Pulse width, sensor input low	500		ns
$t_{d(sens\text{-}int)}$	Delay time, sensor to interrupt (time between leading edges)		2000	ns
$t_{d(rst\text{-}int)}$	Delay time, RST instruction to interrupt (time between trailing edges)		500	ns

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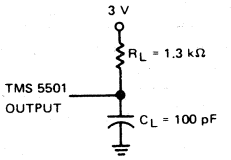
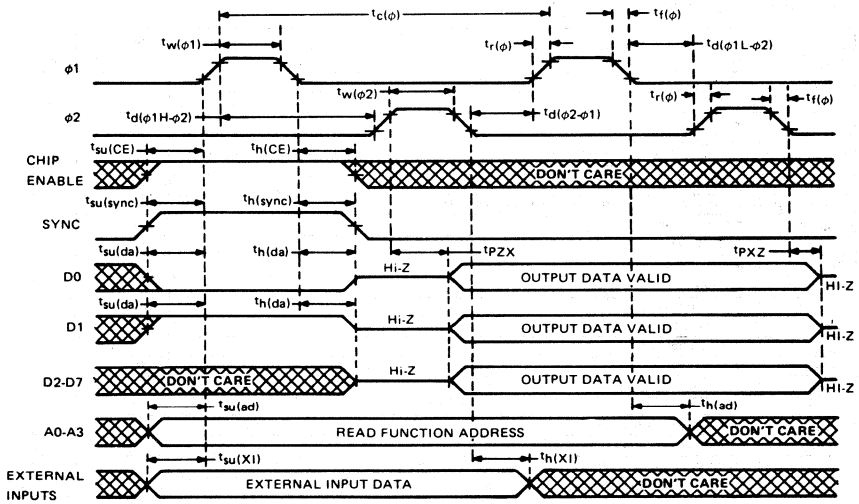
3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 6 AND 7)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PZX}	Data bus output enable time	C_L = 100 pF, R_L = 1.3 kΩ		200	ns
t_{PXZ}	Data bus output disable time to high-impedance state			180	ns
t_{PD}	External data output propagation delay time from φ2			200	ns



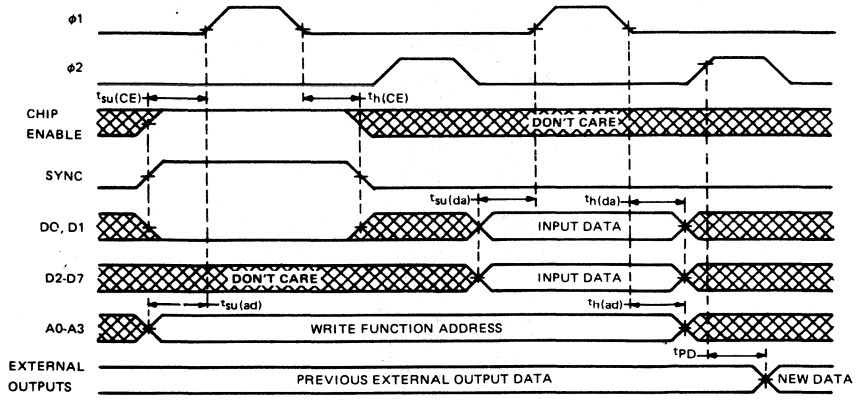
C_L includes probe and jig capacitance

LOAD CIRCUIT



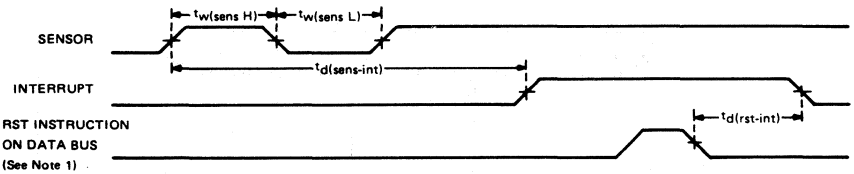
NOTE: For φ1 or φ2 inputs, high and low timing points are 90% and 10% of $V_{IH(\phi)}$. All other timing points are the 50% level.

FIGURE 6–READ CYCLE TIMING



NOTE: For φ1 and φ2 inputs, high and low timing points are 90% and 10% of $V_{IH(\phi)}$. All other timing points are the 50% level.

FIGURE 7—WRITE CYCLE TIMING

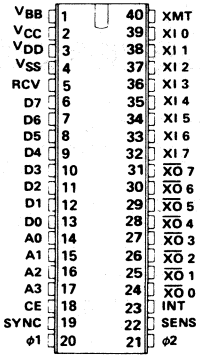


NOTES: 1. The RST instruction occurs during the output data valid time of the read cycle.
2. All timing points are 50% of V_{IH}.

FIGURE 8—SENSOR/INTERRUPT TIMING

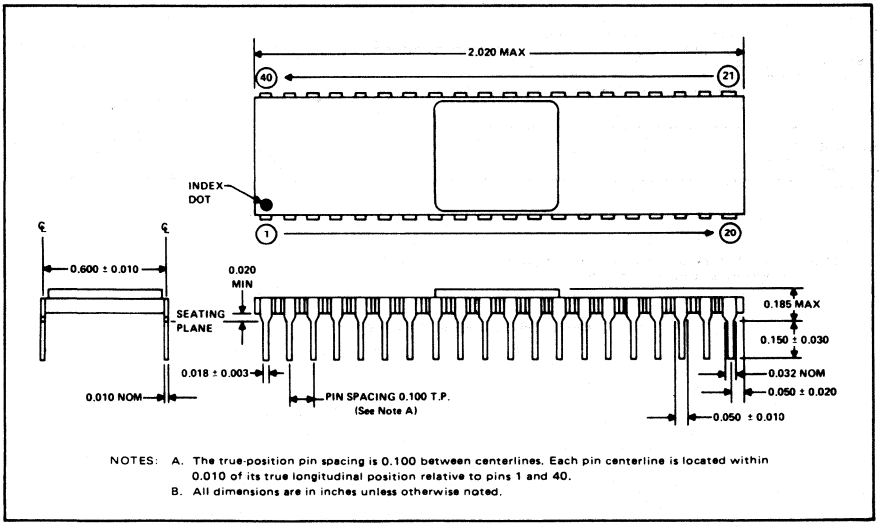
3.6 TERMINAL ASSIGNMENTS

TMS 5501

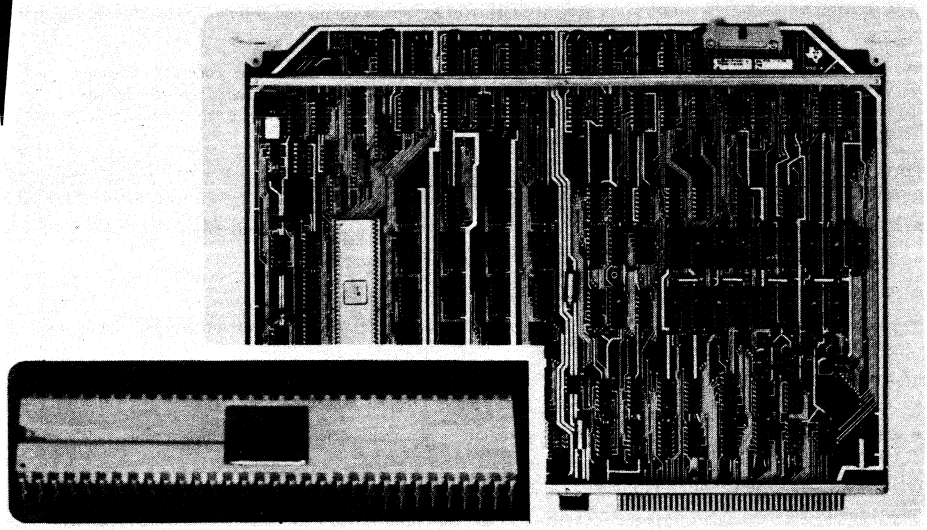


3.7 MECHANICAL DATA

40-PIN CERAMIC PACKAGE



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 40.
B. All dimensions are in inches unless otherwise noted.



TMS 9900 Microprocessor (Left) and TI 990/4 Microcomputer (Right)

The TI 990 prototyping system provides for effective development of applications programs for users of the TMS 9900 microprocessor and Model 990/4 microcomputer. High performance and ease of operation, coupled with low cost, make the system ideal for development of software and firmwave modules to replace electro-mechanical devices, discrete logic or conventional integrated circuits.

Housed in a compact tabletop cabinet, the basis of the prototyping system is the 990/4 computer on a board. The memory features include 16K bytes of read/write random access memory (RAM) for both the system and the user software storage, and 512 bytes of read only memory (ROM) which provides nondestructible storage of 733 ASR load software and 990/4 self-testing diagnostic software.

The prototyping system includes a comprehensive programming panel, *Silent 700** Model 733 ASR Twin Cassette Data Terminal, and power supply. An optional flexible PROM Programming Module provides users of the TMS 9900 and 990/4 the capability to implement their application software in nondestructible (erasable or permanent) programmable read only memory (EROM or PROM).

The prototyping system memory can be expanded to a total of 64K bytes using a combination of dynamic RAM and EROM. An optional battery pack is available to prevent memory loss of dynamic RAM during removal of main power.

A comprehensive software package, supplied with the prototyping system permits the user to generate, edit, assemble, and evaluate programs for the TMS 9900 and 990/4. The standard software includes a debug monitor, which combines a powerful interactive debugging facility with system support functions, and a keyboard command interpreter for full user control of the system. A cassette-based source editor operates under control of the debug monitor and provides a facility that enables the user to generate, edit, and save source programs. A unique one-pass assembler processes source input from cassettes and generates relocatable, linkable object modules. A link editor accepts object modules generated by the assembler (or 9900 cross-support systems) and loads them into memory as an executable program. The user may then execute the program directly or under the control of the debug monitor. With the debug monitor, the user can examine and modify parts of memory and registers, set multiple breakpoints and, if necessary, execute with a complete trace.

THE TI990 PROTOTYPING SYSTEM

A completed program may be saved on cassette for production of ROM masks or may be directly burned into PROM with the optional PROM programming unit.

The prototyping system provides the flexibility required to support software development from concept through implementation. It is suitable as a standalone system or can be used in conjunction with a cross-support system available on time sharing networks. The prototyping system serves as a mechanism for development of software and firmware modules for the TMS 9900 microprocessor and the 990/4 microcomputer.

HARDWARE

- 990/4 microcomputer in an attractive tabletop enclosure.
- Memory featuring: 16K bytes of dynamic RAM, 1024 bytes of ROM and 512 bytes of static RAM.
- Read Only Memory (ROM) containing 733 ASR Loader and CPU self-testing capability.
- Programmer panel to augment system control and monitoring.
- System available with either a Model 733 ASR data terminal kit or with the Model 733 ASR interface only for users who currently have a 733 ASR with designated options.

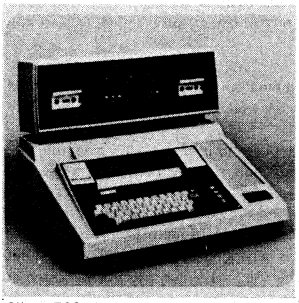
SOFTWARE

- *Debug monitor* for full control of the prototyping system during program development.
- *One-pass assembler* to convert source code stored on cassette to relocatable object. (Object is upward compatible with other 990 series assemblers).
- *Linking loader* capable of loading absolute or relocatable object and performing required reference linkages.
- *Source editor* to allow user modification of both source and object from cassette with resultant storage on cassette.
- *Trace routine* to enable the user to monitor status of computer at completion of each instruction.
- *PROM programming/documentation facility* to provide documentation for ROM mask generation or to communicate directly with the optional PROM programming unit.

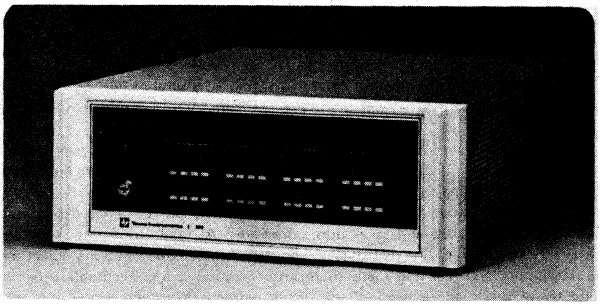
OPTIONAL FEATURES

- Battery pack to prevent memory loss when power is off.
- Additional memory capacity to a total of 64K bytes RAM and PROM.
- Optional external PROM programming unit capable of system-controlled programming and verification of the following TI PROMs: SN74S287, SN74S471, and SN74S472.

Texas Instruments provides a full range of support for the TI 9900 computer family, including a nationwide sales and service network; full documentation; user training programs; lease and purchase plans; and applications assistance.

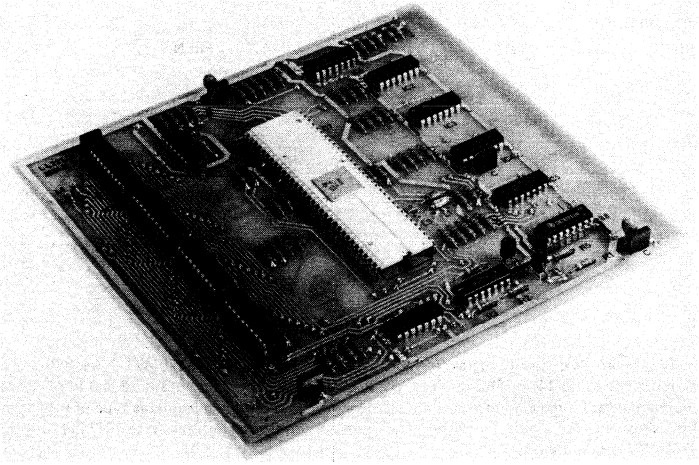


Silent 700 Model 733 Electronic Data Terminal



TI 990/4 Tabletop Model

LL221 MICROCOMPUTER/TMS1000 DEVELOPMENT SYSTEM PRINTED CIRCUIT BOARD



Description

The LL221 printed circuit board is a micro computer system specifically designed for the Texas Instruments TMS1099 Microprocessor device. The system uses the TMS1099 as the Central Processor Unit (CPU), with TTL Programmable Read Only Memories (PROMs) for program store and output coding. An SN74S188 PROM converts the five data outputs from the CPU to eight output lines and either four SN74S471 PROMs (256 x 8) or two SN74S472 PROMs (512 x 8) are used to give 1024 words x 8 bits of program memory. Alternatively, the Texas Instruments ROMSYN ROM simulator system can be plugged into a socket on the board and be used as the program memory, thus simplifying program development.

All system data inputs and outputs, including the thirteen steady state outputs, are TTL buffered and there is provision to either use the on-chip clock oscillator of the TMS1099 by connecting link 'L2', or alternatively to drive the system from an external clock source at TTL level, by connecting link L3 instead of L2, and replacing or shorting C1 with link L1. The system is on a single 168 x 158 mm (6.6" x 6.2") p.c.b. with a 60 way 2.54 mm (0.1") pitch gold plated edge connector.

When fully populated with program memory, the system is identical in function and organisation with the Texas Instruments TMS1000 micro-computer device, and is extremely useful as a TMS1000 program development tool, as well as being a complete system in its own right.

Operation

The overall operation of the system is specified in the TMS1000 and TMS1099 data and programming literature. The SN74S188/288 PROM replaces the output Programmable Logic Array (PLA) of the TMS1000 and is addressed as shown in the TMS1099 data sheet. The outputs from this device are connected directly to the output pins of the system.

The integrated circuits forming the program memory occupy positions IC14, IC13, IC12, IC11 on the p.c.b. Position IC14 has all the 'true' addresses supplied to it from the TMS1099 Page Address and Program Counter outputs, and hence the TI ROMSYM can be connected into this position. The addressing of these four device locations is shown in Table 1.

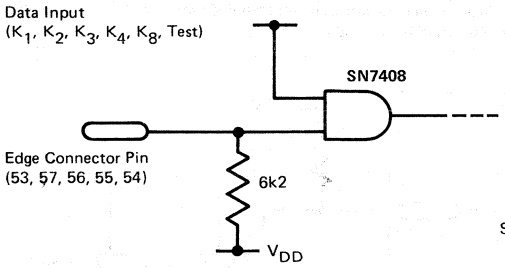
TMS1099 Output	IC14 Pin No	IC13 Pin No	IC12 Pin No	IC11 Pin No
PA0	15	–	15	–
PA0	–	15	–	15
PA1	16	16	–	–
PA1	–	–	16	16
PA2	19	19	19	19
PA3	18	18	18	18
PC0	17	17	17	17
PC1	5	5	5	5
PC2	4	4	4	4
PC3	3	3	3	3
PC4	2	2	2	2
PC5	1	1	1	1

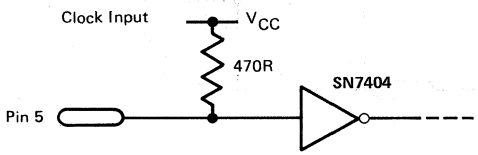
The 1024 words x 8 bits of program memory can be made up of SN74S470/471 256 x 8 Proms in all four locations (IC11-14) or SN74S472/3 512 x 8 PROMs only in locations IC13 and IC14. It should be noted that care is required in programming these devices if changing from one type of PROM to the other, since address inputs F, G and H are not on corresponding pins. (See SN74S470/471 and SN74S472/473 data sheets).

Recommended Operating Conditions

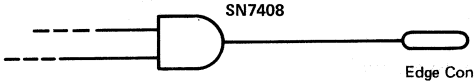
PARAMETER	MIN	NOM	MAX	UNITS
Supply Voltage V_{DD}	−9	−10	−12.5	V
Supply Voltage V_{CC}	+4.5	+5.0	+5.5	V

TYPICAL INPUT/OUTPUT CIRCUITS

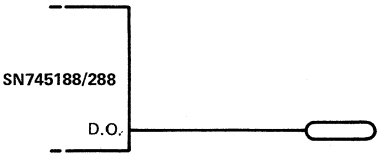




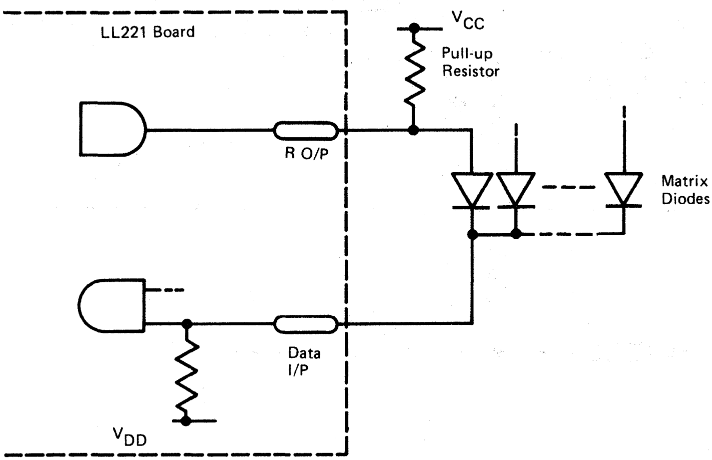
'R' Output



'O' Data Output



NOTE 1. The data inputs are normally 'low' as in the case with the TMS1000 device. By using pull-up resistors to V_{CC} of between 330 ohm and 820 ohm on the 'R' outputs, the latter can drive the data inputs directly. If a diode is included in this connection for scanning switch matrix applications, then the pull-up resistor should be between 330 ohm and 620 ohm.

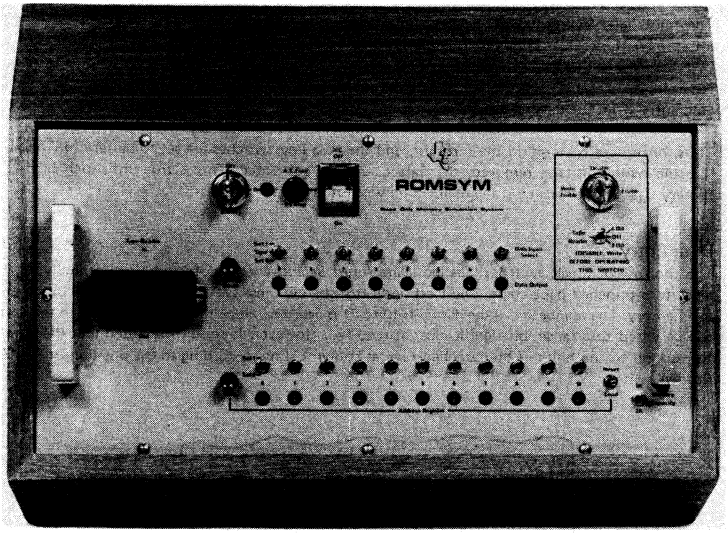


NOTE 2. For 'Power Up' initialisation of the system the 'test' input (edge connector pin 54) should be held at a logic high level for a minimum of six clock periods.

Edge Connector Pin Assignments

Pin	Signal
60	DV
59	VCC
58	VDD
57	K2
56	K4
55	K8
54	Test
53	K1
52	
51	
50	
49	R12
48	R11
47	R10
46	
45	
44	
43	
42	
41	R9
40	R8
39	R7
38	R6
37	
36	
35	
34	
33	
32	R5
31	R4
30	R3
29	R2
28	
27	
26	
25	
24	
23	
22	R1
21	R0
20	
19	
18	
17	
16	
15	DO 8
14	DO 1
13	DO 2
12	DO 3
11	DO 4
10	DO 7
9	DO 6
8	DO 5
7	
6	
5	Clock
4	
3	
2	VCC
1	

ROMSYM–READ ONLY MEMORY SIMULATION SYSTEM



The TI ROMSYM is a system specifically designed to simulate the function of ROMs and PROMs as program memory in microprocessor systems. However, it is equally suitable for use in many other applications.

Features

- 1k words x 8 bits memory available as standard.
- Can be ordered with 2k x 8 memory, or upgraded to this capacity.
- 500ns access/cycle time, compatible with most microprocessor requirements.
- Non volatile. Contains auto-operating back-up battery supply to protect program against mains failure. 192 hrs. min. storage for 8k bits. 96 hrs. min. storage for 16k bits.
- Two methods of data entry. A comprehensive programmer's panel and a paper tape reader are incorporated, the latter with selectable tape format.
- Once programmed the system is electrically identical to TTL ROM/PROM at interface connector.
- Available for 110V 60Hz or 220V 50Hz nominal mains supplies.

Panel Facilities

Data Protection:

The two key-operated switches situated at the top of the panel control the most critical functions. The left hand switch, labelled *'Battery'*, when turned to the 'off' position isolates the battery supply in the system. When turned to the 'on' position the battery is connected, and the system is then protected against mains supply failure, or accidental 'switch off'. When the mains supply is not present, no operations on the system are possible, but data is stored. The battery is automatically charged whenever the unit is functioning from the mains supply. The light emitting diode (l.e.d.) associated with this key switch flashes at an approximate rate of once per second providing the battery key switch is turned 'on' and the battery voltage is sufficient to maintain stored data in the memory.

This product is only available in the United Kingdom

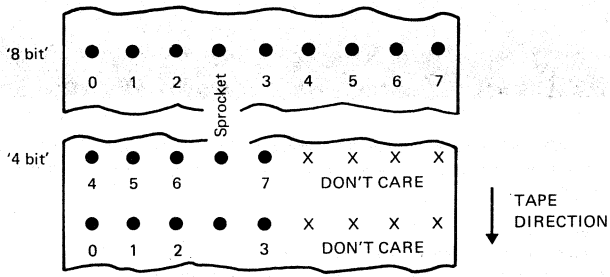
The right hand key switch labelled *'Write Enable'* is a protection against accidentally writing data into the memory when a program is already stored.

When in the 'Disable' position the 'Write' function of the memory cannot be operated. This includes data entry from the tape reader.

Thus, once data is stored in the memory, and the two key switches are set to battery 'on' and Write 'Disable' with the keys removed, the data cannot be corrupted. This is true until such time as the battery charge is exhausted if the mains supply is not present.

Data Entry

The top row of toggle switches labelled *'Data Input Select'* enable data to be set manually, or to be read from punched paper tape. The l.e.d. indicators below these switches show the data output from the memory. The numbering of the data bits (0 to 7) is arbitary, since the interface cable to the system can be wired to arrange 'bit significance' as required. However, it should be noted that the numbers correspond to the holes in the punched tape as shown below, according to the position of the *'Tape Reader'* switch.



The *'Manual Write'* switch causes the data word set up on the data selector switches to be entered into the memory at the current address. This will operate providing:

- The mains supply is present.
- The 'Write Enable' key switch is at 'Enable'.
- The address register has not been incremented to 'maximum count + 1'. (See 'addressing').

Note that if the 'Manual Write' switch is operated when a 'Data Input Select' switch is set to the centre 'Tape' position, the data entered into this bit is undefined.

To facilitate entering large amounts of data, a punched tape reader is incorporated in the ROMSYM. This simple device is hand-powered and self synchronising. The tape can be pulled through at any speed, but must not be allowed to reverse direction. The tape should have a blank leader section at least 1.5" in length with only sprocket holes punched in it.

To enter data from a tape:

- The mains supply must be switched on.
- Insert blank leader of tape into reader, the correct way round as indicated on the reader.
- Select tape format (4 bit or 8 bit).
- Select correct memory capacity (1k or 2k).
- Set 'Write Enable' switch to 'Enable'.
- Set 'Data Input Select' switches to 'Tape'.
- Reset Address register and load starting address.
- Pull tape completely through the reader.

Addressing

The address register supplies the address to the memory devices which is displayed on the lower row of 11 l.e.d. indicators. It can be reset, loaded, or incremented by 1 in the binary sequence and has protection against any attempt to increment it beyond the maximum count state to prevent over-writing of data in low order locations. The maximum count length is controlled by the *'Memory Capacity'* switch situated at the lower right of the panel, marked 1k/2k. These settings correspond to address register lengths of 1024 and 2048 states. If the system is only populated with 1k x 8 of memory, then the 'Memory Capacity' switch should always be set to 1k. If 2k x 8 of memory is fitted, then using the system with this switch in the 1k position will restrict all activities to a 1k x 8 section of memory. Setting the switch to 2k allows all the memory to be used, and in this state the l.e.d. indicator corresponding to address 10 becomes active.

The *'Reset/Load'* switch is also situated at the lower right of the panel, and when operated to the 'Reset' position it causes the content of the address register to be set to all 'zero' (i.e. logic low). It also initialises the tape reader logic such that if the blank leader section of a tape is present in the reader the logic will detect the first relevant data bit on the tape, according to the position of the 'Tape Reader' switch, as it is pulled through the reader and enter that the subsequent data into the memory. This providing the previously described conditions for data entry have been met. The 'Reset' function also removes the 'lock up' condition which the system adopts if the address register has been incremented to maximum count +1, as previously described.

Operating the 'Reset/Load' switch to the 'Load' position causes the address combination selected by the lower row of 11 toggle switches to be loaded into the address register. The 'Load' function also clears the address register overrun 'Lockout' condition, but does not initialise the tape reader logic. Thus if data is to be entered from paper tape into a sequence of address locations starting from a combination other than all 'zero', then the 'Reset/Load' switch is first used to 'Reset' the system, and then to 'Load' the starting address into the address register, after the blank leader section of the tape has been inserted into the reader.

The switch marked *'Step'*, situated at the lower left of the panel, allows the content of the address register to be incremented by one state in the binary count sequence. The address bit numbering is in order of significance in this sequence, with bit 0 being the least significant.

General notes about panel operation

The l.e.d. indicators for both data and address are lit to indicate a logic 1 or 'high' state. The data indicators show the output data of the memory from the location shown on the address indicators.

NOTE: For all panel operations, i.e. entering data, controlling the address register to examine the memory contents etc, the 'Write Enable' key switch must be in the 'Enable' position. The only exception is the 'Tape Reader' switch which must not be changed while the 'Write' function is enabled since it will cause erroneous data to be entered into the memory.

Using the System as a Read Only Memory (R.O.M.)

Having successfully entered data into the memory, and verified it if required, the system is made 'safe' by disabling the 'Write Enable' key switch. In this condition the only panel functions operative are the l.e.d. displays of data and address, and the system can now be accessed via the interface connector on the side of the case.

Addresses can be supplied to the system via this connector and Data Output will be supplied to the connector by the memory from corresponding locations. The address inputs to the system each represent one normal 74 series transistor-transistor-logic (t.t.l.) load, and the data outputs are 3-state t.t.l. with fan out capability of 20 normal 74 series t.t.l. loads.

A 'System Enable' ($\overline{SE}$) is also present at the interface connector, and this enables the 3-state output gates when driven to the 'low' state. This function allows the Data Outputs of the ROMSYM to be bus connected with those of other memory devices, or indeed with another ROMSYM.

Also present at the interface connector are ground and 5V supply pins. This allows interface cables to be constructed with proper signal screening etc. and also containing active elements if necessary. A possible example of this is to have a ROM code converter device in the cable, converting the address sequence supplied by the main system, into a different sequence for the ROMSYM. This can be useful when using the ROMSYM with a device such as the TMS1099 SE-1 which generates addresses in a pseudo-random sequence. This technique would allow the pseudo-random sequence to be converted to a binary sequence, thus simplifying program loading and editing in the ROMSYM.

Interface Connector

Pins 1-25 inclusive are connected to 'ground' (0V).

Pin No.	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
Function	0V	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	0V	5V	$\overline{SE}$	0V	D0	D1	D2	D3	D4	D5	D6	D7	0V

NOTE: The 5V supply on pin 39 should only be used to provide 100mA maximum to external circuitry, and should not be connected to any external supply.

38510/MACH IV

High-Reliability Microelectronics Procurement Specifications

MIL-STD-883

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REVISIONS

CLASSIFICATION (MAJOR/MINOR)	DATE CODE EFFECTIVITY	LTR	DESCRIPTION	DATE	APPROVED
Major	7040	A	Incorporate MIL-M-38510 and Revision Notice 2 of MIL-STD-883	8/15/70	
Major	7239	B	Incorporate Revision Notice 3 and 4 of MIL-STD-883 and Revision A of MIL-STD-38510	9/1/72	
Major	7401	C	Incorporate revised Level IV (SNH) processing with inclusion of recorded electrical data with delta requirements; incorporate technological criteria in Table III for precap of complex circuits.	1/1/74	
Minor	7518	D	Incorporate Revision A of MIL-STD-883 and provisions for MOS LSI and CMOS devices	4/15/75	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGLES ± 1°
3 PLACE DECIMAL ±.010
2 PLACE DECIMAL ±.02
INTERPRET DWG. IN ACCORDANCE WITH STD. DESCRIBED IN MIL-STD-100
MATERIAL:

	DR	DATE
	C. E. [illegible]	9/22/69
CHK	[illegible]	10/7/69
ENGR	[illegible]	10/7/69
QUALITY CONTROL	[illegible]	10/6/69
QRA MGR.	D Adams	10/6/69
DESIGN ACTIVITY RELEASE DEPARTMENT MANAGER, TAL	[illegible]	10/7/69
CIRCUITS DIVISION MANAGER	[illegible]	

TEXAS INSTRUMENTS INCORPORATED
SEMICONDUCTOR CIRCUITS DIVISION DALLAS, TEXAS

TITLE: MICROELECTRONICS, HIGH RELIABILITY PROCUREMENT SPECIFICATION (MIL-STD 38510/883)

SIZE	CODE IDENT NO.	DRAWING NO.
A	01295	38510/MACH IV PROGRAM

SCALE	REV D	SHEET

38510/MACH IV PROGRAM

1.0 SCOPE

1.1 This specification establishes standards for materials, workmanship, performance capabilities, identification, and processing of high-reliability monolithic integrated circuits.

1.2 Intent

The intent of this document is such as to recognize that quality and reliability are *built* into, not *tested* into, a product. There is no specification or screening procedure that can substitute for inherent, built-in reliability. However, it must be realized that irrespective of lot quality, there will always be some small percentage of devices that are subject to early failure (infant mortality). A well engineered screening procedure will eliminate most, if not all, of these early failures. Secondly, the screening and acceptance testing described herein will also serve to demonstrate, with a high degree of statistical confidence, that the required levels of quality and reliability have, in fact, been built into the product.

2.0 APPLICABLE DOCUMENTS

2.1 The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein:

2.2 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	Microcircuits devices, general specification for

2.3 Standards

Military

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-790	Reliability Assurance Program for Electronic Parts Specification
MIL-STD-1276	Leads, Weldable, for Electronic Components Parts
MIL-STD-1313	Microelectronics Terms and Definitions

Detail Specifications

SNXXXX (Bipolar) TMSXXXX (MOS LSI) TFXXXX (CMOS)	Detail Specification for a Particular Part Type (e.g., Manufacturer's Data Sheet)

2.4 Precedence of Documents

For the purpose of interpretation, in case of any conflicts, the following order of precedence shall apply:

a)	Purchase Order	—The purchase order shall have precedence over any referenced specification.
b)	Detail Specification	—The detail specification shall have precedence over this specification and other referenced specifications.
c)	This Specification	—This specification shall have precedence over all referenced specifications.
d)	Referenced Specifications	—Referenced Specifications shall apply to the extent specified herein.

2.5 Federal and/or military specifications and standards required shall be obtained from the usual government sources.

3.0 GENERAL REQUIREMENTS

The individual item requirements shall be as specified herein and in accordance with the applicable detail specification. In the event of any conflict between the requirements of this specification and the detail specification, the latter shall govern. The static and dynamic electrical performance requirements of the integrated circuits plus absolute maximum ratings and test methods shall be as specified in the detail specifications.

3.1.1 Definitions

a)	LTPD	Lot Tolerance Percent Defective shall be as defined by MIL-M-38510.
b)	λ	Lambda, stated in percent per 1000 hours as defined by MIL-M-38510.
c)	MRN	Minimum reject number as defined by MIL-M-38510.
d)	Production Lot	For the purpose of this specification, a production lot shall be defined per MIL-M-38510.
e)	Inspection Lot	An inspection lot shall be as defined in MIL-M-38510.
f)	C	Acceptance number as defined by MIL-M-38510.

3.1.2 Terms and Definitions

Terms and definitions shall be as defined in MIL-STD-1313.

3.1.3 Classification of Requirements

The requirements for the integrated circuits are classified herein as follows:

Requirement	Paragraph
Process Conditioning, Testing and Screening	3.2
Qualification	3.3
Design and Construction	3.4

Marking of Integrated Circuits	3.5
Product Assurance	3.6
Workmanship	3.7
Performance Capabilities	3.8
Quality and Reliability Assurance Program Plan	3.9

3.2 Process Conditioning, Testing and Screening

Three levels of screening and quality assurance for integrated circuits are provided for in this specification. Process conditioning, testing and screening shall be as specified in 4.3 and the applicable figure for the appropriate quality assurance level stated on the purchase order and defined as follows:

SCREENING LEVEL	PART NUMBER PREFIX			APPLICABLE FLOW CHART
	BIPOLAR	CMOS	MOS LSI	
38510/883 Class A (Level IV)	SNH	TFH	Not Avail.	Figure 4
38510/883 Class B (Level III)	SNC	TFC		Figure 3
			SMC	Figure 2
38510/883 Class C (Level I)	SNM	TFM	Not Avail.	Figure 1

3.3 Qualification

Vendor qualification for delivery of integrated circuits to this specification shall be as specified in paragraph 4.2.

3.4 Design and Construction

Integrated circuit design and construction shall be in accordance with the requirements specified herein and in the applicable detail specification.

3.4.1 Topography

Integrated circuits furnished under this specification shall have topography information available for review by procuring activity. The information made available shall provide sufficient data for thorough circuit design, application, performance, and failure analysis studies.

3.4.1.1 Monolithic Die Topography

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the topography of elements formed on the silicon monolithic die shall be available for review. This shall be identified with the specific detail integrated circuit part-type in which it is used and the applicable detail specification.

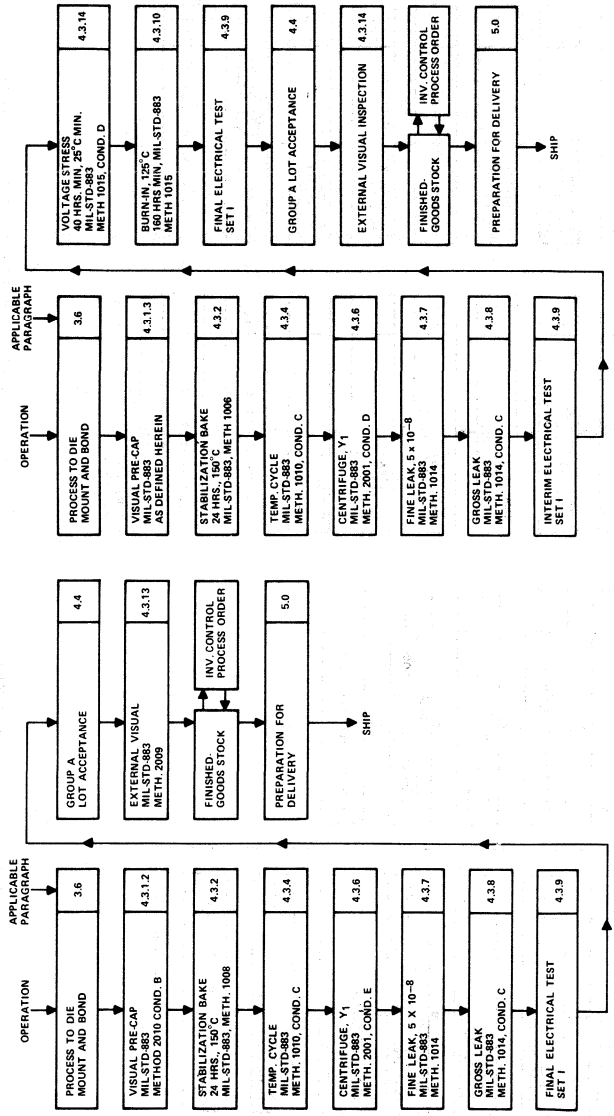

FIGURE 1–FLOW CHART FOR 38510 CLASS C LEVEL I

FIGURE 2–FLOW CHART FOR MOS LSI
38510 CLASS B (LEVEL III SMC)

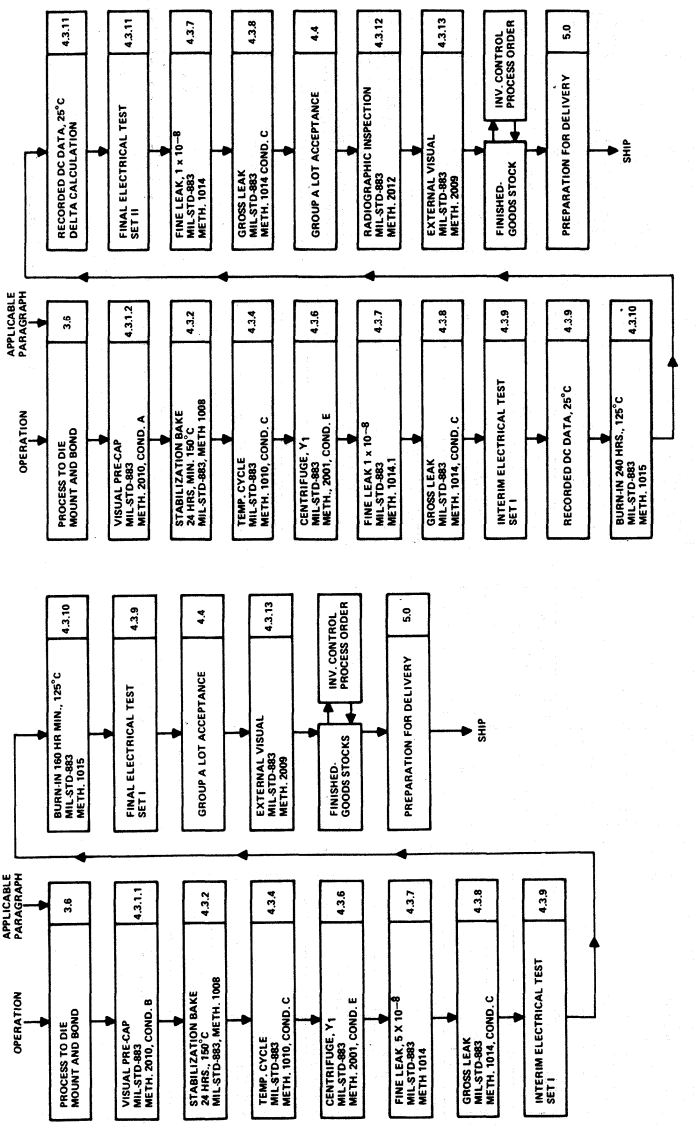

FIGURE 3—FLOW CHART FOR 38510 CLASS B LEVEL III

FIGURE 4—FLOW CHART FOR 38510 CLASS A LEVEL IV

3.4.1.2 Die Intraconnection Pattern

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the specific intraconnection pattern utilized to intraconnect the elements in the circuit. This shall be in the same scale as the die topography 3.4.1.1 so that the elements utilized and those not being used can easily be determined.

3.4.2 Materials

Materials shall be inherently non-nutrient to fungus and shall not blister, crack, outgas, soften, flow or exhibit other immediate or latent defects that adversely affect storage, operation or environmental capabilities of integrated circuits.

3.4.2.1 Material Selection

Materials selected for use in the construction of the integrated circuits shall be chosen for maximum suitability for the application. This shall include consideration of the best balance for:

a) Electrical performance

b) Thermal compatibility and conductivity

c) Chemical stability including resistance to deleterious interactions with other materials

d) Metallurgical stability with respect to adjacent materials and change in crystal configuration

e) Maximum stability with regard to continued uniform performance through the specified environmental conditions and life.

3.4.2.2 Foreign Materials

No lacquer, grease, paste, desiccant or other similar foreign encapsulant or coating material shall be included in the circuit enclosure nor applied to any part of the internal circuit assembly.

3.4.3 Mechanical

3.4.3.1 Case

Each integrated circuit shall be securely mounted and hermetically sealed within a case designed and constructed to conform to the outline and physical dimensions shown in the detailed specification.

3.4.3.2 Interconnections

Interconnections within the integrated circuit case shall be minimized and there shall be no wire crossovers. Circuit intraconnections by means of wire jumpers shall not be used. (See Note 6.2)

3.4.3.3 Leads

Lead material, construction, and outline shall be as specified on the detail specification and shall be capable of meeting the solderability test of MIL-STD-883, Method 2003. (See note 6.4).

3.4.3.3.1 Lead Size

Lead outline and dimensions shall be as specified in the detail specification.

3.4.3.3.2 Lead Surface Condition

Leads shall be free of the following defects over their entire length when inspected under a minimum of 4X magnification:

a) Foreign materials adhering to the leads such as paint, film, deposits and dust. Where adherence of such foreign materials is in question, leads may be subjected to a clean, contaminant-free (e.g., oil, dust, etc.), filtered air stream (suction or expulsion) of 88 feet per second maximum, or a wash/rinse as necessary and reinspected.

b) Nicks, cuts, scratches or other surface defacing defects which expose the base metal.

3.4.3.3.3 Lead Straightness

Leads shall be aligned within a 0.050-inch diameter, 0.050-inch length cylinder concentric to the point of lead emergence from the case and the X-axis (the axis parallel to the lead axis). Along the remaining lead length, there shall be no unspecified bend whose radius is less than 0.10 inch and no twist whose angle is greater than 30° (ribbon leads, only).

3.4.3.3.4 Preformed Leads

Preformed leads, when specified, shall be in accordance with the detail specification. The part number of the integrated circuit shall remain as specified in the applicable detail specification or purchase order, the applicable suffix designation shall appear on the purchase order but shall not be marked on the device.

3.4.3.3.5 Carriers (Mech-Pak Carrier)

Carrier-matrix assemblies consisting of individually mounted integrated circuits shall be furnished when so specified by purchase order. The individual carriers shall have provisions for use with automatic test equipment contacts. Devices supplied "clipped-out" of the Mech-Pak Carrier shall be supplied in the Barnes Carrier type 029-188 or equivalent. (Applicable to Flat Packs only.)

3.5 Marking of Integrated Circuits

3.5.1 Legibility

All marking shall be permanent in nature and remain legible when subjected to specified operating, storage, and environmental requirements. All markings shall be insoluble in standard solvents such as trichlorethylene, water and xylene.

3.5.2 Marking Details

Marking of the integrated circuits shall be located as follows unless otherwise specified in the detail specification:

a) TO-99, TO-100, and similar "can" cases shall be marked on the top of the case. Where space limitations exist, the side of the case may be used.

b) Flat Packs shall be marked on the top of the case. Where space limitation exists, the bottom of the package may be utilized as necessary. As a minimum the top of the package shall show the manufacturer's identification mark or symbol, the device part number, date code, and pin 1 orientation mark (where applicable).

c) Dual-in-line plug-in packages shall be marked in the same manner as flat packs.

3.5.3 Required Device Marking

a) Index point indicating the starting point for numbering of leads shall be as indicated in the detail specification. The indexing point may be a tab, color dot, or other suitable indicator.

b) Manufacturer's identification mark or symbol.

c) An alpha-numeric lot date code indicating the week of initial submission for screening or inspection. The date code shall be as follows:

1) EIA four-digit date code, the first two numbers shall be the last two digits of the year, the last two numbers shall indicate the calendar week.

2) A Gothic letter which identifies separate lots of the same device type processed within the same calendar week. (If no more than one lot is processed through screening or inspection in a given calendar week, the Gothic letter may be omitted.)

d) Manufacturer's part number defining circuit type and applicable MIL-STD-883 screening level and MIL-M-38510 product assurance level as defined in paragraph 3.2.

e) Individual device serial number is required for Class A (SNH).

f) A dot to indicate acceptance by Radiographic inspection

NOTE:

When a color dot is used to identify pin one, the radiographic inspection acceptance dot shall be placed on the bottom of the package.

g) Gothic letter per U.S. Customs code preceding data code identifies assembly location.

3.6 Product Assurance

The manufacturer shall establish and maintain a reliability assurance program that complies with the basic intent of MIL-STD-790. Furthermore, it is intended that each integrated circuit delivered shall be free of any defect in design, material, manufacturing process, testing and handling, which would degrade or otherwise limit its performance when used within the specified limits.

3.6.1 Visual and Mechanical Examination

Integrated circuits shall be examined to verify that material, design, construction, physical dimensions, marking and workmanship are in accordance with the specified acceptance criteria.

3.6.2 Test Equipment

The manufacturer shall prepare and maintain a current list, by name and drawing number or other unique identification, of test equipment used in the manufacturing and testing of devices submitted for acceptance inspection under this specification. This list shall be made available to the procuring activity representative upon request.

3.6.3 Process Controls

Each integrated circuit shall be constructed by manufacturing processes which are under the surveillance of the manufacturer's Quality Control department. The processes shall be monitored and controlled by use of statistical techniques in accordance with published specifications and procedures. The manufacturer shall prepare and maintain suitable documentation (such as quality control manuals, inspection instructions, control charts, etc.) covering all phases of incoming part and material inspection and in-process inspections required to assure that product quality meets the requirements of this specification. The

procuring activity may verify, with the permission of and in the company of the manufacturer's designated representative, that suitable documentation exists and is being applied. Information designated as proprietary by the manufacturer will be made available to the procuring activity or its representative only with the written permission of the manufacturer.

Process control is recognized as being vital to the concept of "built-in" quality. The process control program shall include a scanning electron microscope (SEM) monitor program for evaluating the metal integrity over oxide step and oxide step contour. The SEM analysis will be defined in a Quality & Reliability Assurance document.

3.6.4 Production Changes

The manufacturer shall advise the procuring activity of the time at which any major change(s) in production or QC methods or documentation become effective during the period of device production for delivery against any given purchase order referencing this specification.

3.7 Workmanship

Integrated circuits shall be manufactured and processed in a careful and workmanlike manner, in accordance with the production processes, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the reliability assurance program established by paragraph 3.6.

3.7.1 Personnel Certification

The manufacturer shall be responsible for training, testing and certification of personnel involved in producing integrated circuits. Training shall be commensurate and consistent with the requirements of this specification and in conformance to the basic intent of MIL-STD-790. Training aids in the form of satisfactory criteria shall be available for operator and inspector review at any time.

3.7.2 Personnel Evaluation

The supplier shall maintain a continuous evaluation of the proficiency of personnel concerned with production and inspection. Retraining of an operator or inspector shall be required when this evaluation establishes that a degree of proficiency necessary to meet the requirements of this specification is not being exercised.

3.7.3 Rework provisions

3.7.3.1 Rework

All rework on micorcircuits manufactured under this specification shall be accomplished in accordance with paragraph 3.7.1 of MIL-M-38510 as defined herein.

3.7.3.2 Rebonding

Rebonding shall be in accordance with MIL-M-38510, as defined herein (see Note 6.5)

3.8 Performance Capabilities

The integrated circuits delivered to this specification shall be designed to be capable of meeting the environmental requirements specified in Table II. The manufacturer need not perform these tests specifically for the contract or specification, but shall provide data which demonstrates the ability of the integrated circuits to pass the environmental tests. The data shall have been generated on devices from the same generic family as the circuits being supplied to this specification, and the package configuration shall be the same as for the delivered parts (i.e., Flat Pack, TO-100, etc.).

3.9 Quality and Reliability Assurance Program Plan

The manufacturer shall establish and implement a Quality and Reliability Assurance Program Plan that meets the intent of MIL-M-38510, Appendix A. Submission of the program plan to the procuring activity shall not be a requirement of this specification; however, the program plan shall be maintained by the manufacturer and shall be available for review by the procuring activity.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection

Unless otherwise specified in the contract or purchase order, the manufacturer is responsible for the performance of all inspection requirements specified herein. Except as otherwise specified, the manufacturer may utilize his own facilities or any commercial laboratory acceptable to the procuring activity. The procuring activity may, at its discretion, perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.1 Inspection and Testing Procedures Coverage

Inspection and testing processes and procedures prepared in fulfillment of the reliability assurance program established per paragraph 3.6 shall be prescribed by clear, complete and current instructions. These instructions shall assure inspection and test of materials, work in process and completed integrated circuits as required by this specification. In addition, criteria for approval and rejection of materials and integrated circuits shall be included.

4.1.2 Inspection at Point of Delivery

The procuring activity may, at its discretion, reinspect any or all of the delivered parts excluding Group B and C destructive samples as defined by MIL-STD-883. All parts found to be defective, excluding devices exhibiting damage from use, may be returned to the manufacturer at the manufacturer's expense.

4.1.3 Inspection Records

The manufacturer shall maintain a reliability data and records library. This library shall have on file, for review by the procuring activity, records of examination, qualification test results, variables data (when required) and all other pertinent data generated on devices manufactured to this specification.

4.1.4 Control of Procurement Sources

The manufacturer shall be responsible for assuring that all supplies and services conform to this specification, the detail specification and the manufacturer's procurement requirements.

4.1.4.1 Manufacturer's Receiving Inspection

Purchased supplies shall be subjected to inspection after receipt as necessary to ensure conformance to contract requirements. In selecting sampling plans, consideration shall be given to the controls exercised by the procurement source and evidence of sustained quality conformance.

4.1.4.2 The manufacturer shall provide procedures for withholding from use all incoming supplies pending completion of required tests or receipt of necessary certification or test records and their evaluation.

4.1.4.3 The manufacturer shall initiate corrective action with the procurement source depending upon the nature and frequency of receipt of nonconforming supplies.

4.1.5 Procuring Activity Quality Assurance Representative

The procuring activity, may, at its discretion, place quality assurance representatives in the manufacturer's plant as deemed necessary to assure conformance to contract requirements in any non-proprietary phase of design, fabrication, processing, inspection, and testing of the integrated circuits being produced. The manufacturer shall provide reasonable facilities and assistance for the safety and convenience of such personnel in the performance of their duties. Inspection and test procedures shall be made available for review by the quality assurance representative.

4.2 Qualification and Quality Conformance Inspection

4.2.1 Qualification

Manufacturer's specific device qualification shall be based on compliance with the quality conformance test per Table III for MOS LSI devices. Qualification for other technologies shall be per Table 1 except that the testing will be to one LTPD level tighter than as defined in Table B-I of MIL-M-38510.

4.2.1.2 Procedures and Definitions

4.2.1.2.1 Sampling Procedure

Device selection for the qualification procedure of 4.2.1 shall be based on a random sampling technique and will be selected from a generic family.

4.2.1.2.2 Generic Family

Electrically and structurally similar devices shall be said to comprise a generic family (e.g., TTL) if they meet the following criteria:

a) Are designed with the same basic circuit-element configuration such as TTL, TTL Schottky, DTL, CMOS, MOS metal-gate, or MOS silicon-gate, and differ only in the number or complexity of specified circuits which they contain. Generic family for linear circuits is defined by circuit function (e.g. op amp, comparator, etc.).

b) Are designed for the same supply, bias and signal voltage, and for input/output capability with each other under an established set of loading rules.

c) Are enclosed in housings (packages) of the same basic construction (e.g., hermetically sealed flat packages, dual-in-line ceramic, dual-in-line plastic) and outline, differing only in the number of active housing terminals included and/or utilized.

4.2.2 Quality Conformance Inspection

Quality conformance inspection group B and C requirements are per Tables I and II, Table II shall apply to MOS LSI and Table I to other technologies.

a) When specifically called out and funded on the purchase order or contract, the manufacturer shall perform the quality conformance inspections (Group B and/or Group C) on a lot-by-lot basis.

b) The manufacturer shall, upon request, make available for review generic quality conformance inspection and data. Data on Group B shall be by package type, number of pins, and assembly location for all subgroups.

Data on Group C, subgroups 1, 2, and 3, shall be by package type, number of pins, and assembly location. Subgroups 4 and 5 by chip generic family in hermetic packages.

4.2.2.1 Lot Acceptance Sampling

Statistical sampling for quality conformance inspections shall be in accordance with MIL-M-38510 Table B-I.

Group B samples, except bond strength samples, shall be selected from sublots that have successfully completed all of the 100% processing steps specified on the applicable process flow chart.

4.2.2.2 Resubmission of Failed Lots

When any lot submitted for quality conformance inspection fails any subgroup requirement, it may be resubmitted a maximum of one time for that particular subgroup. One additional submission is permitted, provided an analysis is performed to determine the failure mechanism for each reject device in the subgroup, and that it is determined that the failures are due to one of the following:

a) Testing error resulting in electrical damage to devices

b) A defect that can effectively be removed by rescreening the lot

c) Random defects which do not reflect poor basic device designs or poor workmanship.

4.2.2.3 Early Shipments

When quality conformance inspection is being performed for a specific contract or purchase order, the accepted Group A devices that are awaiting shipment pending successful completion of Group B and/or Group C, shall be stored in the Quality Assurance test area. Under no circumstances shall such parts be shipped prior to the successful completion of the Group B tests.

4.2.2.4 Groups B and C Test Data

All lot-by-lot data generated by Group B and/or Group C testing when specifically called out and funded on the purchase order, shall accompany the initial shipment of devices. This data shall consist, at a minimum, of the following:

a) Attributes data for Group B. Endpoints for the subgroups are visual per the applicable MIL-STD-883 test method.

b) Attributes data for Group C subgroups 1, 2, 4 and 5. Endpoints for these subgroups shall be per Table I and II.

4.2.2.5 Precedure in Case of Test Equipment Failure or Operator Error

Where an integrated circuit is believed to have failed as a result of faulty test equipment or operator error, the failure shall be entered in the test record which shall be retained for review along with a complete explanation verifying why the failure is believed to be invalid. If it is determined that the failure is invalid, a replacement integrated circuit from the same inspection lot may be added to the sample. The replacement integrated circuit shall be subjected to all those tests to which the discarded integrated circuit was submitted prior to its failure, and any remaining specified test to which the discarded integrated circuit was not subjected prior to its failure.

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4.3 Quality Assurance Processing, Methods and Procedures

This section establishes the test methods and conditions to be used for the 100% processing (screening) requirements specified by the applicable process flow chart.

4.3.1 Precap Visual Inspection

Each microcircuit shall be required to pass the appropriate precap visual inspection defined as follows. Precap Lot Acceptance shall be per paragraph 4.6.

4.3.1.1 38510 Class C (Level I) and 38510 Class (Level III) devices shall be visually inspected in accordance with MIL-STD-883, Method 2010, Condition B.

4.3.1.2 38510A (Level IV) devices (designated for NASA type applications) shall be visually inspected in accordance with MIL-STD-883, Method 2010, Condition A. (See notes 6.1.1.1 and 6.1.1.2).

4.3.1.3 Complex MSI and LSI circuits as defined in MIL-STD-883, Method 5004, paragraph 3.3 may be precap inspected per MIL-STD-883, Method 5004, paragraph 3.3.1 for 38510 Class B (Level III) and paragraph 3.3.2 for 38510 Class C (Level I).

4.3.2 Stabilization Bake

The purpose of this test is to determine the effect on microelectronic devices of baking at elevated temperatures without electrical stress applied. Test shall be performed in accordance with MIL-STD-883, Method 1008, Condition C.

4.3.3 Thermal Shock

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. Test shall be performed in accordance with MIL-STD-883, Method 1011.1, Condition A.

4.3.4 Temperature Cycle

This test is conducted for the purpose of determining the resistance of a part to exposures to extremes of high and low temperatures, and to the effect of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. Test shall be performed in accordance with MIL-STD-883, Method 1010, Condition C, minimum of 10 cycles. For MSI and LSI complex devices as defined in MIL-STD-883, Method 5004, paragraph 3.3, 50 cycles may be used in lieu of alternate pre-cap visual inspection criteria.

4.3.5 Mechanical Shock

The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Test shall be performed in accordance with MIL-STD-883, Method 2002, Condition B, five blows minimum.

4.3.6 Centrifuge (Constant Acceleration)

The centrifuge test is used to determine the effects on microelectronics devices of a centrifugal force. This test is designed to indicate structural and mechanical weaknesses not necessarily detected in shock and vibration tests. Test shall be performed in accordance with MIL-STD-883, Method 2002, Condition E for devices having less than 20 pins and Condition D for those having more than 20 pins.

4.3.7 Fine Leak Test

Each integrated circuit for 38510 Class C (Level I), 38510 Class B (Level III), and 38510 Class A (Level IV) screens shall be subject to a fine leak test in accordance with paragraph 4.3.7.1 or 4.3.7.2. The method shall be optional providing it is consistent with and capable of detecting the specified leak rate of the applicable process flow chart.

4.3.7.1 Helium Leak Test

Helium leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition A.

4.3.7.2 Radiflo Leak Test

Radiflo leak test- shall be performed in accordance with MIL-STD-883, Method 1014, Condition B. Krypton 85 bomb pressure and dwell time are a function of the radioactivity level and shall be selected so as to conform to the equations given in Condition B.

4.3.8 Gross-Leak Test

Each integrated circuit for 38510 Class C (Level I), 38510 Class B, (Level III) and 38510 Class A (Level IV) screens shall be subjected to the appropriate gross-leak test of paragraph 4.3.8.1 or 4.3.8.2, or an approved equivalent. The manufacturer may, at his option, perform gross-leak testing after the Set I Electrical Tests of paragraph 4.3.9.

4.3.8.1 When specifically called out and funded on the purchase order or contract, units will be bombed 2 hours minimum at 30 psig in FC-78, or equivalent. Units will then be immersed in FC-40 or equivalent at +125°C ±5°C for 30 seconds minimum and observed for for a definite stream of bubbles, more than two large bubbles, or an attached bubble that grows in size, per MIL-STD-883, Method 1014, Condition C2.

4.3.8.2 Units will be immersed in FC-40 or equivalent at +25°C ± 5°C for 30 seconds minimum and observed for a definite stream of bubbles, more than two large bubbles or an attached bubble that grows in size, per MIL-STD-883, Method 1015, Condition C1,.

4.3.9 Final Electrical Test (Set I)

Each integrated circuit shall be required to pass the electrical requirements of the data sheet. The manufacturer shall also perform such additional testing necessary to assure the parts will meet the temperature extreme limits. MOS LSI memory devices will be 100% dc and ac tested both at 25°C and at high temperature.

When specifically called out and funded on the purchase order or contract, the manufacturer shall perform subgroups 2, 3, and 4 of paragraph 4.4 in accordance with Method 5004 of MIL-STD-883.

4.3.10 Burn-In

The burn-in screen is performed for the purpose of eliminating marginal devices and early-life failures evidenced as time and stress dependent. Test shall be in accordance with MIL-STD-883, Method 1015, Condition A, D, or E at 125 ± 5°C for digital circuits and Conditions A, B, C, or D for linear circuits. 38510 Class B (Level III) MSI and LSI complex devices, as defined in MIL-STD-883, paragraph 3.3.1, may receive a 240-hour-minimum burn-in in lieu of alternate precap visual inspection criteria per MIL-STD-883, Method 5004, paragraph 3.3.1.

4.3.11 Final Electrical Test (Set II)

Each 38510 Class A (Level IV) integrated circuit shall be required to pass the electrical requirements of the detail specifications. The following tests shall be performed as a minimum: dc parameters at maximum and minimum rated temperatures, and switching parameters at 25°C. In addition, each bipolar device shall have critical 25°C dc electrical parameters read and recorded by serial number and shall pass the following delta requirements:

PARAMETER	DELTA LIMIT
V_{OL}	±10% of detail specification limit
V_{OH}	±10% of detail specification limit
I_{IL}	±10% of detail specification limit
I_{IH}	±10% of detail specification limit

CMOS recorded parameters and delta limits will be defined by the manufacturer as required.

One copy of the pre-burn-in and post-burn-in recorded data with delta calculations shall be shipped with each lot. Data will not be available for the metal flat pack (T). See MIL-M-38510, Class S. The manufacturer may, when deemed necessary, elect to perform additional electrical testing over and above the requirements stated herein.

4.3.12 Radiographic Inspection (X-ray)

Test shall be performed in accordance with MIL-STD-883, Method 2012. X-ray may be performed at any point after serialization at the manufacturer's option. (see note 6.3).

4.3.13 External Visual Inspection

The purpose of this examination is to verify that materials, construction, marking, and general workmanship are as specified. Examination shall be in accordance with MIL-STD-883, Method 2009.

4.3.14 Voltage Stress

Selected n-channel MOS LSI devices will be voltage stressed for 40 hours minimum at 25°C min per MIL-STD-883 Method 10155, Condition D.

4.4 Group A Conformance

Group A conformance shall consist of the electrical parameters in the manufacturer's data sheet. If an inspection lot is made up of a collection of sublots, each sublot shall conform to Group A, as specified.

SUBGROUP	LTPD (%) LEVEL I 38510C	LEVEL II	LEVEL III 38510B	LEVEL IV 38510A
Subgroup 1 25°C, dc	5	7	5	5
Subgroup 2 High Temperature, dc	10	10	7	5
Subgroup 3 Low Temperature, dc	10	10	7	5
Subgroup 4	10	10	7	5
Dynamic and Switching Tests @ 25°C				

NOTE: Functional tests included in dc tests.

4.5 Certification

The manufacturer shall include a certificate of compliance with each shipment of parts if requested on the purchase order. This certificate shall indicate that all specified tests and requirements of this specification have been made or met, and that the lot of devices (identified by lot and/or batch number) is acceptable. The certificate shall bear the name and signature of the manufacturer's Quality Control representative, the date of acceptance or signing, and any pertinent notes as applicable.

4.6 Precap Lot Acceptance

After each precap inspection the lot of devices shall be sampled by quality control and inspected for the specified visual criteria.

TABLE I
QUALITY CONFORMANCE TEST (GROUP B/GROUP C)

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD LEVEL IV 38510A	LTPD LEVEL III 38510B	LTPD LEVEL I 38510C
Subgroup 1[2]					
Physical Dimensions	2016		19	15	20
Subgroup 2[2]					
Marking Permanency	2015				
Visual and Mechanical	2014				
Bond Strength[1]	2011	Condition C or D 2 grams for Au bonds 1.5 grams for Al bonds	10	15	20
Subgroup 3[2]					
Solderability	2003	Omit Aging	10	15	15
Subgroup 4[2]					
Lead Fatigue	2004	Conditions B_2			
Fine Leak	1014	Conditions A or B, per para. 4.3.7 of this spec.			
Gross Leak	1014	Condition C, per para. 4.3.8 of this spec.	10	15	15
		GROUP C			
Subgroup 1					
Thermal Shock	1011	Condition B			
Temp. Cycle	1010	Condition C			
Moisture Resistance	1004	Omit Initial Cond.			
Fine Leak	1014	Conditions A or B, per para 4.3.7 herein			
Gross Leak	1014	Condition C, per para. 4.3.8 herein	10	15	15
Electrical End Points	5005	Subgroups 1, 2, 3, and 7			
Subgroup 2					
Mechanical Shock	2002	Condition B			
Vibration Variable Freq.	2007	Condition A			
Constant Acceleration	2001	Condition E[3]			
Fine Leak	1014	Conditions A or B, per para. 4.3.7 herein			
Gross Leak	1014	Condition C, per para. 4.3.8 herein	10	15	15
Electrical End Points	5005	Subgroups 1, 2, 3, and 7			
Subgroup 3					
Salt Atmosphere	1009	Condition A Omit Initial Conditioning	10	15	15
Subgroup 4					
High Temp Storage	1008	150°C, 1000 Hrs.			
Electrical End Points	5005	Subgroups 1, 2, 3, and 7	7	7	7
Subgroup 6					
Operating Life Test	1005	125°C, 1000 Hrs. Minimum			
Electrical End Points	5005	Subgroups 1, 2, 3, and 7	5	5	5

1. Bond strength test may be performed on samples randomly selected immediately following internal visual prior to sealing.
2. Visual and/or hermetic end points; hence, electrical or visual rejects may be used. Reference MIL-STD-883, Method 5005.2, para. 3.4.
3. Condition D for packages with 20 pins or more. Condition E for packages with less than 20 pins.

TABLE II
QUALITY CONFORMANCE TEST
MOS LSI CIRCUIT

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD
Subgroup 1			
Temperature Cycle	1001	Condition C	
Constant Acceleration	2001	Condition D[1], Y_1 Plane	
Electrical End Points	5005	Subgroup 1	15
Subgroup 2			
Operating Life	1005	Condition D, 500 Hrs. Minimum	
Electrical End Points	5005	Subgroup 1	10

1. Condition D for packages with 20 pins or more. Condition E for packages with less than 20 pins.

TABLE III
MANUFACTURERS QUALIFICATION PROCEDURE
MOS LSI CIRCUITS

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD
Subgroup 1[1]			
Physical Dimensions	2016		15
Visual and Mechanical	2014		
Subgroup 2[1]			
Solderability	2003	Omit Aging	15
Subgroup 3[2]			
Thermal Shock	1011	Condition B	
Temperature Cycling	1010	Condition C	
Moisture Resistance	1004	Omit Initial Conditioning	
Electrical End Points	5005	Subgroup 1	15
Subgroup 4[2]			
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E[3]	
Electrical End Points	5005	Subgroup 1	15
Subgroup 5[1]			
Lead Fatigue	2004	Condition B2	
Fine Leak	1014	Condition A or B Per Para. 4.3.7 Herein	
Gross Leak	1014	Condition C2 Per Para. 4.3.7 Herein	15
Subgroup 6[1]			
Salt Atmosphere	1009	Condition A, Omit Initial Conditioning	15
Subgroup 7[2]			
Storage Life	1008	150°C, 1000 Hrs. Minimum	
Electrical End Points	5005	Subgroup 1	7
Subgroup 8[2]			
Operating LIfe	1005	85°C, 1000 Hrs. Minimum	
Electrical End Points	5005	Subgroup 1	10
Subgroup 9[1]			
Bond Strength	2011	Condition B, D	10 devices not greater than 1% defective

1. Visual and/or hermetic end points; hence, electrical rejects may be used. Reference MIL-STD-883, Method 5005.2, Para. 3.4.
2. Electrical end points only.
3. Condition D for packages with 20 pins or more. Condition E for packages with less than 20 pins.

5.0 PREPARATION FOR DELIVERY

5.1 Final Visual Shipping Inspection

Each lot of microcircuits and its associated documentation shall be sampled by Quality Control and visually inspected for the following:

a) Scratched, nicked or bent leads

b) Damaged header (packages)

c) All test data specified in section 4.0

d) Certificate of Compliance as specified in section 4.0

e) All other pertinent documentation required and specified by this specification.

5.2 Packing Requirements

Parts shall be packed in containers of the type, size, and kind commonly used which will ensure acceptance by common carriers and safe delivery at the destination and in accordance with MIL-M-55565, Level C, bulk pack. The containers shall be clearly marked with manufacturer's name or symbol.

5.3 Preservation and Package Identification

The package shall be marked with the following:

The country of origin if other than U.S.A.

Procuring activity parts number

Purchase order number

Material nomenclature

Quantity

Lot number

Date code

This information shall appear on the label or shall be directly marked on each container. Method is optional.

6.0 NOTES

6.1 Precap Visual Method 2010

The following criteria may be in conflict with the circuit design topology and construction techniques of some microcircuit manufacturers. Where such a conflict does exist, the inspection criteria listed herein may be waived. (Reference paragraph 3.0 of MIL-STD-883, Method 2010).

6.1.1 Preseat Visual Inspection, Test Condition B [38510 Class B (Level III) and 38510 Class C (Level I)].

6.1.1.1 Paragraph 3.2: a 20-PSI minimum blow-off prior to seal will be performed to meet the intent of a controlled environment.

6.1.1.2 For titanium-tungsten, gold, titanium-tungsten multilayered systems, the underlying metal is defined as the bottom titanium tungsten and the top layer is defined as gold.

6.2 Interconnections

Circuit interconnections (metallization pattern) shall be designed so that no properly fabricated connection shall experience a current density greater than 5×10^5 amperes/cm^2, including allowances for worst-case conductor composition, normal production tolerances on design dimensions, and nominal thickness at critical areas such as contact windows.

6.3 X-Ray Method 2012

Paragraph 3.9.2.2a(2) and (3) delete and replace with: "Cause for rejection shall be a single void in the bar attachment material opening two adjacent sides and exceeding 50% of the length of one side and 100% of the length of the other side."

6.4 Salt Atmosphere Test, Method 1009

Where package design considerations necessitate (such as 0.75-inch tip-to-tip metal flat packs), there may be a conformal coating applied prior to the salt atmosphere test.

6.5 Rebonding

Attempts to bond where only impressions have been made in the metal and where the bond did not make a physical attachment to the pad or post shall not be considered evidence of rebonding.

JAN MIL-M-38510
Integrated Circuits

JAN MIL-M-38510 INTEGRATED CIRCUITS

The MIL-M-38510 JAN Program implemented by Texas Instruments provides a standardized qualification and specification system for high-reliability military applications. The program covers a wide range of monolithic integrated circuits including digital and linear device types in both dual-in-line and flat pack configurations. For device types not yet covered by MIL-M-38510 JAN slash sheets or for cost-effectivity and improved availability, the Texas Instruments 38510/MACH IV Program is recommended. It includes all the significant and practical controls, lot acceptances, and screenings included in the MIL-M-38510 JAN Program and is available at approximately one-third of the cost. The 38510/MACH IV Program includes a controlled procurement document encompassing general specifications MIL-M-38510A and MIL-STD-883A dated 15 November 1974. Revision D of the TI 38510/MACH IV specification is included in Tab Section 7 of this book.

The TI 38510/MACH IV Program also offers an aid to specification writing by providing a cost-effective 38510 and 883 base document, whereby special device program specifications may be written invoking any additional testing options unique to a specific program. The TI 38510/MACH IV specification is organized and written per MIL-STD-100 to allow its use as a program specification by merely adding the user's company name and drawing number, as well as any required additions or deletions necessary to meet the specific program goals.

Table I provides a convenient cross-reference from the JAN part numbers to the corresponding standard catalog part numbers. The cross reference from the catalog numbers to the JAN slash sheet numbers is provided in Table II.

The complete JAN part number with the tables of class, case, and lead finish codes is given in Table III, along with a cross reference to the TI 38510/MACH IV part number. A table of standard TI cases and lead finishes is also provided to assist in specifying the proper JAN part number. It is imperative that the proper case and lead finish shown in the table be specified on the parts list and procurement documentation. The specific package for each device is determined by referring to the proper data sheet.

The following figure defines the reliability classes of MIL-M-38510 JAN and TI 38510/MACH IV ICs, and the intended areas of application. MIL-M-38510 recommends that for original equipment complements, the device class appropriate to the need be used, while Class B is recommended for spare parts for logistic support.

RECOMMENDED USE	TYPICAL SYSTEM APPLICATIONS	MIL-STD-883 MIL-M-38510 CLASS	38510/MACH IV LEVEL
Where repair or replacement is readily accomplished and "down time" is not critical	Prototype, noncritical support or ground systems	Class C	I (SNM)
Where repair or replacement is difficult or impossible and reliability is vital	Avionics and tactical missile systems	Class B	III (SNC)
Where repair or replacement is difficult or impossible and reliability is imperative	Critical avionics, space and strategic missile systems	Class A/S	IV (SNH)

Wide acceptance of TI 38510/MACH IV Class B "SNC" level devices has made possible improved availability thru distributor and factory stocking programs. The following military documents (see Note 1) establish the processing, quality, and reliability assurance requirements for JAN integrated circuits. The detail requirements of each individual JAN device are specified in the slash sheets.

MIL-M-38510/XXX, Microcircuits, Digital, TTL, . . ., . . ., Monolithic Silicon (Slash Sheets)
MIL-M-38510A, Microcircuits, General Specification for
MIL-STD-883A, Test Methods and Procedures for Microelectronics
QPL-38510, Qualified Products List for MIL-M-38510

NOTE 1: Copies of these documents may be requested from the Naval Pulbications and Forms Center, 5801 Tabor Avenue, Philadelphia, Pa. 19120.

TABLE I. JAN INTEGRATED CIRCUITS AND CIRCUIT-TYPE CROSS-REFERENCE

JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE
00101	5430	01401	54150	04001	54H50	07501†	54S86
00102	5420	01402	9312‡	04002	54H51	07502†	54S135
00103	5410	01403	54153	04003	54H53	07601†	54S194
00104	5400	01404	9309	04004	54H54	07602†	54S195
00105	5404	01405	54157	04005	54H55	07701†	54S138
00106	5412	01406†	54151	04101	54L51	07702†	54S139
00107	5401	01501	5475	04102	54L54	07703†	54S280
00108	5405	01502	5477	04103	54L55	07801†	54S181
00109	5403	01503	54116	04104♦	54L54	07802†	54S182
00201	5472	01504	9314‡	04201	54L121	07901†	54S151
00202	5473	01601	5408	04202	54L122	07902†	54S153
00203	54107	01602	5409	05001	4011A	07903†	54S157
00204	5476	01701	54174	05002	4012A	07904†	54S158
00205	5474	01702	54175	05003	4023A	07905†	54S251
00206	5470	01703†	54173	05101	4013A	07906†	54S257
00207	5479‡	01801†	54170	05102	4027A	07907†	54S258
00301	5440	01901†	54180	05201	4000A	08001†	54S11
00302	5437	02001	54L30	05202	4001A	08002†	54S15
00303	5438	02002	54L20	05203	4002A	08101†	54S140
00401	5402	02003	54L10	05204	4025A	08201†	54S85
00402	5423	02004	54L00	05301	4007A	10101	52741
00403	5425	02005	54L04	05302	4019A	10102	52747
00404	5427	02006	54L01/54L03	05303	4030A	10103	52101A
00501	5450	02101	54L71	05401	4008A	10104	52108A
00502	5451	02102	54L72	05501	4009A	10105†	LH2101A
00503	5453	02103	54L73	05502	4010A	10106†	LH2108A
00504	5454	02104	54L78	05503	4049A	10201	52723
00601	5482	02105	54L74	05504	4050A	10202†	52104
00602	5483	02201	54H72	05601	4017A	10203†	52105
00603	9304‡	02202	54H73	05602	4018A	10301	52710
00701	5486	02203	54H74	05603	4020A	10302	52711
00801	5406	02204	54H76	05604	4022A	10303	52106
00802	5416	02205	54H101	05605	4024A	10304	52111
00803	5407	02206	54H103	05701	4006A	10401	55107
00804	5417	02301	54H30	05702	4014A	10402	55108
00805	5426	02302	54H20	05703	4015A	10403	55114
00901	5495	02303	54H10	05704	4021A	10404	55115
00902	5496	02304	54H00	05705	4031A	10405	55113
00903	54164	02305	54H04	05706†	4035A	10406†	7831
00904	54165	02306	54H01	05707†	4034A	10501†	52733
00905	54194	02307	54H22	05801†	4016A	10601	LM102‡
00906	54195	02401	54H40	06001	10501‡	10602	52110
00907†	9300‡	02501	54L90	06002	10502‡	10701	52109
00908†	9328	02502	54L93	06003	10505‡	10801†	3018A
00909†	54198	02503†	54L193	06004	10506‡	10802†	3045
00910†	54166	02504†	93L10	06005	10507‡	15001	5485
01001	5442	02505†	93L16	06006	10509‡	15101	5413
01002	5443	02601	54L86	06101†	10531‡	15102	5414
01003	5444	02701	54L02	06102†	10631‡	15103	54132
01004	5445	02801	54L95	06103†	10576‡	15201†	54154
01005	54145	02802	54L164	06104†	10535‡	15202†	54155
01006	5446	02803	93L28‡	07001	54S00	15203†	54156
01007	5447	02804	93L00	07002	54S03	15204†	8250
01008	5448	02805	76L70	07003	54S04	15205†	8251
01009	5449	02806♦	54L91	07004	54S05	15206†	8252
01101	54181	02901	54L42	07005	54S10	15301†	54125
01102	54182	02902	54L43	07006	54S20	15302†	54126
01201	54121	02903	54L44	07007	54S22	15501†	54H08
01202	54122	02904	54L46	07008	54S30	15502†	54H11
01203	54123	02905	54L47	07009	54S133	15601†	54147
01301	5492	02906	76L42A	07010	54S134	15602†	54148
01302	5493	03001	15930	07101	54S74	15801†	9321
01303	54160	03002	15935	07102	54S112	15802†	9301
01304	54163	03003	15936	07103	54S113	15803†	9311
01305	54162	03004	15946	07104	54S114	15804†	9317
01306	54161	03005	15962	07105	54S174	20101	54186 (PROM 512)
01307	5490	03101	15932	07106	54S175	20102	MCM5304‡
01308	54192	03102	15944	07201	54S40	20103†	IM5603A
01309	54193	03103	15957	07301	54S02	20201†	54S387 (PROM 1024)
01310†	54196	03104	15958	07401	54S51	20202†	IM5623
01311†	54197	03105	15933	07402	54S64	23001†	5531 (256 RAM)
01312†	54177	03501	MH0026	07403	54S65	23002†	93410 (256 RAM)

NOTE: Only the basic JAN and SN numbers are shown. Complete the numbers as shown in Table III.
†Slash sheets not released as of date of this publication.
‡Not recommended for new designs.
♦Class S only.

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JAN MIL-M-38510 INTEGRATED CIRCUITS

TABLE I. JAN INTEGRATED CIRCUITS AND CIRCUIT-TYPE CROSS-REFERENCE

JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE
23501†	TMS4060 (4K RAM)	30109†	54LS109	30701†	54LS138	31202†	54LS283
23502†	TMS4050 (4K RAM)	30201†	54LS40	30702†	54LS139	31301†	54LS13
30001†	54LS00	30202†	54LS37	30703†	54LS42	31302†	54LS14
30002†	54LS03	30203†	54LS38	30704†	54LS47	31303†	54LS132
30003†	54LS04	30301†	54LS02	30801†	54LS181	31401†	54LS123
30004†	54LS05	30302†	54LS27	30901†	54LS151	31402†	54LS221
30005†	54LS10	30303†	54LS266	30902†	54LS153	31501†	54LS90
30006†	54LS12	30401†	54LS51	30903†	54LS157	31502†	54LS93
30007†	54LS20	30402†	54LS54	30904†	54LS158	31503†	54LS160
30008†	54LS22	30501†	54LS32	30905†	54LS251	31504†	54LS161
30009†	54LS30	30502†	54LS86	30906†	54LS257	31505†	54LS168
30101†	54LS73	30601†	54LS194	30907†	54LS258	31506†	54LS169
30102†	54LS74	30602†	54LS195	30908†	54LS253	31507†	54LS192
30103†	54LS112	30603†	54LS95	31001†	54LS11	31508†	54LS193
30104†	54LS113	30604†	54LS96	31002†	54LS15	31601†	54LS75
30105†	54LS114	30605†	54LS164	31003†	54LS21	31602†	54LS279
30106†	54LS174	30606†	54LS298	31004†	54LS08	31701†	54LS124
30107†	54LS175	30607†	54LS395	31101†	54LS85	31702†	54LS324
30108†	54LS107	30608†	54LS670	31201†	54LS83A	31801†	54LS261

TABLE II. CIRCUIT-TYPE AND JAN INTEGRATED CIRCUITS CROSS-REFERENCE

CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.
LH2101A	10105†	4016A	05801†	54H72	02201	54LS114	30105†
LH2108A	10106†	4017A	05601	54H73	02202	54LS123	31401†
LM102	10601	4018A	05602	54H74	02203	54LS124	31701†
MCM5304‡	20102	4019A	05302	54H76	02204	54LS132	31303†
MH0026	03501	4020A	05603	54H101	02205	54LS138	30701†
TMS4050	23502 (4K RAM)	4021A	05704	54H103	02206	54LS139	30702†
TMS4060	23501 (4K RAM)	4022A	05604	54LS00	30001†	54LS151	30901†
1M5600	20103	4023A	05003	54LS02	30301†	54LS153	30902†
1M5603A	20103†	4024A	05605	54LS03	30002†	54LS157	30903†
1M5623	20202†	4025A	05204	54LS04	30003†	54LS158	30904†
10501‡	06001	4027A	05102	54LS05	30004†	54LS160	31503†
10502‡	06002	4030A	05303	54LS08	31004†	54LS161	31504†
10505‡	06003	4031A	05705	54LS10	30005†	54LS164	30605†
10506‡	06004	4034A	05706†	54LS11	31001†	54LS168	31505†
10507‡	06005	4035A	05707†	54LS12	30006†	54LS169	31506†
10509‡	06006	4049A	05503	54LS13	31301†	54LS174	30106†
10531‡	06101†	4050A	05504	54LS14	31302†	54LS175	30107†
10535‡	06104†	52101A	10103	54LS15	31002†	54LS181	30801†
10576‡	06103†	52104	10202†	54LS20	30007†	54LS192	31507†
10631‡	06102†	52105	10203†	54LS21	31003†	54LS193	31508†
15930	03001	52106	10303	54LS22	31008†	54LS194	30601†
15932	03101	52108A	10104	54LS27	30302†	54LS195	30602†
15933	03105	52109	10701	54LS30	30009†	54LS221	31402†
15935	03002	52110	10602	54LS32	30501†	54LS251	30905†
15936	03003	52111	10304	54LS37	30202†	54LS253	30908†
15944	03102	52710	10301	54LS38	30203†	54LS257	30906†
15946	03004	52711	10302	54LS40	30201†	54LS258	30907†
15957	03103	52723	10201	54LS42	30703†	54LS261	31801†
15958	03104	52733	10501†	54LS47	30704†	54LS266	30303†
15962	03005	52741	10101	54LS51	30401†	54LS279	31602†
3018A	10801†	54H00	02304	54LS54	30402†	54LS283	31202†
3045	10802†	54H01	02306	54LS73	30101†	54LS298	30606†
4000A	05201	54H04	02305	54LS74	30102†	54LS324	31702†
4001A	05202	54H08	15501†	54LS75	31601†	54LS395	30607†
4002A	05203	54H10	02303	54LS83A	31201†	54LS670	30608†
4006A	05701	54H11	15502†	54LS85	31101†	54L00	02004
4007A	05301	54H20	02302	54LS86	30502†	54L01	02006
4008A	05401	54H22	02307	54LS90	31501†	54L02	02701
4009A	05501	54H30	02301	54LS93	31502†	54L03	02006
4010A	05502	54H40	02401	54LS95	30603†	54L04	02005
4011A	05001	54H50	04001	54LS96	30604†	54L10	02003
4012A	05002	54H51	04002	54LS107	30108†	54L20	02002
4013A	05101	54H53	04003	54LS109	30109†	54L30	02001
4014A	05702	54H54	04004	54LS112	30103†	54L42	02901
4015A	05703	54H55	04005	54LS113	30104†	54L43	02902

NOTE: Only the basic JAN and SN numbers are shown. Complete the numbers as shown in Table III.
†Slash sheets not released as of date of this publication.
‡Not recommended for new designs.

TABLE II. CIRCUIT-TYPE AND JAN INTEGRATED CIRCUITS CROSS-REFERENCE

CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.
54L44	02903	54S140	08101†	5447	01007	54164	00903
54L46	02904	54S151	07901†	5448	01008	54165	00904
54L47	02905	54S153	07902†	5449	01009	54166	00910†
54L51	04101	54S157	07903†	5450	00501	54173	01703†
54L54	04102, 04104♦	54S158	07904†	5451	00502	54174	01701
54L55	04103	54S174	07105	5453	00503	54175	01702
54L71	02101	54S175	07106	5454	00504	53177	01312†
54L72	02102	54S181	07801†	5470	00206	54180	01901†
54L73	02103	54S182	07802†	5472	00201	54181	01101
54L74	02105	54S194	07601†	5473	00202	54182	01102
54L78	02104	54S195	07602†	5474	00205	54186	20101
54L86	02601	54S251	07905†	5475	01501	54192	01308
54L90	02501	54S257	07906†	5476	00204	54193	01309
54L91	02806♦	54S258	07907†	5477	01502	54194	00905
54L93	02502	54S280	07703†	5479‡	00207	54195	00906
54L95	02801	54S387	20201†	5482	00601	54196	01310
54L121	04201	5400	00104	5483	00602	54197	01311†
54L122	04202	5401	00107	5485	15001	54198	00909†
54L164	02802	5402	00401	5486	00701	5531	23001† (256 RAM)
54L193	02503†	5403	00109	5490	01307	55107	10401
54S00	07001	5404	00105	5492	01301	55108	10402
54S02	07301†	5405	00108	5493	01302	55113	10405
54S03	07002	5406	00801	5495	00901	55114	10403
54S04	07003	5407	00803	5496	00902	55115	10404
54S05	07004	5408	01601	54107	00203	76L42A	02906
54S10	07005	5409	01602	54116	01503	76L70	02805
54S11	08001†	5410	00103	54121	01201	7831	10406†
54S15	08002†	5412	00106	54122	01202	8250	15204†
54S20	07006	5413	15101	54123	01203	8251	15205†
54S22	07007	5414	15102	54125	15301†	8252	15206†
54S30	07008	5416	00802	54126	15302†	93L00	02804
54S40	07201	5417	00804	54132	15103	93L10	02504†
54S51	07401	5420	00102	54145	01005	93L16	02505†
54S64	07402	5423	00402	54147	15601†	93L28‡	02803
54S65	07403	5425	00403	54148	15602†	9300‡	00907†
54S74	07101	5426	00805	54150	01401	9301‡	15802†
54S85	08201	5427	00404	54151	01406†	9304‡	00603
54S86	07501†	5430	00101	54153	01403	9308	01503
54S112	07102	5437	00302	54154	15201†	9309	01404
54S113	07103	5438	00303	54155	15202†	9311	15803†
54S114	07104	5440	00301	54156	15203†	9312‡	01402
54S133	07009	5442	01001	54157	01405	9314‡	01504
54S134	07010	5443	01002	54160	01303	9317	15804†
54S135	07502†	5444	01003	54161	01306	9322	01405
54S138	07701†	5445	01004	54162	01305	9328	00908
54S139	07702†	5446	01006	54163	01304	93410	23002 (266 RAM)

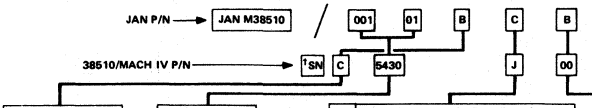
NOTE: Only the basic JAN and SN numbers are shown. Complete the numbers as shown in Table III.

†Slash sheets not released as of date of this publication.

‡Not recommended for new designs.

♦Class S only.

TABLE III. TI JAN AND 38510/MACH IV INTEGRATED CIRCUITS



CLASS	
JAN	†38510/ MACH IV
A/S*	H
B	C
C	M

CIRCUIT TYPE
See Cross Reference Tables I & II

BLOCK A											
JAN CASE OUTLINE & FINISH FOR TI FAMILIES											
PRODUCT	A	B	C	D	E	F	G	I	J	L	
SERIES 54			X	X	X	X			X	X	
SERIES 54H			X	X	X	X					
SERIES 54L		X									
SERIES 54LS			X	X	X	X			X	X	
SERIES 54S			X	X	X	X			X	X	
SERIES 52	X		X				X	X			
SERIES 55	X		X		X	X					
†SERIES 4000 (CMOS)			X	X	X	X					
†MOS LSI										X	X
LEAD FINISH A											
LEAD FINISH B			X	X	X	X			X	X	X
LEAD FINISH C	X	X					X	X			

	CASE OUTLINE (SEE BLOCK A)		
JAN	PACKAGE	38510 (APP.C)	38510/ MACH IV
A	1/4" X 1/4" FLAT-14	F-1	FA
B/T*	1/4" X 1/8" FLAT-14	F-3	T
C	DIP-14	D-1	J
D	1/4" X 3/8" FLAT-14	F-2	W
E	DIP-16	D-2	J
F	1/4" X 3/8" FLAT-16	F-5	W/SB
G	TO-99	A-1	L
H	1/4" X 1/4" FLAT-10	F-4	U
I	TO-100	A-2	L
J	DIP-24	D-3	J
K	3/8" X 5/8" FLAT-24	F-6	W
L	3/8" X 1/2" FLAT-24	F-7	W
‡	DIP-22	‡	J
‡	DIP-18	‡	J
X	TO-5	–	–
Y	TO-3	–	–
Z	1/4" X 3/8" FLAT-24	F-8	–

LEAD FINISH (SEE BLOCK A)		
JAN	TYPE	38510/ MACH IV
A	SOLDER DIP	10
B	TIN-PLATE	00
C	GOLD-PLATE	00

NOTES:

1. Complete the 38510/MACH IV number by adding prefix for class, and suffixes for case outline and lead finish to the basic circuit type number as shown above.

   Example:
   SNC5430J-00

2. Complete the JAN number by adding a three letter suffix for class, case outline, and lead finish as shown above.

   Example:
   JAN M38510/00101BCB

†Prefix designation for Class B 38510/MACH-IV for CMOS is "TFC" and for MOS LSI is "SMC".
‡Unassigned.
*Per MIL-M-0038510B.